IEEE Access
Multidisciplinary | Rapid Review | Open Access Journal

Received March 26, 2020, accepted April 6, 2020, date of publication April 13, 2020, date of current version May 6, 2020.

Digital Object Identifier 10.1109/ACCESS.2020.2987620

Closed-Loop Control and Performance Evaluation of Reduced Part Count Multilevel Inverter Interfacing Grid-Connected PV System

PRABHAT RANJAN BANA[1], (Graduate Student Member, IEEE), KAIBALYA PRASAD PANDA[1], (Graduate Student Member, IEEE), SANJEEVIKUMAR PADMANABAN[2], (Senior Member, IEEE), LUCIAN MIHET-POPA[3], (Senior Member, IEEE), GAYADHAR PANDA[1], (Senior Member, IEEE), AND JIANZHONG WU[4], (Member, IEEE)

[1]Department of Electrical Engineering, National Institute of Technology at Meghalaya, Shillong 793003, India
[2]Department of Energy Technology, Aalborg University, 9220 Aalborg, Denmark
[3]Faculty of Engineering, Østfold University College, 1757 Halden, Norway
[4]School of Engineering, Cardiff University, Cardiff CF24 3AA, U.K.

Corresponding authors: Kaibalya Prasad Panda (kaibalyapanda@nitm.ac.in) and Sanjeevikumar Padmanaban (san@et.aau.dk)

ABSTRACT Multilevel inverters (MLIs) have drawn tremendous attention in the power sector. Application of MLI has grown extensively to improve the power quality and efficiency of the photovoltaic (PV) system. For an MLI interfacing PV system, the size, cost and voltage stress are the key constraints of the MLI that need to be minimized. This paper presents a novel reduced part count MLI interfacing single-stage grid-tied PV system along with a closed-loop control strategy. The proposed MLI consists of n repeating units and a level boosting circuit (LBC) that assists in generating $4n + 7$ voltage levels instead of $2n + 3$ levels. Three different algorithms are proposed for a proper selection of dc-link voltages to enhance the levels further. A comparative analysis is carried out to confirm the superiority of the developed MLI. The workability of the proposed MLI is investigated with a 1.3 kW PV system. The closed-loop control strategy ensures the maximum power tracking, dc-link voltage balancing, satisfactory operation of the MLI and injection of clean sinusoidal grid current under any dynamic changes. Comprehensive simulation analysis is carried out considering a 15-level MLI structure. Experimental tests further confirm the practicality of the topological advancement for a PV system under different dynamic conditions.

INDEX TERMS Asymmetrical repeating unit, distributed maximum power point tracking, multilevel inverter, photovoltaic (PV) system, reduced components.

I. INTRODUCTION

Research attempts for the development of renewable energy-based power generation systems integrated with multilevel inverter (MLI) are burgeoning. These systems developed for both the standalone and grid-tied applications [1]–[3]. The primary goal of such systems is to attain full power with reduced harmonic distortion, low power loss, and low voltage stress, unlike the commonly used three-level inverter. In retrospect, the cascaded H-bridge (CHB) MLI structures employed extensively interfacing with photovoltaic (PV) systems [4]–[6] for higher reliability and easy modularity. Consequently, higher power rating and higher voltage levels achieved as per the requirement. CHB MLI requires multiple isolated dc sources in each H-bridge, thus making it highly suitable for PV application as individual PV panel used in each H-bridge along with distributed maximum power point tracking (DMPPT) control. It can help in harvesting maximum energy from the PV sources [4], [7], [8]. On the contrary, single dc source-based MLIs such as diode-clamped and capacitor-clamped MLI demands several components and complex control circuitry to synthesize multilevel output [9], [10]. The shortcoming of conventional MLIs is the involvement of a higher number of power devices.

The associate editor coordinating the review of this manuscript and approving it for publication was Ramazan Bayindir.

In such cases, the switching losses are more as the semiconductor switches generally operate at high frequency. Although the asymmetrical CHB MLI structure can reduce the number of switching devices but still, the switch count stands high and control complexity increases for higher-level applications [11], [12].

MLIs have immense capability to improve the efficiency of the solar PV system. Such a system integrated with the grid through a dc-dc converter (single-stage) or without it (two-stage). Although both the configurations have nearly the same loss factor and efficiency, the single-stage configuration can save the cost of additional dc-dc converters [13]. Several CHB MLI based single/two-stage PV power conversion systems reported in the literature. Single-stage structure in [5] adopted fuzzy logic for controlling the CHB MLI operating in standalone as well as in grid-connected mode. Individual PV panel control, dc-link voltage balancing, maximum power tracking, and phase-shifted pulse width modulation (PWM) control further explored in [14]. To deal with heavy mismatch condition in large scale two-stage PV interfaced CHB MLIs, detailed system analysis is reported in [4]. DMPPT thereby incorporated to extract maximum power, from all the sub-modules of the MLI under uniform as well as partially shaded conditions. A cascaded quasi-Z source MLI for a PV system is further explored in [15] addressing single-stage dc-dc conversion and inversion along with the second harmonic voltage and current ripples in the Z source network.

It is worth mentioning that the efficiency of the solar PV system is very low. Thus, the use of conventional MLIs in such a system is not an ideal choice. In this context, several reduced switch MLIs (RSMLIs) have been developed in recent years [16]. By reducing the number of components, the power losses reduced, and the efficiency of the standalone/grid-connected PV system can be improved [17], [18]. Several single-phase and three-phase 5-level RSMLIs using reduced power devices have been proposed in [8], [19], [20] for grid-tied PV systems. These MLIs altogether uses eight switches per phase and comprises an H-bridge for changing the polarity at the output. The DMPPT, global MPPT, and inter-phase power balancing addressed in [8]. Extending the structure proposed [19], a two-stage grid-tied PV MLI system introduced in [21]. This work deals with capacitor voltage balancing issues, and also several grid side control objectives addressed. In [20], the issues related to the reduction of leakage current and common-mode voltage investigated in detail. Three-phase asymmetrical RSMLI structures are subsequently developed in [22], [23] that uses a reduced number of switches for the generation of multilevel output.

Continuing the research trend, MLIs are further explored broadly in two forms, i.e., switched-diode based or switched-capacitor based RSMLI. The authors in [18], [24], [25] have introduced a cascaded MLI based on the switched-diode modules for standalone applications. Use of diodes makes the circuit simple and reduces the switch count and control complexity. Several switched-capacitor based MLIs that allow dc source reduction is also witnessed in the literature with level boosting feature. The developed MLI in [26] is an example of it which is a CHB MLI, but with additional bidirectional switches used to replace the isolated dc sources by capacitors.

Nevertheless, the switch count is higher compared to a CHB MLI. The MLI topologies proposed in [27]–[31] adopt the switched-capacitor principle to reduce the source count as well as the switch count. The capacitors are self-balanced at the desired voltage by charging in parallel from the input dc source and discharging in series through the load. Appropriate charging & discharging of capacitors, capacitance sizing, and dc-link voltage balancing are the critical challenges of these MLI types [32].

Apart from reducing the switch count, minimization of voltage stress is also a key factor. Besides the above-discussed RSMLIs that address this issue, different types of level boosting circuits (LBCs) developed to optimize the MLI and addition, reduce the stress. In [3], [33]–[35], the introduced LBC doubles the number of levels and reduces the component count per level ratio (CLR). Almost all the above-cited MLIs formed by combining a low-frequency H-bridge as polarity generation unit and high-frequency level generation units. The level of generating units can be cascaded to increase the number of levels. The switches in the H-bridge withstand higher voltage stress than the level generating units. Few compact module hybrid MLI structures, therefore, realized without using an H-bridge [36], [37].

It is evident from the above discussion that there is a need for an optimized PV MLI that possibly reduces the number of semiconductor devices, device stress and power losses. In addition, the power quality and efficiency of the (PV) system can be improved. This work presents a detailed analysis of the grid-tied single-phase single-stage PV system interfaced with a novel MLI. Structural and functional analysis of the proposed MLI detailed in Section II and Section III highlights the superiority of the proposed MLI compared to the prior art topologies. In Section IV, a closed-loop PWM control strategy developed to balance the individual dc-link voltages, synthesize the desired staircase output with low distortion under any perturbations, and maintain the power quality of the grid-tied system. Extensive simulation and experimental analysis of the proposed system is presented in Section V & VI, respectively. In the end, concluding remark on the whole research work is presented.

II. PROPOSED SYSTEM CONFIGURATION

The generalized structure of the proposed voltage level boost (VLB) MLI for the single-stage grid-connected PV system shown in Fig. 1. As indicated, VLB MLI is the combination of three modules such as; repeating unit (RU), H-bridge, and LBC. RU consists of two PV strings as input sources which can be repeated in a series manner to achieve higher voltage levels. Moreover, the inclusion of LBC in the VLB MLI exactly doubles the number of levels with the addition of four extra switches. Numbers of switches (N_{sw}), the number of sources (N_{dc}) and the number of diodes (N_{dd})

TABLE 1. Proposed algorithms for suitable selection dc-links in VLB MLI.

Parameters	Proposed Algorithm 1 (PA1)	Proposed Algorithm 2 (PA2)	Proposed Algorithm 3 (PA3)
Magnitude of dc-links	$V_1 = V_3 = \cdots = V_{2n-1} = V_{dc}$ (Asymmetrical)	$V_1 = V_{dc}, V_3 = 2V_{dc}, \ldots V_{2n-1} = nV_{dc}$ (Arithmetic progression)	$V_1 = V_{dc}, V_3 = 2V_{dc}, \ldots V_{2n-1} = 2^{n-1}V_{dc}$ (Binary ratio)
		$V_2 = V_4 = \cdots = V_{2n} = V_{dc}/n, V_L = 0.5V_{dc}$	
N_l	$4n + 7$	$2n^2 + 2n + 7$	$2^{n+2} + 3$
TBV ($\times V_{dc}$)	$(5n + 6)$	$0.5(5n^2 + 5n + 12)$	$5.2^n + 1$
S_{loss}	$4(n + 1)f_o + (n + 2)f_s$	$2(n^2 + n + 2)f_o + 0.5(n^2 + n + 4)f_s$	$(2^{n+2})f_o + (2^n + 1)f_s$

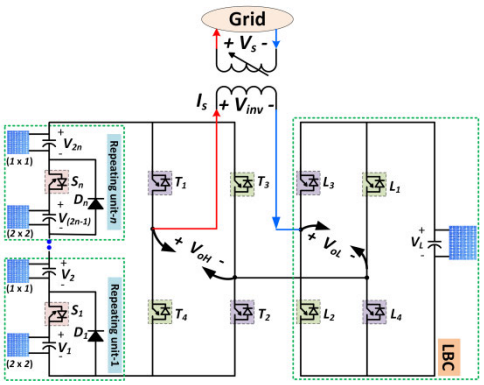

FIGURE 1. Proposed MLI interfacing grid-tied PV system.

involved in the VLB MLI in terms of RU (n) are expressed in (1-3). In this work, the VLB MLI is integrated with the grid through a small size low pass filter (inductor) to reduce further the current harmonics caused by switching action. Moreover, optimization of the proposed system attempted in two ways, i.e., use of dc-dc converter eliminated, and three different algorithms to select input source magnitude developed for reducing the source count.

$$\text{Number of switches } (N_{sw}) = n + 8 \tag{1}$$

$$\text{Number of input sources } (N_{dc}) = 2n + 1 \tag{2}$$

$$\text{Number of diodes } (N_d) = n \tag{3}$$

Other than the component count, total blocking voltage (TBV) is an important parameter to be considered while designing an MLI. TBV is the addition of blocking voltage of each switch which decides the suitability of MLI for a different level of voltage application. In this respect, blocking voltage by the RU switches, H-bridge switches, and LBC switches expressed in (4-6), respectively considering V_1, $V_2, \ldots, V_{2n-1}$, V_{2n}, and V_L as the dc-link voltages.

$$V_{S1} = V_1, \quad V_{S2} = V_3, \ldots, V_{Sn} = V_{2n-1} \tag{4}$$

$$V_{L1} = \ldots = V_{L4} = V_L \tag{5}$$

$$V_{T1} = \ldots = V_{T4} = (V_1 + V_2 + \ldots + V_{2n-1} + V_{2n}) \tag{6}$$

A. PROPOSED ALGORITHMS (PA)

Magnitudes of the dc-links for RUs are selected as per the algorithms presented in Table 1. Magnitudes can be selected as asymmetrical, arithmetic and binary ratio according to PA1, PA2 and PA3, respectively. The generalized

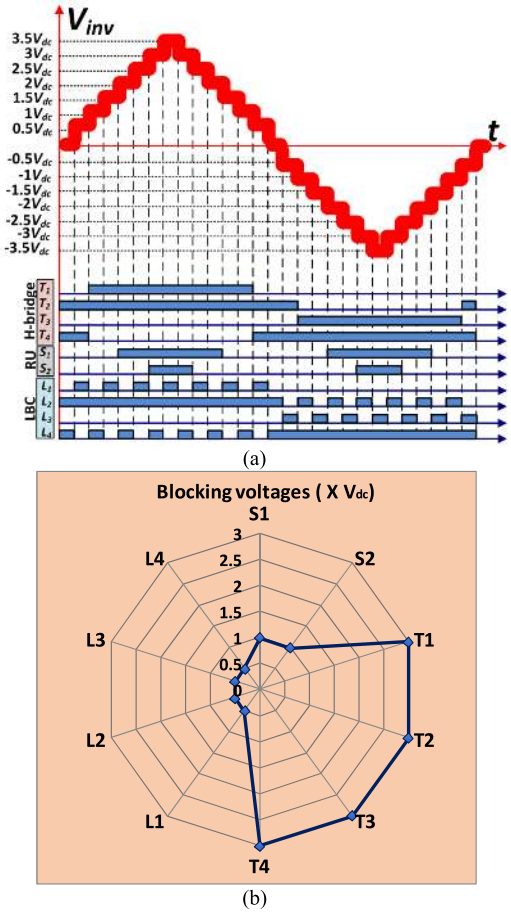

FIGURE 2. (a) Switching states for producing 15-level output. (b) Blocking voltages of the individual switch for the 15-level MLI.

expressions for the output voltage levels (N_l), TBV, and switching loss (S_{loss}) in terms of RUs also included. This work analyzes the performance of the VLB MLI considering PA1.

The VLB MLI produces a 15-level output with PA1 when two RUs (i.e., with ten switches) are taken into consideration. Fig. 2(a) shows the expected 15-level staircase output waveform with switching pulse duration of all the switches. The source used in the LBC is responsible for the generation of the first step while the second step is produced by turning off the switches in the RU along with deactivating the LBC. The third step can be obtained by activating the LBC source. Afterwards, RUs are switched to generate the fourth step and the further. For the 15-level case, blocking voltages

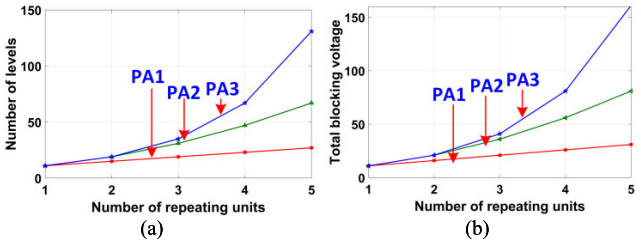

FIGURE 3. Comparison of PA (a) N_l versus n. (b)TBV versus n.

across each switch is illustrated in Fig. 2(b). Performance of the VLB MLI with the three proposed algorithms is further evaluated in Fig. 3(a) & (b). The N_l increases significantly considering PA3; however, TBV also increases accordingly.

III. COMPARATIVE ANALYSIS

The prime purpose of the current work is to devise a novel MLI structure having lesser switch count and TBV. To validate the competence, the proposed VLB MLI is compared with different MLI topologies developed recently. Hereafter the MLI topologies in [18], [28], [38], [23], [36], [29], [37], [26] are termed as T1, T2, …, T8. The MLI presented in [26] utilizes a higher number of switches but reduces the source count. The MLIs presented in [29], [36], [37] employs lesser switch count than a conventional CHB MLI, but the reduction is not significant as compared to the presented MLIs in [18], [23], [28], [38]. Accordingly, the superiority of the proposed VLB MLI acknowledged from Fig. 4(a). Moreover, it is observed that some of the MLI topologies use diodes in the circuit. The MLIs in [18], [28], [29] employ diodes to synthesize a staircase output. It is obvious from Fig. 4(b) that, the VLB MLI requires less number of diodes among all the compared MLIs.

Addition of more number of dc sources will result in more number of voltage levels, but at the same time, TBV will increase. The MLI topologies developed in [26], [28], [29], [38] involves a single dc source and additional capacitors for generating multiple voltage levels. All these MLI topologies are corroborated for lower-level applications. Although TBV becomes less for these MLIs, but voltage balancing issue and control complexity may arise in higher-level applications. It is clear from Fig. 4(c) that, the proposed VLB MLI requires a lesser number of dc sources to synthesize the same level output. Fig. 4(d) shows there is no need for additional capacitors in the proposed MLI. Further, CLR is calculated for all the MLI topologies for evaluating a generic cost comparison. CLR is the ratio of sum of the cost deciding parameters (N_{sw}, N_d, N_c, N_{dc}, and the number of driver circuits) with N_l. In this perspective, the VLB MLI exhibits a lower value of CLR among all the considered MLIs, as shown in Fig. 4(e) which indicates the cost-effectiveness of the proposed structure.

TBV is an important parameter which decides the applicability of an MLI in high voltage. In order to compute the TBV, the blocking voltages of all the individual switches are added together. The blocking voltages for the proposed MLI are summarized in (4-6) along with TBV in Table 1 for PA1, PA2, and PA3. Significant reduction in TBV can be clearly noted from Fig. 4(f). Furthermore, Table 2 presents a summary of well known standalone and grid-tied MLI interfacing PV systems.

IV. CONTROL STRATEGY

The 15-level VLB MLI utilizes two varieties of dc-link voltages ($0.5V_{dc}$ & V_{dc}). Thus it is most important to control the dc-link voltage so that they can be maintained at

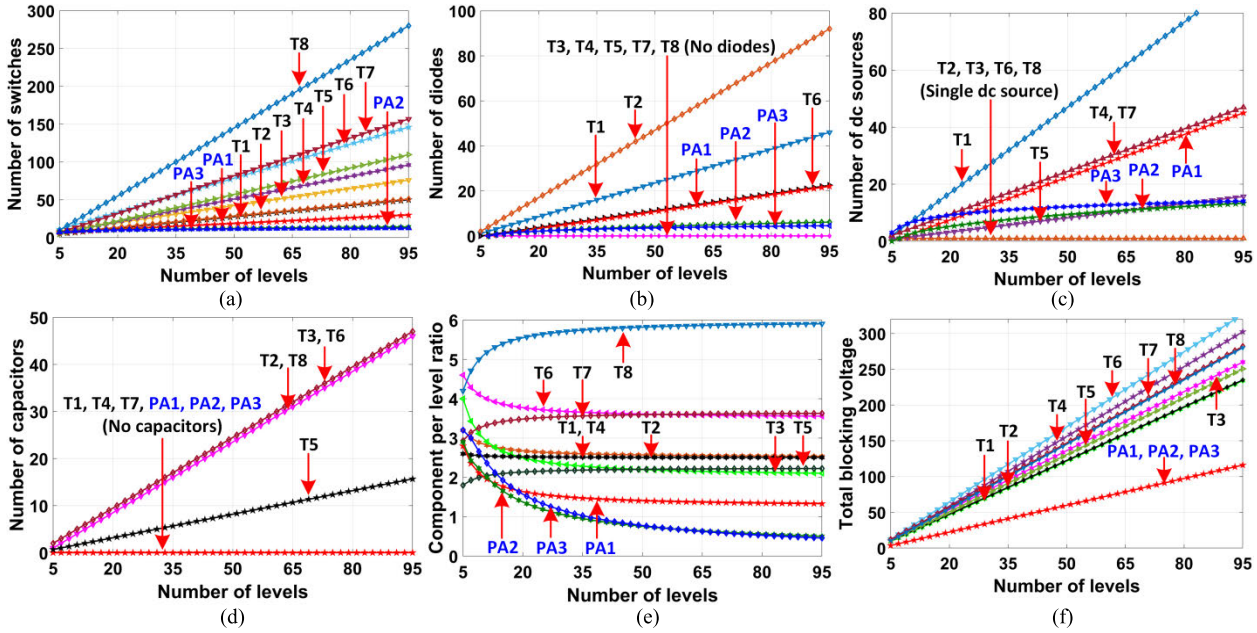

FIGURE 4. Comparison with state-of-art MLI structures (a) N_{sw} versus N_l, (b) N_{dd} versus N_l, (c) N_{dc} versus N_l, (d) N_c versus N_l, (e) CLR versus N_l, (f) TBV versus N_l.

TABLE 2. Comparison of MLI interfacing PV systems.

Topologies	N_l	N_{sw}/N_l	TBV (X V_{dc}) /N_l	Polarity change	Remarks (1. Structure Type, 2. MLI Control Technique & 3. Suggested system)
[8]	5	1.6	2	With H-bridge	1. Hybrid modular MLI 2. PS-PWM 3. Grid-connected single-stage PV
[11]	19	0.631	1.89	With H-bridge	1. CHB MLI 2. SPWM 3. Grid connected single-stage PV
[19]	5	1	1.8	With H-bridge	1. Modular multi-string MLI 2. SPWM 3. Grid-connected two-stage PV
[21]	9	1.11	2	With H-bridge	1. Hybrid modular MLI 2. PS-PWM 3. Grid-connected two-stage PV
[20]	5	1.6	2	With H-bridge	1. Hybrid cascaded extendable MLI 2. High switching frequency control 3. Grid-connected single-stage PV
[30]	17	0.588	1	Without H-bridge	1. Single source boost type MLI 2. High switching frequency control 3. Grid-connected two-stage PV
[26]	7	2.28	2.28	With H-bridge	1. Single source cascaded boost MLI 2. PS-PWM 3. Single-stage standalone PV
[18]	7	0.857	2	With H-bridge	1. Switched diode type MLI 2. SHE & SPWM control 3. Two-stage standalone PV
Proposed	15	0.66	1.06	With H-bridge	1. Voltage level boost MLI 2. PD-PWM 3. Grid-connected single-stage PV

desired values. In this aspect, a suitable close loop control strategy has been employed for the grid-tied PV fed VLB MLI system with critical objectives such as maximum power extraction from the PV-array, dc-link voltage balancing under dynamic change in insolation, injection of clean sinusoidal grid current at unity power factor, control of overall system under phase change and grid side perturbations. The comprehensive control system is shown in Fig. 5.

A. MPPT CONTROL

The performance of the PV systems is highly dependent on the temperature and insolation level, which are not uniform throughout the day. For harvest maximum power, MPPT control technique is adopted, which will make the sure operation of PV at MPP. Although various MPP tracking techniques have been investigated in literature [39], [40], incremental conductance MPPT [13], [40] is implemented due to its full viability and simplicity. The MPPT control then produces the reference voltage signal for the voltage control loop. For efficiently extract maximum PV power under insolation mismatch conditions, DMPPT control is performed, i.e., MPP tracking is carried out in each RUs. The required reference current is further generated by comparing the actual individual PV voltages with the total PV voltage.

B. TOTAL VOLTAGE CONTROL LOOP

Closed-loop voltage control is employed to maintain the total dc-link voltage corresponding to the reference set voltage considering any change in PV characteristics. The control loop calculates error taking the sum of the actual/measured dc-link voltages (V_{total}) and the sum of individual reference dc-link voltages (V_{total*}) that are generated from the MPPT control algorithm. The obtained voltage error is minimized by processing it through a proportional-integral (PI) controller. The parameters (K_{p1}, K_{i2n}) of this PI-controller are tuned so that the peak value of the injected grid current becomes maximum. Further, a phase-locked loop (PLL) is used to synchronize with the grid frequency.

C. INDIVIDUAL VOLTAGE CONTROL LOOP

Although the total voltage controller module maintains the total dc-link voltage at the desired value, but individual dc-link balancing is not guaranteed. Therefore, an individual control loop is also used for balancing each dc-links. The output of each individual voltage control modules is used to generate the reference signal for PD-PWM controller of VLB MLI.

D. CURRENT CONTROL LOOP

For obtain the desired power balancing in addition to the voltage control, a current controller is used to maximize the PV output. This current control loop generates the current error by comparing the reference grid current (I_s^*) and the actual/measured grid current (I_s) which is then processed through a PI-controller. The parameters of the PI-controller (K_p, K_i) are tuned for optimizing the error.

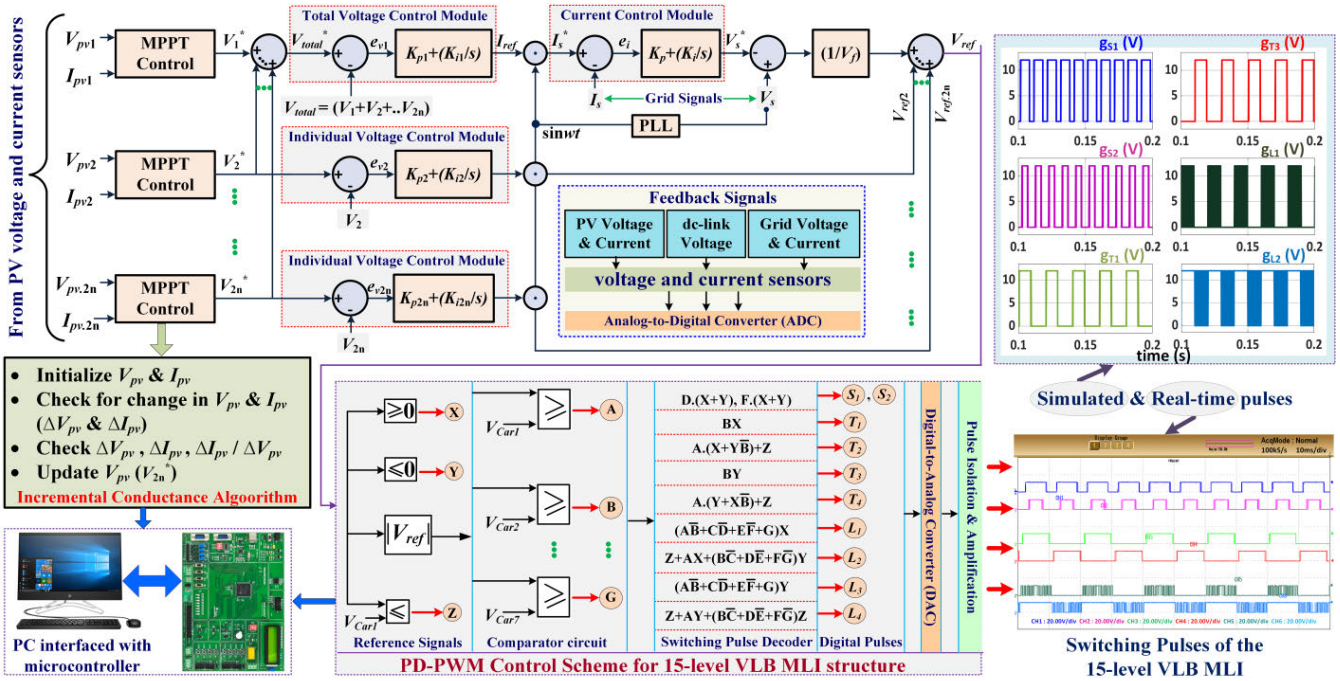

FIGURE 5. Closed-loop control scheme for the proposed grid-tied PV system.

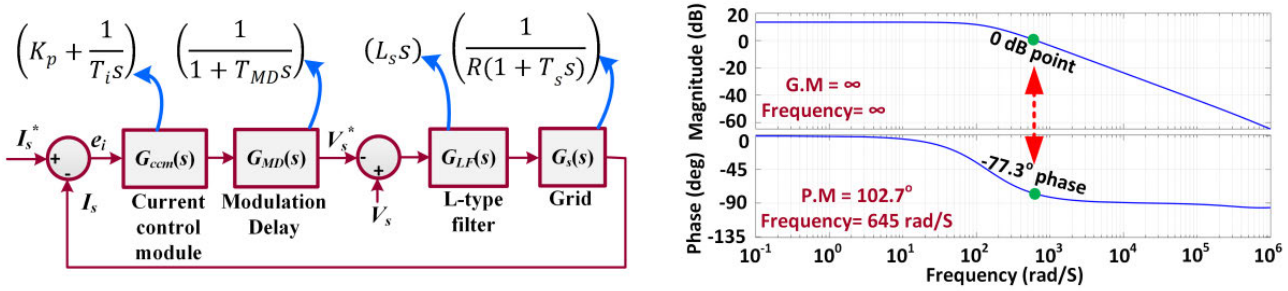

FIGURE 6. Equivalent block diagram of the closed-loop current controller & stability performance.

The output of this controller is compared with the grid voltage (V_s) for generating the reference voltage of the inverter for any change in V_s. Accordingly, the inverter voltage follows the grid voltage under every unwanted circumstance.

E. PHASE-DISPOSITION PWM CONTROL OF VLB MLI

The phase-disposition PWM (PD-PWM) control scheme can be implemented in three stages such as; reference signal generator, a comparator circuit, and switching pulse decoder. For an MLI to produce N_l level output, $(N_l - 1)/2$ number of triangular carriers are required for the aforesaid control mechanism [10]. Thus, seven carriers are disposed of in-phase with a precise offset level for the 15-level VLB MLI. Thereby, the carriers are compared with the reference sinusoidal signal in the comparator circuit for producing seven switching states. The switching pulse decoder circuit comprises of several digital logic gates then generate pulses considering switching logic as illustrated in Fig. 2(a) for all the ten switches.

F. STABILITY ANALYSIS

The stable functionality of the adopted closed-loop controller for the proposed grid-tied system [11] is examined in this section. The overall equivalent block diagram shown in Fig. 6 is considered for stability analysis. The overall transfer function (TF) of the proposed system in Laplace domain ($G(s)$) is computed taking the product of TF of current control module ($G_{ccm}(s)$), modulation delay ($G_{MD}(s)$), grid ($G_s(s)$), and L-type filter ($G_{LF}(s)$). The value of the proportional gain (K_p) & integral gain (K_i) of the current control module is taken as 0.7 & 10, respectively. The integral time constant (T_i) is the reciprocal of K_i. The time of modulation delay (T_{MD}) is considered as 1.5 times of sampling time (T_s). Fig. 6 also depicts the bode plot stability analysis of the considered system. The phase margin (PM) is computed to be 102.7° and the phase plot stabilizes much ahead of −180°. Therefore, the gain margin (GM) of the proposed system is infinite. It may be concluded from the figure that both GM & PM values are more significant than zero, which verifies a stable control strategy.

TABLE 3. Simulation & experimental design parameters.

Parameter	Value
Standard insolation & temperature	1 kW/m^2, 25° C
Total PV array power (P_{pv})	1.375 kW
Maximum power of PV panel (P_{mp})	125 W
Open circuit voltage of PV (V_{oc})	21.4 V
Short-circuit current of PV (I_{sc})	7.6 A
Voltage & current at P_{mp} (V_{mp}, I_{mp})	17.7 V, 7.1 A
Panel efficiency	16.3 %
No. of series, parallel modules (N_{s1}xN_{p1}), (N_{s2}xN_{p2})	(2x2), (1x1)
Grid voltage (V_s)	90 V (peak)
Grid impedance	0.7 Ω-5 mH
dc-link capacitors	1500 µF, 2200 µF
Filter inductance (L_s)	4.7 mH
Inverter output & switching frequency (f_o, f_{sw})	50 Hz, 5 kHz

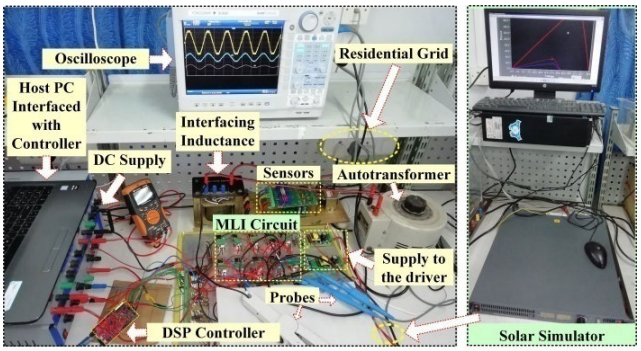

FIGURE 7. Experimental test setup of the proposed system.

V. SIMULATION ANALYSIS

In this section, the operation of 15-level VLB MLI in single-stage grid-tied PV system under MATLAB/Simulink environment is investigated. The adopted closed-loop control strategy as outlined earlier makes sure maximum PV power extraction and the dc-links are maintained at desired voltage levels ($0.5V_{dc}$ & V_{dc}). PV panels are connected to the VLB MLI through the 1500 μF & 2200 μF dc-link capacitors. The values are chosen, considering 2-3 % voltage ripple and nominal output frequency. The carrier frequency and reference sinusoidal frequency are chosen as 5 kHz & 50 Hz. Several 125 W PV panels arranged in (2×2) and (1×1) are considered as an input source for the VLB MLI to obtain the desired dc-link voltage V_{dc} & $0.5V_{dc}$, respectively. The parameters considered in the simulation are given in Table 3. Fig. 8(a) shows the output voltage of the proposed VLB MLI (V_{inv}) and injected grid current (I_s) at different *MI* values ($MI = 0.5$, $MI \approx 1$, $MI > 1$). With the decrease in *MI* value, the MLI is able to operate at a reduced voltage level. On the other hand, overmodulation ($MI > 1$) causes distortion in voltage waveform. Hence, it is always desirable to operate near unity *MI* value. Fig. 8(b) depicts the harmonic spectra of the output voltage of the MLI and grid current. The % THD values of both output voltage and current waveform are below 5% obeying the IEEE-519 standard.

Tests are further conducted under different dynamic conditions. Fig. 8(c) shows the results with varying insolation at 0.12 s to 300 W/m^2 from 750 W/m^2. During this, the grid voltage (V_s) remains unaffected; however, grid current magnitude changes accordingly with insolation change. MPP tracking performance is also delineated in Fig. 8(d). The dc-link voltage is automatically tracked to the reference value and maintained at the desired level even under a change in insolation level. Voltage sag is a common incident in the power system network which is generally caused by faults in the transmission line, sudden load change or excessive load demand. Under voltage sag initiated at 0.4 s, Fig. 8(e) also shows the grid current increases to an extent which ensures the power balance, *i.e.*, the injected power to the grid is maintained Moreover; the PV fed VLB MLI continuously injects a clean sinusoidal current to the grid even under 0.94 lagging power factor (PF) condition as shown in Fig. 8(f). However, the proposed converter can result in unsatisfactory performance under very low PF due to the presence of discrete diodes in the conducting path.

VI. EXPERIMENTAL VERIFICATION

The real-time operation of the proposed VLB MLI in grid-connected mode is verified on a prototype developed in the laboratory, as shown in Fig. 7. The 12N60A4D insulated gate bipolar transistors (IGBTs) and RGP30D discrete diodes are used to build the power circuit. According to the current laboratory availability, one SAS 120/10 solar simulator and four variable dc sources are used as input sources to mimic the PV panel characteristics. Solar simulator and dc sources voltage magnitudes are so adjusted according to Table 3. The output of the VLB MLI is connected to the residential grid through an auto-transformer which steps down the grid voltage to match with the inverter output such that the current from the PV fed MLI can be continuously injected to the grid. LA-55p and LV-25 hall-effect sensors are used to sense the current and voltage, respectively. A DSP controller is used to implement the control technique. Generated pulses are further amplified using TLP250 drivers. All the waveforms are acquired with the help of a YOKOGOWA ScopeCoder. All the experimental results are obtained under similar test conditions as in the simulation analysis. The output voltage waveform with grid current at different *MI* values is shown in Fig. 9(a). At *MI* value > 1, the voltage waveforms get slightly distorted. At *MI* value < 0.5, the grid supply is also reduced to continuously feed power to the grid as the MLI operates at a reduced voltage level. Further tests are conducted at $MI \approx 1$, where a clean voltage output is evident. Fig. 9(b) shows the steady-state results that confirm $V_{inv,}$ is the sum of the output voltage without LBC (V_{oH}) and the output voltage of the LBC (V_{oL}). A 15-level output voltage is produced instead of 7-level by adding V_{oL} at the intermediate levels. The grid voltage and grid currents which are in phase with each other are also shown in the figure. The MLI output voltage and injected grid current harmonic profile are shown in Fig. 9(c) which is following the IEEE-519 standard.

For verify the theoretically calculated blocking voltages, voltage stress across some switches (S_1, S_2, T_1, T_3, L_1, L_3) are shown in Fig. 10(a). It implies the unidirectional nature of

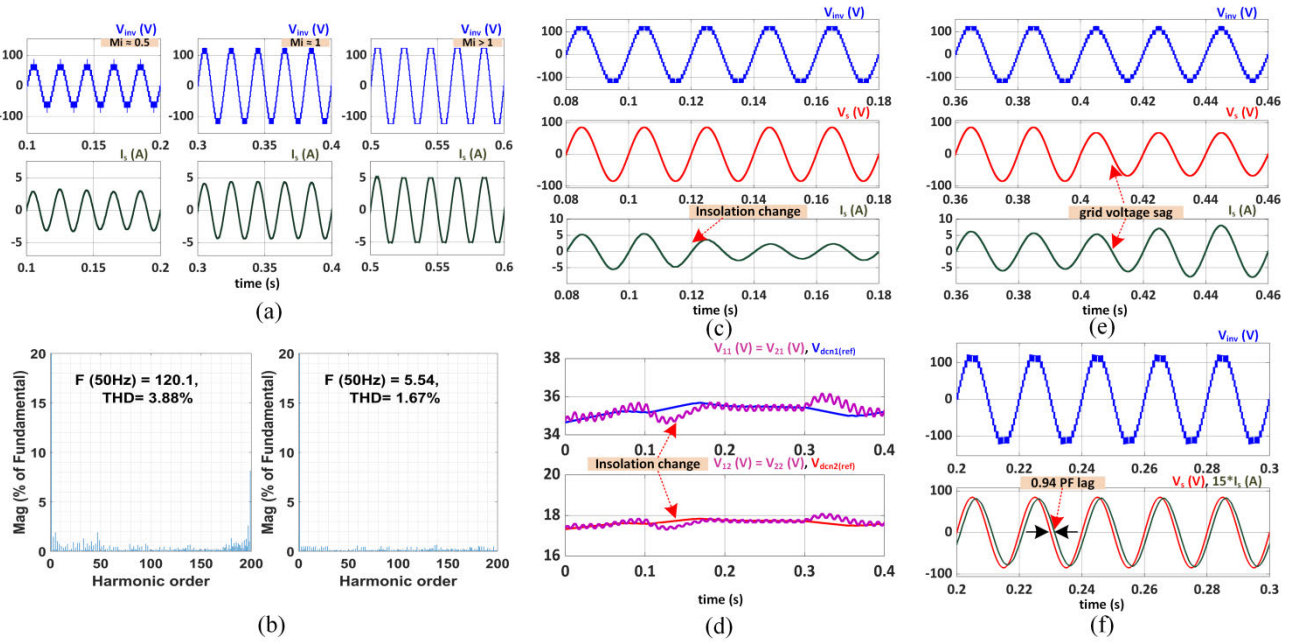

FIGURE 8. Simulation results of the PV fed VLB MLI: (a) V_{inv} & I_s under different *MI* values, (b) Harmonic spectra of V_{inv} & I_s, (c)V_{inv}, V_s, I_s under varying insolation, (d) dc-link voltages, (e) V_{inv}, V_s, I_s under grid voltage sag condition, (f)V_{inv}, V_s, I_s under lagging PF.

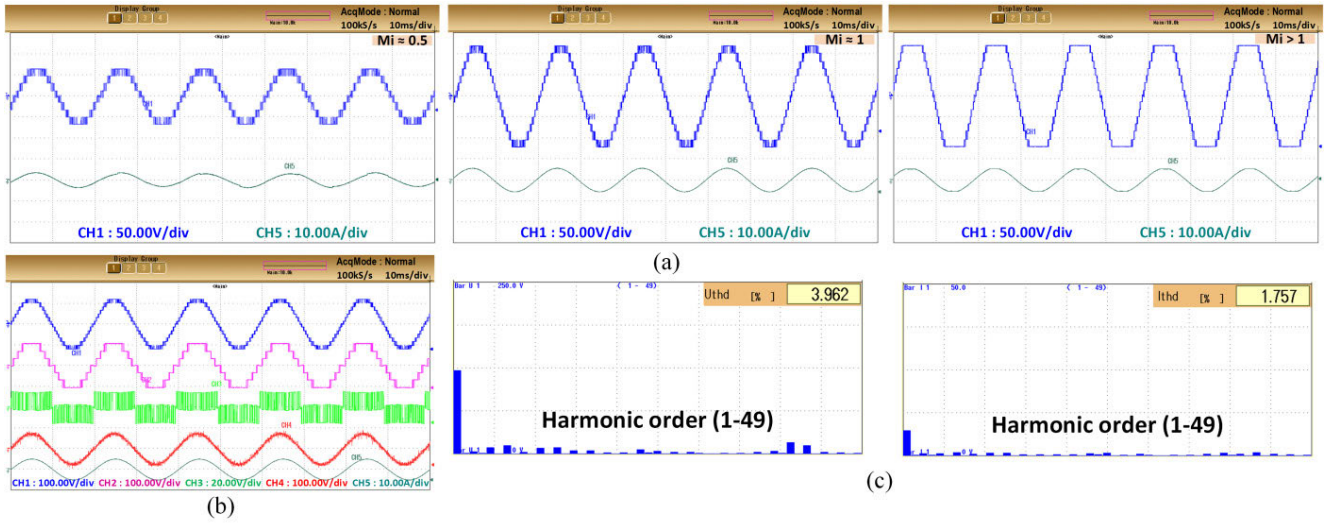

FIGURE 9. Experimental results:(a) V_{inv} & I_s at $MI = 0.5, \approx 1, \& > 1$, (b) Voltages of different stage V_{inv}, V_{oH}, V_{oL}, V_s, & I_s, (c) THD spectra of V_{inv} & I_s.

all the switches. Under dynamic solar insolation change and grid voltage sag condition, results are further acquired. MPP tracking performance is shown in Fig. 10(b) at 750 W/m^2 and 300 W/m^2 insolation levels. These curves show the tracking efficiency is about 99.9% at MPP. In Fig. 10(c), insolation level is changed from 750 W/m^2 to 300 W/m^2. During this, the current grid change is noticeable. The performance under grid voltage sag condition keeping the insolation level fixed is depicted in Fig. 10(d). This causes the minor change in inverter output voltage as the *MI* varies according to the change in grid voltage or dc-link voltage. However, the grid current increases proportionally ensuring the power balance between the grid and PV system.

Moreover, Fig. 11 depicts the grid power, PF, frequency under steady-state, insolation change and voltage sag conditions. Low reactive power attests operation near unity PF in all conditions while the grid frequency is maintained at 50 Hz. Power loss is a crucial factor that dictates the system efficiency, which includes both switching and conduction losses. Switching loss occurs during the state transition of a switch [18]. Although the switching losses are high due to high-frequency PWM switching, the proposed MLI in a way minimizes the switching loss by operating the switches having higher blocking voltage at the fundamental frequency (f_o) and the switches having lower blocking voltage at switching frequency (f_s). For instance, RU and LBC switch

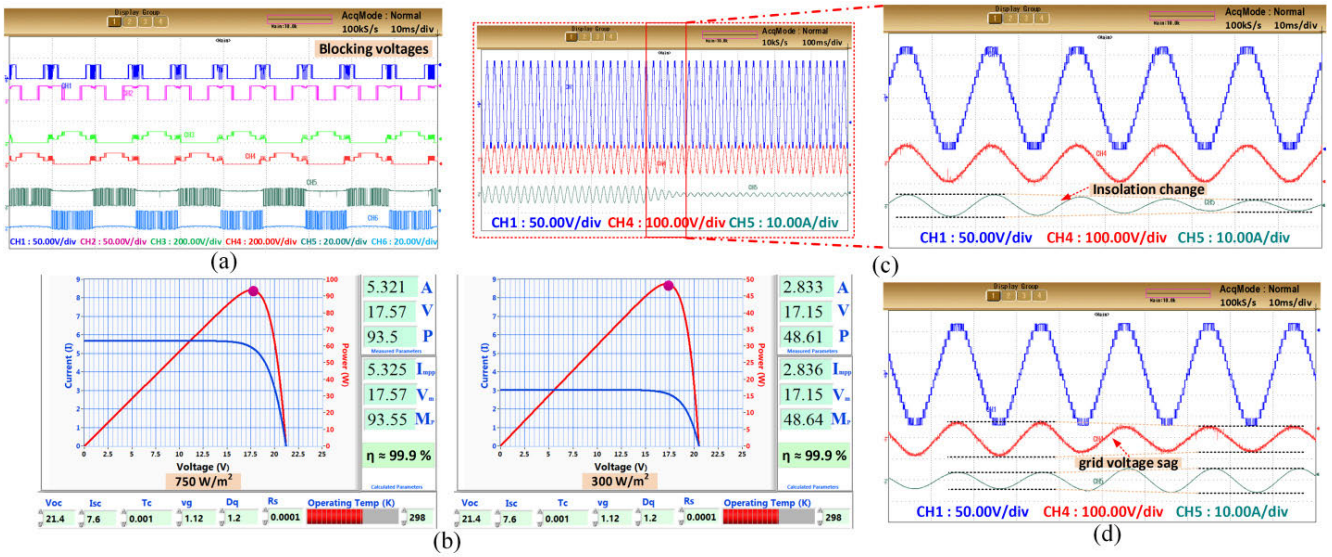

FIGURE 10. Experimental results: (a) Blocking voltages of S_1, S_2, T_1, T_3, L_1, L_3, (b) MPP tracking curves at 750 W/m^2 & 300 W/m^2, (c) V_{inv}, V_s, & I_s under insolation change condition, (d) V_{inv}, V_s, & I_s under grid voltage sag condition.

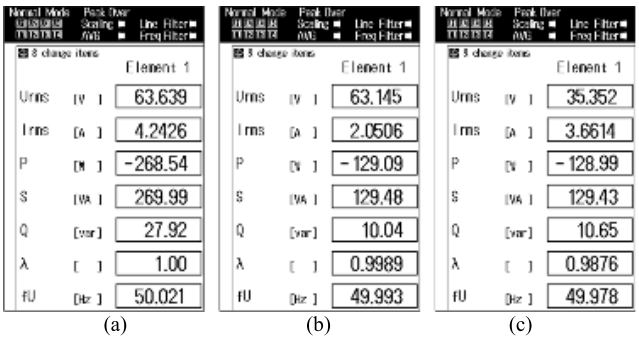

FIGURE 11. Grid power and PF (a) steady-state condition, (b) during insolation change, (c) during voltage sag condition.

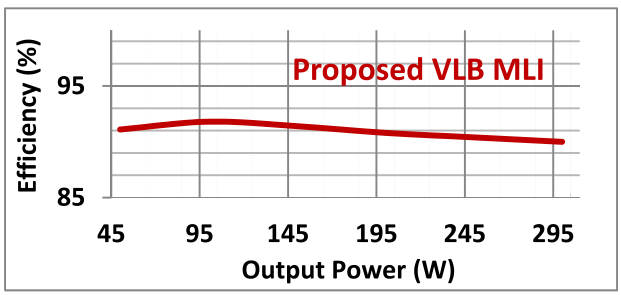

FIGURE 12. Efficiency evaluation of the proposed MLI.

faceless blocking voltage operated at f_s and H-bridge switches withstand a high blocking voltage are operated at f_o. By considering it, switching losses for the proposed VLB MLI is calculated as per Table 1. Further, and conduction loss is also calculated for one complete cycle by considering the number of switches and diodes that conduct during any interval of time. Total power loss is accordingly computed to examine the efficiency of the proposed VLB MLI by neglecting drivers and snubber circuit losses. Fig. 12 illustrates a significantly higher efficiency of VLB MLI interfacing single-stage PV system considering parameters tabulated in Table 3. With the change in insolation level of the PV system, dc-link voltage, grid supply, switching and supply frequencies, efficiency may change.

VII. CONCLUSION

A novel VLB MLI structure introduced in this work along with three different algorithms to choose dc-link magnitude for producing higher voltage steps using the fewer part count. Using two RUs with two different varieties of sources, the proposed MLI generates a 15-level output voltage. In addition to the reduction in the number of switches, both the CLR and TBV are reduced significantly compared to the prior-art MLIs. Low CLR value verifies that the proposed VLB MLI can easily extend to any number of levels with a reduced number of components and lower TBV ($16V_{dc}$ for the 15-level MLI) demonstrates suitability in high-voltage/power applications. The workability of the proposed 15-level MLI is verified in integration with the 1.3 kW PV system. A closed-loop control strategy is developed, which fulfils all the control objectives, and the system operates satisfactorily for any input or output side perturbations. Simulation and experimental analysis under dynamic test cases such as; different *MI* values, under varying insolation, and grid voltage sag condition validates the satisfactory working of the proposed MLI interfacing PV system. The MPP tracking efficiency of the PV system is about 99.9 %, and the overall system efficiency is more than 90%.

REFERENCES

[1] M. di Benedetto, A. Lidozzi, L. Solero, F. Crescimbini, and P. J. Grbovic, "Five-level E-type inverter for grid-connected applications," *IEEE Trans. Ind. Appl.*, vol. 54, no. 5, pp. 5536–5548, Sep. 2018.

[2] J. Munoz, P. Gaisse, C. Baier, M. Rivera, R. Gregor, and P. Zanchetta, "Asymmetric multilevel topology for photovoltaic energy injection to microgrids," in *Proc. IEEE 17th Workshop Control Model. Power Electron. (COMPEL)*, Jun. 2016, pp. 1–6.

[3] S. K. Chattopadhyay and C. Chakraborty, "A new asymmetric multilevel inverter topology suitable for solar PV applications with varying irradiance," *IEEE Trans. Sustain. Energy*, vol. 8, no. 4, pp. 1496–1506, Oct. 2017.

[4] A. Kumar and V. Verma, "Performance enhancement of single-phase grid-connected PV system under partial shading using cascaded multilevel converter," *IEEE Trans. Ind. Appl.*, vol. 54, no. 3, pp. 2665–2676, May 2018.

[5] C. Cecati, F. Ciancetta, and P. Siano, "A multilevel inverter for photovoltaic systems with fuzzy logic control," *IEEE Trans. Ind. Electron.*, vol. 57, no. 12, pp. 4115–4125, 2010.

[6] S. Shuvo, E. Hossain, T. Islam, A. Akib, S. Padmanaban, and M. Z. R. Khan, "Design and hardware implementation considerations of modified multilevel cascaded H-bridge inverter for photovoltaic system," *IEEE Access*, vol. 7, pp. 16504–16524, 2019.

[7] B. Xiao, L. Hang, J. Mei, C. Riley, L. M. Tolbert, and B. Ozpineci, "Modular cascaded H-bridge multilevel PV inverter with distributed MPPT for grid-connected applications," *IEEE Trans. Ind. Appl.*, vol. 51, no. 2, pp. 1722–1731, Mar. 2015.

[8] T. S. Basu and S. Maiti, "A hybrid modular multilevel converter for solar power integration," *IEEE Trans. Ind. Appl.*, vol. 55, no. 5, pp. 5166–5177, Sep. 2019.

[9] S. N and U. R. Yaragatti, "Design and implementation of active neutral-point-clamped nine-level reduced device count inverter: An application to grid integrated renewable energy sources," *IET Power Electron.*, vol. 11, no. 1, pp. 82–91, Jan. 2018.

[10] L. He and C. Cheng, "A Flying-Capacitor-Clamped five-level inverter based on bridge modular switched-capacitor topology," *IEEE Trans. Ind. Electron.*, vol. 63, no. 12, pp. 7814–7822, Dec. 2016.

[11] Y. Han, H. Chen, Z. Li, P. Yang, L. Xu, and J. M. Guerrero, "Stability analysis for the grid-connected single-phase asymmetrical cascaded multilevel inverter with SRF-PI current control under weak grid conditions," *IEEE Trans. Power Electron.*, vol. 34, no. 3, pp. 2052–2069, Mar. 2019.

[12] N. Prabaharan and K. Palanisamy, "A comprehensive review on reduced switch multilevel inverter topologies, modulation techniques and applications," *Renew. Sustain. Energy Rev.*, vol. 76, pp. 1248–1282, Sep. 2017.

[13] V. N. Lal and S. N. Singh, "Control and performance analysis of a single-stage utility-scale grid-connected PV system," *IEEE Syst. J.*, vol. 11, no. 3, pp. 1601–1611, Sep. 2017.

[14] E. Villanueva, P. Correa, J. Rodriguez, and M. Pacas, "Control of a single-phase cascaded H-Bridge multilevel inverter for grid-connected photovoltaic systems," *IEEE Trans. Ind. Electron.*, vol. 56, no. 11, pp. 4399–4406, Nov. 2009.

[15] Y. Liu, B. Ge, H. Abu-Rub, and F. Z. Peng, "An effective control method for Quasi-Z-Source cascade multilevel inverter-based grid-tie single-phase photovoltaic power system," *IEEE Trans. Ind. Informat.*, vol. 10, no. 1, pp. 399–407, Feb. 2014.

[16] P. R. Bana, K. P. Panda, R. T. Naayagi, P. Siano, and G. Panda, "Recently developed reduced switch multilevel inverter for renewable energy integration and drives application: Topologies, comprehensive analysis and comparative evaluation," *IEEE Access*, vol. 7, pp. 54888–54909, 2019.

[17] A. I. M. Ali, E. E. M. Mohamed, M. A. Sayed, and M. S. R. Saeed, "Novel single-phase nine-level PWM inverter for grid connected solar PV farms," in *Proc. Int. Conf. Innov. Trends Comput. Eng. (ITCE)*, Aswan, Egypt, Feb. 2018, pp. 345–440.

[18] K. P. Panda, S. S. Lee, and G. Panda, "Reduced switch cascaded multilevel inverter with new selective harmonic elimination control for standalone renewable energy system," *IEEE Trans. Ind. Appl.*, vol. 55, no. 6, pp. 7561–7574, Nov. 2019.

[19] N. A. Rahim and J. Selvaraj, "Multistring five-level inverter with novel PWM control scheme for PV application," *IEEE Trans. Ind. Electron.*, vol. 57, no. 6, pp. 2111–2123, Jun. 2010.

[20] S. Jain and V. Sonti, "A highly efficient and reliable inverter configuration based cascaded multilevel inverter for PV systems," *IEEE Trans. Ind. Electron.*, vol. 64, no. 4, pp. 2865–2875, Apr. 2017.

[21] J. C. Kartick, K. Suparna, and B. K. Sujit, "Dual reference phase shifted pulse width modulation technique for a N-level inverter based grid connected solar photovoltaic system," *IET Renew. Power Gener.*, vol. 10, no. 7, pp. 928–935, Aug. 2016.

[22] R. Raushan, B. Mahato, and K. C. Jana, "Comprehensive analysis of a novel three-phase multilevel inverter with minimum number of switches," *IET Power Electron.*, vol. 9, no. 8, pp. 1600–1607, Jun. 2016.

[23] A. Hota, S. Jain, and V. Agarwal, "An optimized three-phase multilevel inverter topology with separate level and phase sequence generation part," *IEEE Trans. Power Electron.*, vol. 32, no. 10, pp. 7414–7418, Oct. 2017.

[24] R. S. Alishah, D. Nazarpour, M. Sabahi, and S. H. Hosseini, "New hybrid structure for multilevel inverter with fewer number of components for high-voltage levels," *IET Power Electron.*, vol. 7, no. 1, pp. 96–104, Jan. 2014.

[25] K. P. Panda and G. Panda, "Application of swarm optimisation-based modified algorithm for selective harmonic elimination in reduced switch count multilevel inverter," *IET Power Electron.*, vol. 11, no. 8, pp. 1472–1482, Jul. 2018.

[26] X. Sun, B. Wang, Y. Zhou, W. Wang, H. Du, and Z. Lu, "A single DC source cascaded seven-level inverter integrating switched-capacitor techniques," *IEEE Trans. Ind. Electron.*, vol. 63, no. 11, pp. 7184–7194, Nov. 2016.

[27] R. M. Sekar, D. Nelson Jayakumar, K. Mylsamy, U. Subramaniam, and S. Padmanaban, "Single phase nine level inverter using single DC source supported by capacitor voltage balancing algorithm," *IET Power Electron.*, vol. 11, no. 14, pp. 2319–2329, Nov. 2018.

[28] Y. Ye, K. W. E. Cheng, J. Liu, and K. Ding, "A step-up switched-capacitor multilevel inverter with self-voltage balancing," *IEEE Trans. Ind. Electron.*, vol. 61, no. 12, pp. 6672–6680, Dec. 2014.

[29] M. Khenar, A. Taghvaie, J. Adabi, and M. Rezanejad, "Multi-level inverter with combined T-type and cross-connected modules," *IET Power Electron.*, vol. 11, no. 8, pp. 1407–1415, Jul. 2018.

[30] H. K. Jahan, M. Abapour, K. Zare, S. H. Hosseini, F. Blaabjerg, and Y. Yang, "A multilevel inverter with minimized components featuring self-balancing and boosting capabilities for PV applications," *IEEE J. Emerg. Sel. Topics Power Electron.*, early access, Jun. 12, 2019, doi: 10.1109/JESTPE.2019.2922415.

[31] P. Panda, P. R. Bana, and G. Panda, "A switched-capacitor self-balanced high-gain multilevel inverter employing a single DC source," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, early access, Feb. 20, 2020, doi: 10.1109/TCSII.2020.2975299.

[32] H. Vahedi, M. Sharifzadeh, and K. Al-Haddad, "Modified seven-level pack U-Cell inverter for photovoltaic applications," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 6, no. 3, pp. 1508–1516, Sep. 2018.

[33] V. Rajesh, S. K. Chattopadhyay, and C. Chakraborty, "Full bridge level doubling network assisted multilevel DC link inverter," in *Proc. IEEE 7th Power India Int. Conf. (PIICON)*, Nov. 2016, pp. 1–6.

[34] N. Prabaharan and K. Palanisamy, "Analysis of cascaded H-bridge multilevel inverter configuration with double level circuit," *IET Power Electron.*, vol. 10, no. 9, pp. 1023–1033, Jul. 2017.

[35] P. R. Bana, K. P. Panda, and G. Panda, "Power quality performance evaluation of multilevel inverter with reduced switching devices and minimum standing voltage," *IEEE Trans. Ind. Informat.*, early access, Nov. 12, 2019, doi: 10.1109/TII.2019.2953071.

[36] E. Samadaei, M. Kaviani, and K. Bertilsson, "A 13-levels module (K-type) with two DC sources for multilevel inverters," *IEEE Trans. Ind. Electron.*, vol. 66, no. 7, pp. 5186–5196, Jul. 2019.

[37] S. S. Lee, M. Sidorov, N. R. N. Idris, and Y. E. Heng, "A symmetrical cascaded compact-module multilevel inverter (CCM-MLI) with pulsewidth modulation," *IEEE Trans. Ind. Electron.*, vol. 65, no. 6, pp. 4631–4639, Jun. 2018.

[38] Y. Hinago and H. Koizumi, "A switched-capacitor inverter using Series/Parallel conversion with inductive load," *IEEE Trans. Ind. Electron.*, vol. 59, no. 2, pp. 878–887, Feb. 2012.

[39] Pathy, Subramani, Sridhar, T. Thentral, and Padmanaban, "Nature-inspired MPPT algorithms for partially shaded PV systems: A comparative study," *Energies*, vol. 12, no. 8, p. 1451, 2019.

[40] P. Sen, P. R. Bana, and K. P. Panda, "Firefly assisted genetic algorithm for selective harmonic elimination in PV interfacing reduced switch multilevel inverter," *Int. J. Renew. Energy Res.*, vol. 9, no. 1, pp. 32–43, Mar. 2019.

PRABHAT RANJAN BANA (Graduate Student Member, IEEE) received the B.Tech. degree in electrical engineering from the Parala Maharaja Engineering College, Berhampur, India, in 2016, and the M.Tech. degree in power and energy systems specialization from the National Institute of Technology at Meghalaya, Shillong, India, in 2019. He is currently a Research Fellow of the Department of Electrical Engineering, National Institute of Technology at Meghalaya. His research interests include multilevel inverters, photovoltaic systems, and power quality.

KAIBALYA PRASAD PANDA (Graduate Student Member, IEEE) received the B.Tech. degree in electrical and electronics engineering from Dr. M. G. R. University, Chennai, India, in 2011, and the M.Tech. degree in power electronics and drives specialization from the KIIT University, Bhubaneswar, India, in 2013. He is currently pursuing the Ph.D. degree with the Department of Electrical Engineering, National Institute of Technology at Meghalaya, Shillong, India.

From 2013 to 2017, he was an Assistant Professor with the Department of Electrical Engineering, C. V. Raman College of Engineering, Bhubaneswar. He was a Visiting Scholar with the University of Warwick, U.K., from January to March 2019, funded through the Joint U.K.–India Clean Energy (JUICE) two months exchange program scheme. He was a recipient of the Prof. Subhasis Nandi Student Travel Award from the Power Electronics, Drives, and Energy Systems (PEDES) Conference, in 2018. He has received the IAS Travel Grant from the Power Electronics, Smart Grid, and Renewable Energy (PESGRE) Conference. He is a regular Reviewer of several IEEE and IET journals.

SANJEEVIKUMAR PADMANABAN (Senior Member, IEEE) received the bachelor's degree in electrical engineering from the University of Madras, Chennai, India, in 2002, the master's degree (Hons.) in electrical engineering from Pondicherry University, Puducherry, India, in 2006, and the Ph.D. degree in electrical engineering from the University of Bologna, Bologna, Italy, in 2012.

He was an Associate Professor with VIT University, from 2012 to 2013. In 2013, he joined the National Institute of Technology at Meghalaya, India, as a Faculty Member. In 2014, he was invited as a Visiting Researcher at the Department of Electrical Engineering, Qatar University, Doha, Qatar, funded by the Qatar National Research Foundation (Government of Qatar). Furthermore, he continued his research activities with the Dublin Institute of Technology, Dublin, Ireland, in 2014. He was an Associate Professor with the Department of Electrical and Electronics Engineering, University of Johannesburg, Johannesburg, South Africa, from 2016 to 2018. Since 2018, he has been a Faculty Member of the Department of Energy Technology, Aalborg University, Aalborg, Denmark. He has authored more than 300 scientific articles.

Dr. Padmanaban is a Fellow of the Institution of Engineers, India, the Institution of Electronics and Telecommunication Engineers, India, and the Institution of Engineering and Technology, U.K. He was the recipient of the Best Paper cum Most Excellence Research Paper Award from IET-SEISCON 2013, IET-CEAT 2016, the IEEE-EECSI 2019, and the IEEE-CENCON 2019, and five best paper awards from ETAEERE 2016 for *Lecture Notes in Electrical Engineering* (Springer). He is an Editor/Associate Editor/Editorial Board Member of refereed journals, in particular the IEEE Systems Journal, IEEE Access, *IET Power Electronics*, and the IEEE Transaction on Industry Applications, *IET Power Electronics* and the *International Journal of Electrical Energy Systems, Wiley Publications*, and the Subject Editor and the Subject Editor of the *IET Renewable Power Generation*, *IET Generation, Transmission and Distribution*, and FACTS journal (Canada).

LUCIAN MIHET-POPA (Senior Member, IEEE) was born in 1969. He received the bachelor's degree in electrical engineering, the master's degree in electric drives and power electronics, and the Ph.D. and Habilitation degrees in electrical engineering from the Politehnica University of Timisoara, Romania, in 1999, 2000, 2003, and 2015, respectively.

From 1999 to 2016, he was with the Politehnica University of Timisoara, Romania. He was also working as a Research Scientist with Aalborg University, Denmark, in 2002, Siegen University, Germany, in 2004, and Danish Technical University, from 2011 to 2014. He is also the Head of the Research Lab, Intelligent Control of Energy Conversion and Storage Systems, and one of the Coordinators of the Master's degree Program in Green Energy Technology. Since 2016, he has been working as a Full Professor in energy technology with Østfold University College, Norway. He has published more than 120 articles in national and international journals and conference proceedings, and ten books. He was supported by more than 15 international grants/projects, such as FP7, EEA and Horizon, and more than ten national research grants as well. His research interests include modeling, simulation, control, and testing of energy conversion systems, and distributed energy resource (DER) components and systems, including battery storage systems (BSS) [for electric vehicles and hybrid cars and Vanadium redox batteries (VRB) as well] and energy efficiency in smart buildings and smart grids.

Dr. Mihet-Popa has served as a scientific and technical programme committee member of many IEEE conferences. His paper published by the IEEE IAS Transactions on Industry Applications (2004) entitled Wind Turbine Generator Modeling and Simulation Where Rotational Speed is the Controlled Variable received the 2005 Second Prize Paper Award. Since 2017, he has been a Guest Editor of five special issues for *Energy* and *Applied Sciences* (MDPI) journals, MAJLESI, and *Advances in Meteorology* journal.

GAYADHAR PANDA (Senior Member, IEEE) received the bachelor's degree in electrical engineering from the Institute of Engineers, Kolkata, India, in 1996, the master's degree in power electronics from the Bengal College of Engineering and Technology (presently IIEST), Shibpur, India, in 1998, and the Ph.D. degree in electrical engineering from Utkal University, Bhubaneswar, India, in 2007.

He is currently a Professor with the Department of Electrical Engineering, National Institute of Technology (NIT) at Meghalaya, India. He has served as the head of the department and the chairman of various committees at the institute level. He is currently looking after the Dean Academic Affairs (AA) with NIT at Meghalaya. He has more than 20 years of teaching experience. His current research interests include automatic generation control, stability improvements using flexible alternating current transmission system devices, power quality, power electronic converters, and distributed power generation.

JIANZHONG WU (Member, IEEE) received the B.S., M.S., and Ph.D. degrees in electrical engineering from Tianjin University, China, in 1999, 2002, and 2004, respectively.

From 2004 to 2006, he held a postdoctoral position at Tianjin University. From 2006 to 2008, he was a Research Fellow of The University of Manchester, U.K. He was with Cardiff University, as a Lecturer, in 2008, a Senior Lecturer, in 2013, a Reader, in 2014, and a Professor, in 2015. He is currently a Professor of multivector energy systems and the Head of the Department of Electrical and Electronics Engineering, Cardiff University, U.K. His research interests include energy infrastructure and smart grids.

Prof. Wu is also the Director of the Applied Energy UNiLAB on Synergies Between Energy Networks. He is also the Co-Director of EPSRC Supergen Energy Networks Hub and the U.K. Energy Research Centre. He is also a Subject Editor of *Applied Energy*.