Closed-Loop Electroosmotic Microchannel Cooling System for VLSI Circuits

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***Abstract*—The increasing heat generation rates in VLSI circuits motivate research on compact cooling technologies with low thermal resistance. This paper develops a closed-loop two-phase microchannel cooling system using electroosmotic pumping for the working fluid. The design, fabrication, and open-loop performance of the heat exchanger and pump are summarized. The silicon heat exchanger, which attaches to the test chip (1 cm^2), achieves junction-fluid resistance near 0.1 K/W using 40 plasma-etched channels with hydraulic diameter of 100 μm. The electroosmotic pump, made of an ultrafine porous glass frit with working volume of 1.4 cm^3, achieves maximum backpressure and flowrate of 160 KPa and 7 ml/min, respectively, using 1 mM buffered de-ionized water as working fluid. The closed-loop system removes 38 W with pump power of 2 W and junction-ambient thermal resistance near 2.5 K/W. Further research is expected to strongly reduce the thermal resistance for a given heating power by optimizing the saturation temperature, increasing the pump flowrate, eliminating the thermal grease, and optimizing the heat exchanger dimensions.**

***Index Terms*—Electroosmotic pump, IC cooling technology, microchannel heat exchanger, two-phase heat transfer.**

I. Introduction

ACCORDING to the International Roadmap for Semiconductors [1], microprocessors will generate more than 200 W by the year 2005. During this period, the industry is also facing major challenges in multi-chip integration, such that reducing the chip-backside volume occupied by any cooling solution is a major objective. Conventional macroscopic air-convection fin-array heat sinks are not practical for these levels of heat generation and integration. Moreover, conventional technology is not well suited for solving the problem of highly localized on-chip hotspots, which are resulted from extreme heat generation within confined regions.

These developments are motivating research on novel cooling technology. Conventional heat pipes and vapor chambers have been attractive for microprocessor cooling because they do not require an external electrical power supply and the working fluid is contained within a closed chamber [2], [3]. However, these capillary-driven devices are not optimal for chip powers exceeding a few tens of Watts because of the associated increases in heat pipe cross-sectional area and the limitations in the wick thickness. Recent research on fully-micromachined capillary-driven loops in silicon promises to improve heat spreading within the chip. This approach addresses the hotspot problem, but does not solve the problem of heat removal to the environment [4]. Droplet impingement cooling loops, using piezoelectric atomization, for example, [5], are a promising replacement to conventional aluminum heat sink technology. However, this technology, like heat pipes, is not optimal because it requires substantial volume at the chip backside. Thermoelectric devices are attractive for refrigeration because they may eventually be integrated with VLSI technology. Recent research has generated new classes of superlattice materials with improved figures of merit for thermoelectric cooling [6]. However, solid-state refrigeration augments the overall heating rate and necessitates aggressive fluidic cooling at the heat rejecter junction.

Forced liquid and liquid-vapor convection in microchannel heat sinks have received attention since the original liquid convection research by Tuckerman and Pease, which removed 790 W from a 1 cm^2 silicon chip [7]. The major attraction of microchannels is the extremely low volume required at the chip backside, which facilitates multichip integration. While droplet impingement cooling can achieve lower value of thermal resistance under an optimal liquid film thickness, microchannels achieve an impressively low resistance at a fraction of the occupation volume. The past work indicates that the fundamental physics of boiling convection in microchannels requires additional study, particularly for channels of dimensions below 50 μm. Bowers and Mudawar [8] reported that microchannels with a hydraulic diameter of 510 μm yielded 28% higher critical heat flux (CHF) than minichannels with a hydraulic diameter of 2.45 mm using the same water flowrate of 64 ml/min. Peng *et al.* [9] suggested that nucleate boiling was intensified in microchannels with dimensions of 600 μm$\times$ 700 μm. Stanley *et al.* [10] conducted two-phase flow experiments in rectangular channels with hydraulic diameters between 56 μm and 256 μm. They proposed a homogeneous flow model based on the pressure drop and conductance data. Jiang *et al.* [11], [12] developed silicon microchannel heat sinks with integrated heater and temperature sensors. The test structures captured both temperature distributions and two-phase flow patterns in microchannels with triangular cross sections and hydraulic diameters between 40 and 80 μm. The results suggest that nucleation boiling is

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suppressed in the microchannels. Zhang *et al.* [13] fabricated single-microchannel structures with integrated doped-silicon heaters and thermometers. The channel hydraulic diameters are between 25 and 60 μm and the design achieved relatively uniform heat flux boundary conditions. Numerical modeling of the two-phase microchannel flow has also been conducted. Peles *et al.* [14] developed a one-dimensional flow model with a distinct liquid-vapor evaporation front. They claimed, with the support of experiments, that evaporating two-phase flow in microchannels has a time-average mass quality lower than one at the exit and thus is unsteady. Koo *et al.* [15] presented a modeling approach to simulate two-phase microchannel heat exchanger performance. They predicted a multichannel heat exchanger with the channel hydraulic diameter of 170 μm can dissipate 200 W from a 25 mm $\times$ 25 mm chip with a water flowrate of 15 ml/min and chip temperature rise of 40 K.

For space-critical desktop and portable applications, a practical self-contained cooling system must be implemented in a closed loop with a pump which is compact, highly reliable, and efficient. Research on the development of miniaturized pumps is active and various membrane pumps and field-driven flow pumps have been designed and demonstrated [16], [17]. Membrane pumps, using a micromachined deflectable membrane and one or more valves to generate a pumping action, typically employ electrostatic, thermopneumatic, bimetallic, shape-memory alloy, or piezoelectric actuation. Stemme *et al.* [18] reported a membrane pump with a maximum water flowrate up to 16 ml/min and maximum backpressure of 2 kPa. Zengerle *et al.* [19] presented a pump with a maximum backpressure up to 35 kPa and maximum water flowrate of 0.8 ml/min. These pumps have the advantage of being capable of pumping a wide variety of working fluids. However, the dependence on solid moving parts poses fabrication challenges and may have limited reliability. Electroosmotic, electromagnetic, magnetic, and acoustic effects have been used to induce microscale fluid flow in systems that require no moveable parts [20]–[23]. Electroosmotic pumps, using electroosmosis to propel the liquid, have received much recent attention because of the potential of achieving both high pressure and large flowrate. Paul *et al.* [24] demonstrated packed capillary electroosmotic pumps, which provids a maximum backpressure of 40 000 KPa and a maximum flowrate of 0.045 μl/min at 1.5 kV applied voltage using 1 mM buffered water. Chen *et al.* [25] developed a planar electroosmotic pump by etching a wide and shallow channel in glass. This planar pump generats a maximum backpressure of 150 kPa and a maximum water flowrate of 2.5 μl/min at 3 kV. Zeng *et al.* [26] fabricated an electroosmotic pump using packed silica particles. The capillary pump provides a maximum pressure of 2000 kPa and a maximum water flowrate of 3.6 μl/min at 2 kV. Although simple to fabricate, packed capillary and planar pumps are not yet well suited for VLSI cooling applications which require both water flowrate of about 20 ml/min and pressure of about 100 kPa to remove 200 W. Recently, Yao *et al.* [27] developed electroosmotic pumps with large flowrate for VLSI cooling appliactions. The pumps were fabricated using modified commercially available sintered-glass frits with an active volume of 1.4 cm^3. The prototype pumps demonstrated a maximum flowrate of 7 ml/min and a maximum pressure of 250 KPa at 200 V with 1 mM buffered water. Further progress is anticipated on increasing the flowrate, reducing the operating voltage and working volume, and developing alternative dielectric working liquids.

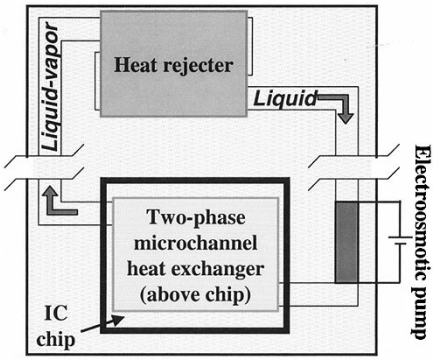

Fig. 1. Conceptual schematic of the proposed electroosmotic cooler. The cooler is comprised of three main components: electroosmotic pump, microchannel heat exchanger and heat rejecter.

This manuscript presents the design and characterization of a closed-loop cooling system using two-phase microchannel heat sink and electroosmotic pumping for applications in VLSI chips cooling.

II. Overall System Description

A conceptual schematic of the cooling system is shown in Fig. 1. The system consists of an electroosmotic pump, a microchannel heat exchanger and a heat rejecter. The working principle of the electroosmotic pump is based on electroosmosis through an ultra-fine porous glass filter. The silanol groups on the glass surface deprotonate while in contact with an electrolyte and form an electric double layer. As an external electric field is applied through the structure, electroosmotic flow develops within the pores. The electroosmotic pumping of the liquid at desired flow rates and pressures is achieved using an electric field. The microchannel heat exchanger is fabricated using plasma etching in a silicon die. The silicon micromachined heat exchanger provides Si-Si compatibility and facilitates multi-chip integration. It also offers a lower thermal resistance by taking advantage of elimination of a thermal interface between the heat exchanger and the IC chip. Two-phase forced convection is performed to utilize fluid latent heat and to achieve more uniform temperature distribution on the IC chip. The heat rejecter is a combination of an aluminum fin array heat sink with embedded flow channels and a fan. It is placed at the down stream of the two-phase heat exchanger to condense the two-phase fluid back to liquid state, and to further lower the liquid temperature to a proper temperature for the pump. The cooled liquid is then pumped back into the heat exchanger, thus forming a closed-loop flow system.

The system developed here is the first hermetically-sealed microchannel cooling system based on electroosmotic pumping. The micro heat exchanger and electroosmotic pump are extremely compact, and the system can be integrated in a modular fashion with the semiconductor chip (heat source). The entire volume of the whole system is far smaller than that of a heat pipe, a vapor chamber, and a fin-array heat sink capable of removing comparable power from the chip.

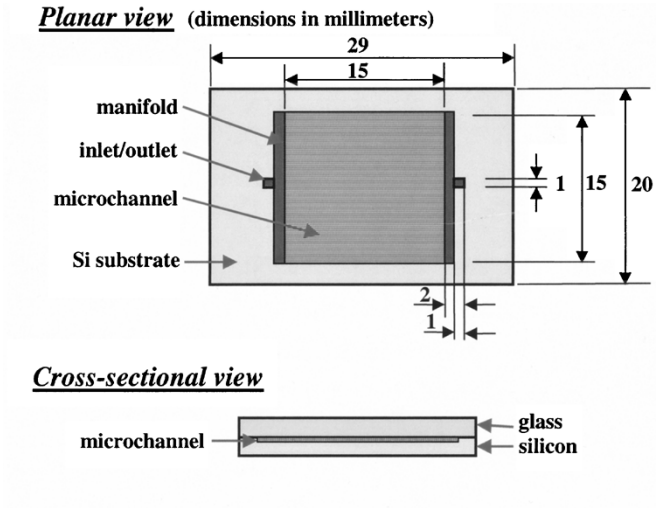

Table of Dimensions

Structure	Dimension
Heat exchanger	20 mm × 29 mm × 500 μm (width × length × thickness)
Channel geometry	100 μm × 100 μm × 15 mm (width × depth × length)
No. of channels	40 (with pitch of 350μm)
Inlet/outlet manifold	1mm × 100 μm × 1 mm (width × depth × length)

Fig. 2. Schematic and a table of dimensions of the heat exchanger.

The system active control ability, through the fast-response field-driven electroosmotic pump, also allows on-demand cooling for hotspots.

III. Microchannel Heat Exchanger

The design of a microchannel heat exchanger aims to achieve the lowest possible thermal resistance with a reasonable pressure drop for a specified range of heat generation and liquid flowrate. The microchannel heat exchanger consists of a numbers of multichannels with shared inlet and outlet manifolds. The optimal design of the heat exchanger is obtained by predicting the performance of a given size heat exchanger while adjusting geometries and numbers of the microchannels. Fig. 2 shows the schematic and dimensions of a heat exchanger capable of dissipating 100 W from a 1 cm × 1 cm thermal chip with a pressure drop of about 160 kPa. The heat exchanger, with 40 microchannels of 100 μm hydraulic diameters, is predicted to be able to achieve a junction-fluid thermal resistance of less than 0.1 K/W.

The heat exchanger is fabricated using deep reactive ion etching (DRIE) in a standard 550 μm thick $\langle 100 \rangle$ silicon substrate. The microchannels are then sealed using anodic bonding of the silicon die to a piece of 500 μm thick Pyrex 7740 glass (Corning). Two pre-drilled holes in the glass, aligned respectively with the inlet and outlet manifolds of the microchannels in the silicon die, serve as taps for the working fluid. Fig. 3 is an image of a fabricated microchannel heat exchanger.

The heat exchanger is characterized for open-loop operation (the outlet pressure of the heat exchanger is ambient pressure) using a commercial pump with room temperature de-ionized

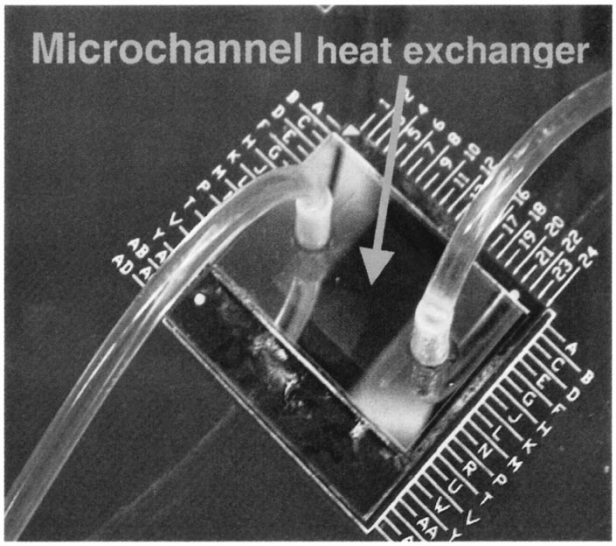

Fig. 3. Photograph of the microchannel heat exchanger.

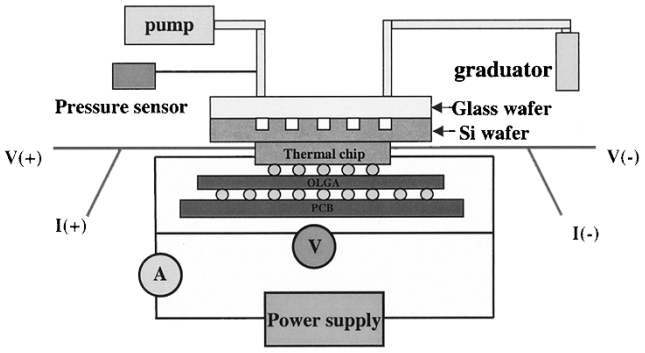

Fig. 4. Schematic of the experimental apparatus for characterization of the microchannel heat exchanger.

water as the working fluid [28]. Fig. 4 shows the schematic of the experimental setup. A 1 cm × 1 cm silicon thermal test chip is fabricated with integrated heaters and temperature sensors. The thermal chip provides uniform heating up to 100 W. The chip temperature for a given input power is obtained from an integrated temperature sensor located at the center of the thermal chip die. The microchannel heat exchanger is attached to the thermal chip using thermal grease with a thermal conductivity near 1.1 $Wm^{-1}K^{-1}$. A gauge pressure transducer measures the pressure drop across the heat exchanger, and a volumetric graduator is placed at the exit of the heat exchanger for volumetric flowrate measurements.

All experiments were conducted under steady-state conditions, and the data were taken after the steady states were reached. Uncertainty estimates in the experimental quantities were calculated using the ANSI/ASME Standard [29], and determined to be 0.1 °C in chip temperature, 3.2% in chip power, 1% in microchannel heat exchanger temperatures, 1% in water volumetric flow rate and 0.25% in pressure. The uncertainty in junction-to-fluid thermal resistance was less than 3.4%. All uncertainty estimates were made assuming a 1% error in thermodynamic properties and 3% error in transport properties.

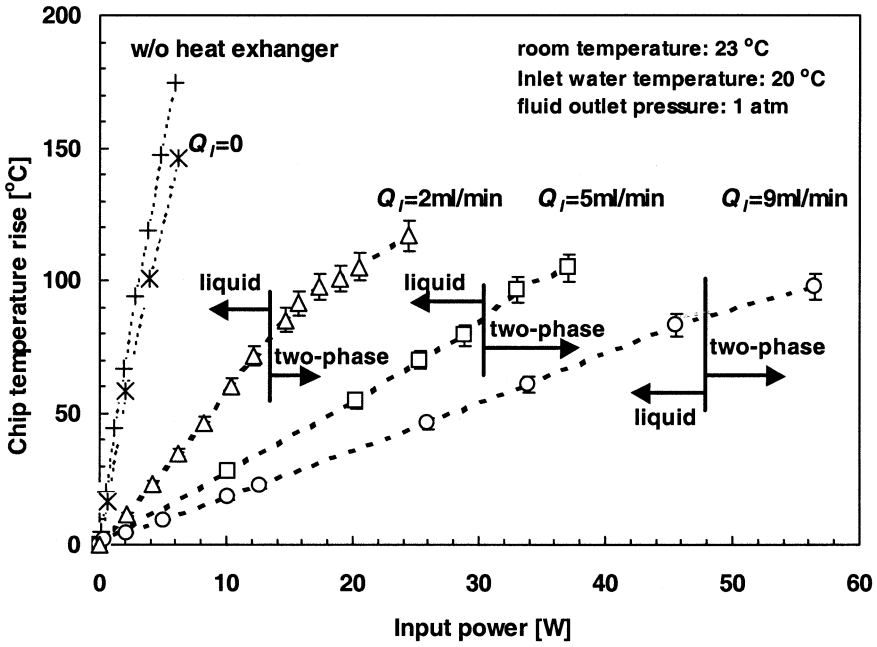

Fig. 5. Measured dependence of the average chip temperature on the input power (vertical bars indicate temeparture flunctuations). Ambient temperature and water inlet temperature were held constant in all experiments.

Fig. 5 shows the dependence of chip temperature rise (ambient temperature as reference temperature) on heater input power under various flowrate conditions. The curves represent the results for the cases:

1) in the absence of the heat exchanger;
2) heat exchanger as a spreader without forced convection;
3) under forced convections.

Both case 1) and case 2) result a steep increase in chip temperature within a small increase in input power, with an estimated junction-to-ambient thermal resistance of more than 25 K/W. The chip temperature decreases when water flows through the channels. A linear increase in chip temperature with increasing input power is observed when the fluid is purely in the liquid phase, for liquid flowrates, Q_l, of 2, 5, and 9 ml/min. The results indicate that the junction-to-ambient thermal resistance can be reduced greatly using forced convection in microchannels, and can be further reduced by increasing the flowrate. A further decrease in slope of the temperature versus input power curves is observed when two-phase flow develops in the microchannels. The junction-to-ambient thermal resistance was determined to be less than 1.5 K/W and the junction-to-fluid thermal resistance is estimated to be less than 0.1 K/W under two-phase convection with a inlet water flowrate of 9 ml/min. No temperature fluctuations were observed when flow is under single-phase conditions. Temperature fluctuations of $\pm 0.2\%$ were recorded when flow is under two-phase conditions, as indicated in Fig. 5.

The corresponding dependence of pressure drop on input power is illustrated in Fig. 6. When the flow is under liquid convection conditions, the pressure drop decreases with the increasing power since the viscosity of water decreases with the increasing temperature. At the onset of two-phase flow with lower fluid qualities, the pressure drop increases rapidly mainly because of the rapidly increased fluid kinetic viscosity. The two-phase flow pressure continuously increases with the

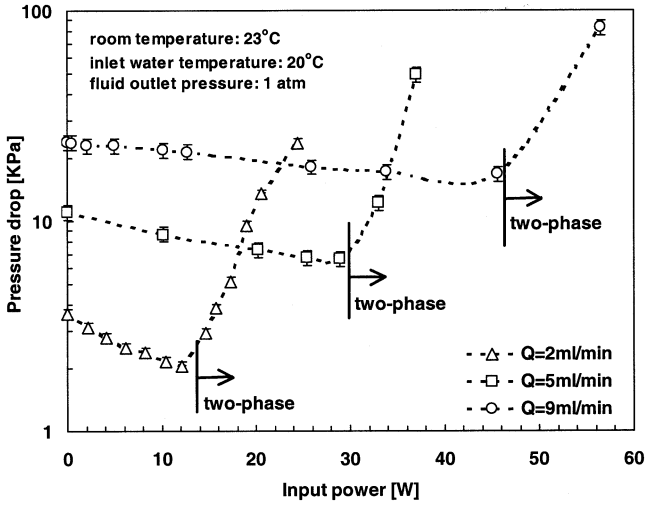

Fig. 6. Dependence of heat exchanger pressure drop on input power (vertical bars indicate pressure flunctuations). Ambient temperature and water inlet temperature were held constant in all experiments.

increasing input power because of the increasing two-phase fluid quality. The further increase in fluid quality leads to pressure drop increase from both friction and vapor acceleration. The flow inlet pressure reaches $30 \sim 80$ KPa higher than the ambient pressure for the highest testing powers, depending on the flowrates. Consequently, the fluid saturation temperature is predicted about $10 \sim 20\,^{\circ}\mathrm{C}$ higher than water boiling temperature at ambient pressure, 100 °C. This explains the higher chip temperatures after the onset of boiling in Fig. 5, owing to both junction-fluid thermal resistance and the interface material thermal resistance. Fig. 6 also demonstrates that the pressure drop under two-phase flow conditions is several to ten times higher than that under single-liquid-phase conditions even the two-phase fluid quality is estimated below 0.2. Pressure

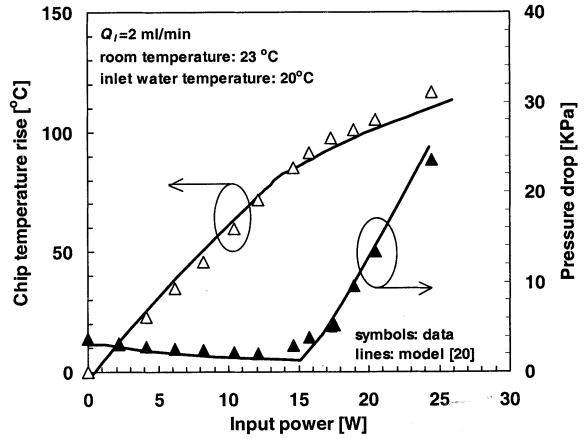

Fig. 7. Comparison between predictions and experimental data for the chip temperature rise and heat exchanger pressure drop as functions of the input power.

fluctuations are observed to be $\pm 1\%$ and $\pm 2\%$ when flow is under single-phase conditions and two-phase conditions, respectively.

The two-phase flow is visualized during the entire period of each experiment. Boiling starts at the downstream manifold of the channels and moves upstream along the microchannels with the increasing power. A distinct interface between the upstream liquid flow and downstream two-phase flow is observed and the two-phase flow is relatively uniform among the microchannels under present uniform heating condition. A typical annular flow is seen in two-phase flow regime, i.e., a moving thin liquid film covers the channel walls with a vapor core accelerating in the center of the channel. The flow in the two-phase regime is dynamic and the annular flow mode is observed stable, corresponding to the steady temperature and pressure measurements. However, larger fluctuations in both temperature and pressure measurements are initiated while the front of the two-phase regime reaches the inlet manifold at certain high powers. The front oscillates along the channels, resulting in a periodic temperature fluctuation up to $\pm 10\%$ and a pressure fluctuation $\pm 50\%$, depending on the flowrates. Optimizations of both microchannel heat exchanger configuration and its operating conditions are suggested to stabilize the two-phase flow for steady temperature and pressure performance.

Numerical simulations are conducted to calculate the channel wall temperature and heat exchanger pressure drop using a two-phase heat transfer model. The model solves steady-state energy equations for heat conduction in the solid walls and for convection by the fluid in microchannels, with boundary conditions dictated by the heat loss to the environment [15]. The simulation uses finite volume method and considers temperature and pressure dependence of the fluid properties. Thermal resistance of the interface material is considered when comparing the predicted channel wall temperature with the measured chip temperature. A constant thermal resistance of 1.2 K/W is used assuming that the thickness of the thermal grease layer is about 120 μm. Fig. 7 compares the prediction with the experimental data for chip temperature rise and heat exchanger pressure drop as functions of the input power. Reasonable agreement is obtained for both chip temperature and pressure drop predictions.

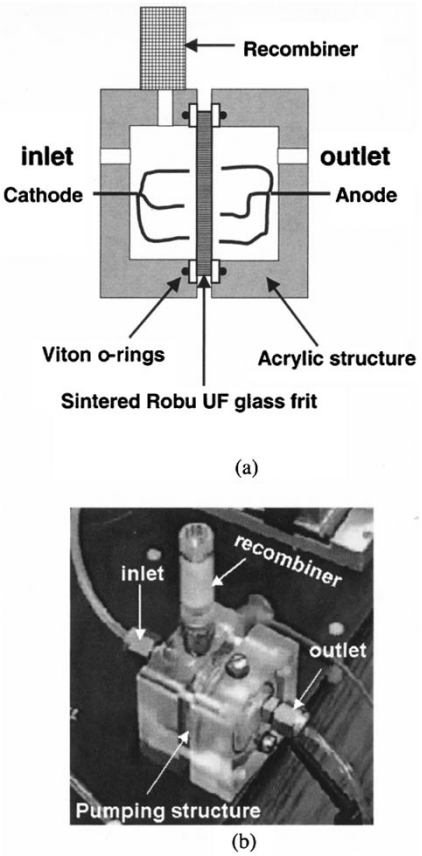

Fig. 8. Schematic and an image of an electroosmotic pump.

The simulations are effective at predicting the onset of boiling and the heat exchanger thermal resistance, thus providing a tool for design and optimization of heat exchangers.

IV. Electroosmotic Pump

Our current electroosmotic pump design consists of an active pumping structure, a catalytic reaction chamber, platinum electrodes, and Plexiglas machined parts, as shown in Fig. 8. The active pumping structure is made of an ultra-fine porous glass filter disk (Robu®), with a diameter of 30 mm, a thickness of 2 mm, and an effective pore diameter of 1 μm. The filter or "frit" disk is sintered and chemically treated to enhance the pump performance and stability. The porous frit pump material is housed within two acrylic structures and sealed into place using viton o-rings. The two acrylic structures also serve as reservoirs and support the pump electrodes and fluidic interconnects. A platinum catalyst recombination chamber, functioning to recombine electrolytic hydrogen and oxygen into water, is located at the top of the inlet reservoir. Electrolytic oxygen generated at the anode rises into the recombination chamber on the upstream side of pump. Electrolytic hydrogen generated at the cathode flows through the system and enters the upstream side of the pump and combines with the oxygen in the recombination chamber.

Characterization of the pump shows a linear relationship between backpressure and flow rate, and suggests that 1 mM buffered de-ionized water (1 mM $Na_2B_4O_7 \cdot 10\,H_2O$ dissolved into 1 liter de-ionized water) both significantly increase

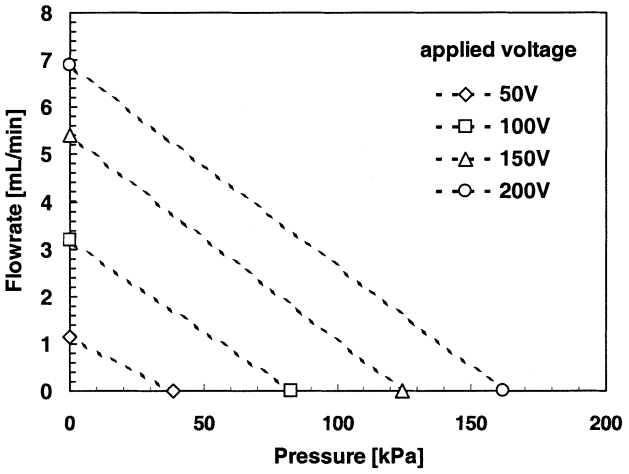

Fig. 9. Performance curves for the electroosmotic pump showing flow rate versus pumping pressure for different operating voltages.

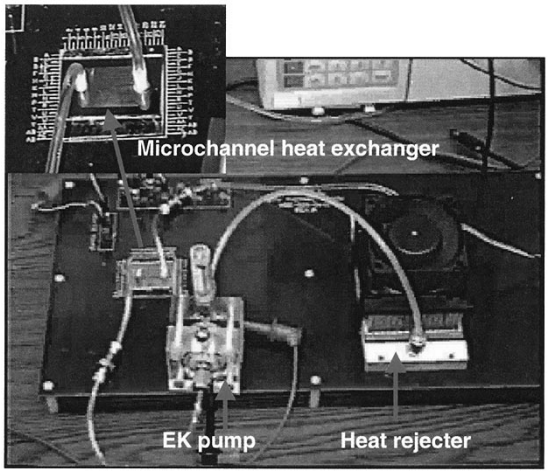

Fig. 10. Image of the closed-loop cooling system.

flowrate and effectively stabilize pump performance [27]. Fig. 9 demonstrates that an electroosmotic pump with an active volume of 1.4 cm^3 delivers a maximum flow rate of 7 ml/min and a maximum pressure of 160 KPa under 200 V applied voltage with 1 mM buffered water.

V. Closed-Loop System Performance

An image of the developed closed-loop cooling system is shown in Fig. 10. The performance of the cooling system is studied using 1 mM buffered de-ionized water as the working fluid. The applied voltage to the electroosmotic pump is 150 V and a flow rate of about 4 ml/min is obtained at the outlet of the pump. The rejecter thermal impedance is estimated to be 0.35 K/W. Its flow impedance is three orders of magnitude smaller than that of the microchannel heat exchanger under the same flow condition, and thus is neglected. Fig. 11 is a schematic of the experimental set-up for the closed-loop system characterization. The embedded heaters in the thermal chip provide uniform heating and are powered using a dc power supply. The embedded temperature sensors provide an average chip temperature using four-wire resistance measurements through a pre-calibrated temperature-resistance relationship.

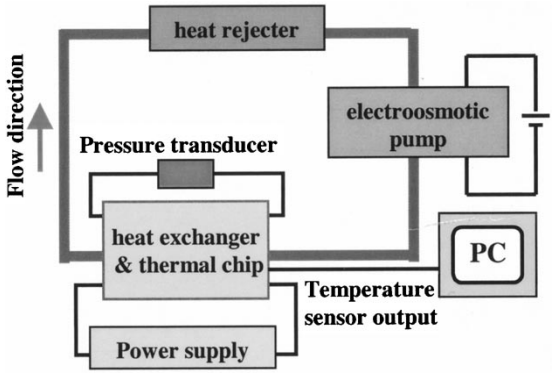

Fig. 11. Schematic representation of the experimental set-up used for characterization of the closed-loop cooling system.

A pressure transducer, connected to the inlet and outlet of the microchannel heat exchanger, provides the pressure drop across the heat exchanger. The in-situ experimental parameters, such as the input power, chip temperature, pressure drop, as well as the current across the pump, are recorded using a data acquisition system.

Fig. 12 illustrates the steady-state chip temperature and pressure drop at varying input powers. For power settings less than 26 W, a linear relation between temperature and input power is obtained. This is expected because the working fluid is in the liquid phase. In addition, the pressure drop across the heat exchanger decreases with the increasing input power due to the decreasing working fluid viscosity with the increasing temperature. A rapid increase in pressure drop indicates the onset of boiling which corresponds to a decrease in the slope of the temperature versus input power curve. Two-phase flow is observed in the microchannels, exiting from the heat exchanger and entering into the rejecter. Pure liquid, with room temperature, flows out of the heat rejecter and back to the pump. This demonstrates that present rejecter dissipates all the heat carried by the two-phase fluid. The system is performed with input power up to 38 W, and the chip temperature is kept well below 120 °C. The fluid saturation temperature is estimated about 110 °C with a pressure drop of 30 KPa at 38 W. The heat exchanger junction-fluid thermal resistance is thus calculated about 0.1 K/W, subtracting the extra temperature rise due to the thermal grease. The system is in continuous operation of five hours for each test run. Many experiments have been conducted without any issues over a few months. The preliminary data indicates that the closed-loop cooling system using electroosmotic pumping is stable and reliable.

VI. Conclusions

We have demonstrated the feasibility of an ultra-compact electroosmotic two-phase microchannel cooling system for cooling VLSI circuits. The present system, with 150 V applied voltage to the pump, removes 38 W from a 1 cm $\times$ 1 cm chip and keeps the chip temperature rise below 100 °C, with reasonable stability and reliability. Modeling predicts that junction-ambient thermal resistance below 0.1 K/W can be achieved by increasing the pump flowrate and by optimizing the channel dimensions and heat exchanger configurations.

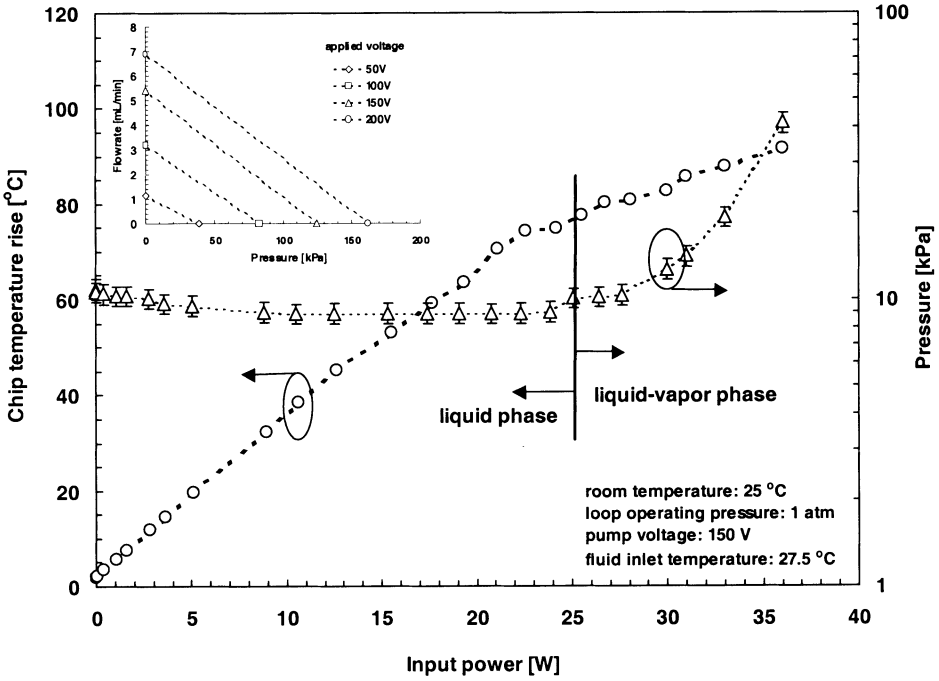

Fig. 12. System performance showing chip temperature rise and heat exchanger pressure drop for varying input powers. Pump voltage, fluid inlet temperature and ambient temperature were constant. The insert shows the pump curve at 150 V.

Future work targets integration of the microchannel heat exchanger directly onto the chip, which will eliminate the thermal interface material and improve the opportunity for alleviating on-chip hot-spots. The integration can be achieved through either fabricating channels directly in the die of an IC chip or bonding a microchannel die to an IC chip at low temperature.

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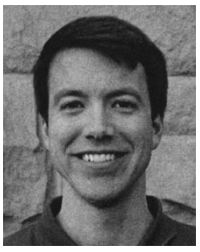

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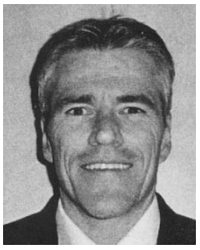

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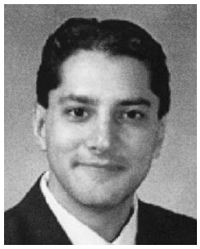

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