# CMOS Amperometric Instrumentation and Packaging for Biosensor Array Applications

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***Abstract*—An integrated CMOS amperometric instrument with on-chip electrodes and packaging for biosensor arrays is presented. The mixed-signal integrated circuit supports a variety of electrochemical measurement techniques including linear sweep, constant potential, cyclic and pulse voltammetry. Implemented in $0.5\ \mu$m CMOS, the $3 \times 3\ \text{mm}^2$ chip dissipates 22.5 mW for a 200 kHz clock. The highly programmable chip provides a wide range of user-controlled stimulus rate and amplitude settings with a maximum scan range of 2 V and scan rates between 1 mV/sec and 400 V/sec. The amperometric readout circuit provides $\pm 500\ f$A linear resolution and supports inputs up to $\pm 47\ \mu$A. A $2 \times 2$ gold electrode array was fabricated on the surface of the CMOS instrumentation chip. An all-parylene packaging scheme was developed for compatibility with liquid test environments as well as a harsh piranha electrode cleaning process. The chip was tested using cyclic voltammetry of different concentrations of potassium ferricyanide at 100 mV/s and 200 mV/s, and results were identical to measurements using commercial instruments.**

***Index Terms*—Biosensor array, biosensor packaging, CMOS amperometry, CMOS potentiostat.**

## I. Introduction

ANALYTE detection and quantification in liquid samples plays a major role in a variety of applications, especially in health care, environmental monitoring, industrial quality control and clinical investigation. Because of the required sensitivity and critical importance in daily lives, these applications require robust, easy to use, efficient, and highly accurate instrumentation systems. Miniaturized sensor arrays are capable of parallel analysis of multiple parameters. Because of the distinct advantages of microsystem platforms, there has been a trend to integrate sensor arrays onto the surface of silicon chips and perform measurement using on-chip CMOS electronics [1]–[5]. At the same time, there is a great opportunity to expand lab-on-chip solutions that replace bulky benchtop sample analysis tools with simple, low power, portable systems. The fabrication compatibility between many bio/chemical sensor interfaces and CMOS technology makes a CMOS circuit an outstanding candidate for a silicon-based lab-on-chip solution [6].

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Many techniques have been developed to measure analyte concentration in solutions including electrochemical methods, optical imaging, thermal detection, spectrometry [7] and magnetic biosensors [8]. Electrochemical methods are attractive because they can readily be adapted to CMOS instrumentation. The two techniques most commonly used to acquire qualitative information in electrochemical sensors are voltammetry and impedance spectroscopy. We have previously reported developments in CMOS voltammetry [9], [10] and impedance spectroscopy [11], [12] circuits for biosensor applications. In voltammetry, a voltage is applied to the electrochemical cell resulting in an output current between the counter electrode (CE) and the working electrode (WE) which is measured using an amperometric readout circuit [13]. A reference electrode (RE) is also often present in the system to stabilize solution potential. Numerous CMOS potentiostats have been introduced over the past decade with various functionality and performance to meet different applications demands. Several approaches to permit the use of CMOS circuitry within liquid test environments have been reported [14]–[19]. These methods utilize epoxy adhesives or PDMS to seal the electrical wires and to create microfluidic structures. However, these materials cannot survive extreme cleaning procedures, e.g., piranha cleaning, which are often required to clean electrode surfaces before biosensor interface formation. Furthermore, epoxy encapsulation has reliability issues due to poor adhesion to the chip substrate, stress imposed on wire bonds, and lack of an accurate alignment method. Another approach reported the use of parylene as the encapsulation material [20]. However, the micromaching laser source used to ablate the parylene during patterning is hard to control and potentially damaging to the sensing region underneath, and the ultrasonic bath used to lift-off the parylene could compromise sealing around the wire bonds.

Fully integrated electrochemical microsystems for DNA and detection of bacteria and biomolecules have been reported [21]–[26], but these systems do not provide all the features needed for nanostructured protein interfaces [12] targeted by this work, such as the necessity for extremely clean and flat electrodes. This paper reports a complete, single chip electrochemical instrumentation system with a broad current range amperometric readout circuit and a digitally programmable voltage waveform generator supporting a diverse set of electrochemical techniques. The multi-function amperometric instrumentation chip (MAIC) includes a $2 \times 2$ array of single-ended potentiostats and amperometric readout circuits and a waveform generator that produces triangular, saw tooth, constant potential and square pulse signals for

cyclic, linear sweep, constant potential and pulse voltammetry techniques, respectively. Furthermore, this paper introduces a chip-scale integration scheme for protein-based biosensors and electrochemical circuitry utilizing post-CMOS microfabrication including on-chip flat microelectrode array fabrication and packaging for liquid environments and harsh chemical cleaning. These post-CMOS fabrication processes were applied to an MAIC chip to form a $2 \times 2$ array of gold electrodes suitable for formation of protein biointerfaces. A unique parylene-based chip-in-package scheme is also introduced, providing excellent biocompatibility, reliable insulation for long-term use in liquids, and resistance to aggressive chemical cleaning.

The system architecture for the CMOS electrochemical sensor array is discussed in Section II. The CMOS electrochemical instrumentation circuitry is presented in Sections III and IV describes the post-CMOS electrode microfabrication and packaging. Finally, test results are presented in Section V.

## II. System Architecture

### A. CMOS Electrochemical Instrumentation

Electrochemical amperometry techniques such as cyclic voltammetry (CV) are often employed to characterize biosensor interface properties. Such techniques can readily be implemented within CMOS instrumentation circuits. For example, our group has previously reported CMOS readout electronics including a compact potentiostat that supports a very broad range of input currents, 6 pA to 10 $\mu$A [10]. A prototype electrochemical sensor platform utilizing this chip and a miniaturized biosensor array was characterized using cyclic voltammetry. Our group also reported a CMOS bi-potentiostat and amperometric readout chip that uses a common potential control unit and two readout channels to implement redox recycling to amplify electrochemical currents [27]. These successful circuits provide the foundation for the chip-scale system integration described in this paper.

### B. CMOS Electrochemical Array System Concept

The chip-scale miniaturization and integration of electrochemical sensors and their instrumentation electronics has many advantages. Through miniaturization of electrodes, the limits of detection can be extended by improving the signal to noise ratio. The direct, on-chip, electrical connection of electrodes to the instrumentation circuit eliminates external wiring and provides immunity from environmental interference. This noise reduction permits highly sensitive circuits to measure the responses of miniature biosensors, allowing a high-density sensor array within the small platform of a CMOS chip.

Many semiconductor devices and fabrication processes are compatible with biological materials, enabling the expanding use of these technologies for devices such as neural probes and biosensor arrays. Combining CMOS instrumentation circuits with miniaturized electrode arrays fabricated on CMOS chips introduces the opportunity for a monolithic measurement system. Fig. 1 illustrates the electrochemical biosensor array microsystem that serves as the conceptual model for the work in this paper. A CMOS electrochemical instrumentation chip acts as the substrate of the microsystem. An array of gold electrodes

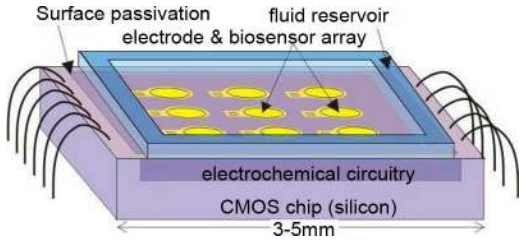


Fig. 1. Conceptual illustration of a CMOS circuit with on-chip electrode array and packaging for use in a liquid environment.

fabricated post-CMOS on the surface of the chip are connected through overglass contact openings to the underlying CMOS electronics. These electrodes must be clean and smooth to support formation of biosensor interfaces on electrode surfaces. Because the surface is uneven at overglass openings, electrode areas are defined away from overglass contacts and connected by surface metal routing. This approach also provides flexibility in the placement of surface contacts that lessens CMOS layout constraints, and it permits modification of electrode patterns without redesigning the underlying CMOS chip. To insulate surface metal routing and define size-adjustable openings over individual electrodes, a passivation layer is applied after metallization. This insulation layer also planarizes the surface and provides an interface to a variety of possible fluid handling schemes, including microfluidics or the simple liquid reservoir illustrated in Fig. 1. Alternatively, the entire chip, including wirebonds, could be coated with an insulating material as described in this paper.

The Fig. 1 electrochemical microsystem concept can be adapted to a wide range of biosensor interfaces. In this work, we have targeted protein-based nanostructured biointerfaces that can be self assembled on electrodes [12]. These nano-scale interfaces permit rapid response but impose additional microsystem design constraints, chiefly the necessity for an electrode that is flat and smooth to the nano scale.

## III. CMOS Design

For an autonomous microsystem, the CMOS chip would include all necessary instrumentation electronics and a communication interface to allow user control of measurement operations and reporting of measurement results. For the multi-function amperometric instrumentation chip (MAIC), this requires a potentiostat to control electrode biasing, a multi-function waveform generator to produce the stimulus signals necessary for voltammetry techniques, and a highly sensitive amperometric readout circuit to measure the current resulting from the stimulus voltage. Fig. 2 illustrates this arrangement of components and serves as the system diagram for the MAIC.

### A. Programmable Waveform Generator

A waveform generator is an important component of an autonomous electrochemical instrumentation system that requires different input waveforms for different voltammetry techniques. A multi-mode waveform generator is desired to produce signals of various shapes, amplitudes (scan range) and frequencies (scan rates). Programmable analog circuits could be constructed to generate continuous waveforms, but different analog circuits

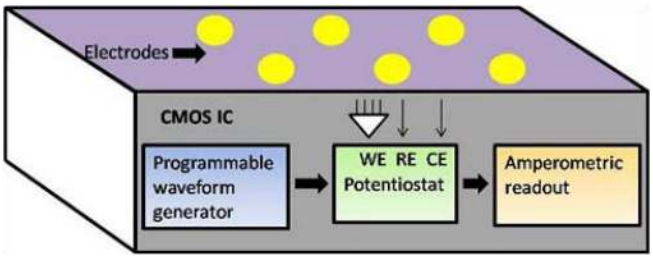


Fig. 2. Block diagram of the multi-function amperometric instrumentation system.

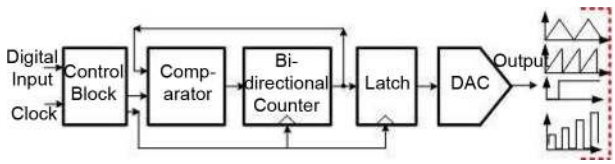


Fig. 3. A DAC-based multi-mode voltage waveform generator.

would be needed for each desired signal shape (triangle, pulse, etc.) with an undesirable impact on power consumption and chip size. A digital solution was explored to avoid the complexity of multiple analog waveform generators. A DAC with a digital controller could implement all shapes, but the output would be quantized and the complexity of the controller could be significant for the desired set of controllable waveforms. A thorough examination of the impacts of stimulus quantization on electrochemical measurements was performed. Tests demonstrated that steps in quantized stimulus signals generated noise in the electrochemical output current, but the noise reduced as step size decreased. It was determined that a stimulus step size of 8 mV or lower produced output results comparable to continuous stimulus signals. It was also determined that, with careful design, a very efficient digitally controlled waveform generator could be realized with low power and chip area. Therefore, a DAC-based multi-mode waveform generator was developed.

The digitally programmable waveform generator is shown in Fig. 3. It is composed of a digital control block, a 10-bit comparator, a 10-bit bidirectional counter, and a 10-bit DAC. The control block generates non-overlapping clock signals and control signals to reset the waveform generator, select up/down count for both positive and negative slope, and select voltammetry mode. A single pin is used to serially shift the 22-bit configuration data into the control block. This configuration input selects the desired frequency and the waveform amplitude maximum and minimum values. Based on the comparator's output, the 10-bit counter counts in either direction as needed to produce a given waveform. The counter binary bits are fed into a 10-bit DAC to produce the final analog voltage. Although an 8-bit DAC is sufficient for these waveforms, to compensate for fabrication process variations a 10-bit segmented DAC was designed to generate a staircase analog signal. It uses a combination of an R-2R ladder network and a current mode thermometer decoder, with the lower six counter bits setting the R-2R ladder and the upper four bits controlling the thermometer decoder.

The DAC output spans the range of $+1\mathrm{V}$ to $-1\mathrm{V}$ relative to analog ground with a step size of 2 mV. The output clock can be

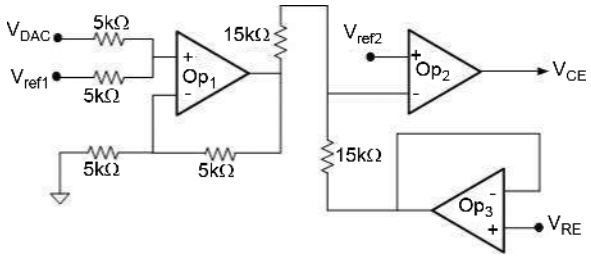


Fig. 4. Single-ended potentiostat designed for the instrumentation system.

selected from CLK, CLK/2, CLK/4, or CLK/8, where CLK is the external input master clock. This provides a stimulus signal up to 2 V pk-pk, which is suitable for most electrochemical measurements.

### *B. Potentiostat Array*

The basic function of a potentiostat circuit is to control and maintain the voltage between the WE and the CE under varying current conditions. Fig. 4 shows the schematic diagram of the 3-electrode single-ended potentiostat. Output from the waveform generator $(\mathrm{V_{DAC}})$ is level shifted by $\mathrm{OP_1}$ to match the input range of $\mathrm{OP_2}$ by summing it with $\mathrm{V_{ref1}}$. The output of $\mathrm{OP_2}$, which is buffered through negative feedback using $\mathrm{OP_3}$, is connected to the CE. For microscale sensors, the solution resistance between RE and CE can be assumed to be negligible so that CE and RE are at the same potential. The input of $\mathrm{OP_3}$ is connected to RE and no current flows through $\mathrm{OP_3}$. The output current resulting from the input stimulus voltage at CE can flow only between CE and WE. $\mathrm{V_{ref2}}$ is a DC offset control input to adjust the scan range. A $2 \times 2$ array of potentiostats was designed to support a $2 \times 2$ electrode array.

### *C. Amperometric Readout Array*

To measure the electrochemical response current within the MAIC, an amperometric readout circuit was developed. For typical biosensors, the CV current range is hundreds of $\mu\mathrm{A}$ to few mA for $1\ \mathrm{cm}^2$ electrodes [28], [29]. For gated ion channel membrane proteins, the detection limit is lower, around few of nA [30], [31]. Thus, a useful current range for a $300\ \mu\mathrm{m}$ electrode would be around pA to $\mu\mathrm{A}$. Because the response current of the biosensor can be very small, the noise performance of the readout circuit will significantly affect measurement sensitivity. For most electrochemical applications, the stimulus frequency is less than 100 Hz, and within this operating frequency the circuit noise will be dominated by 1/f noise rather than thermal noise. Based on our prior work [10], a switched capacitor current readout circuit was designed using correlated double sampling (CDS) to reduce the 1/f noise and amplifier DC offset. These techniques are now standard for low level current detection and used in commercial devices [32].

As shown in Fig. 5, a switched-capacitor (SC) charge integrator converts the input current to a voltage. The voltage is sent to a programmable gain amplifier (PGA) with a gain of $\mathrm{C_2/C_3}$, where $\mathrm{C_2}$ is a digitally programmable on-chip capacitor array. The output of the PGA is sampled and held and then fed to an analog-to-digital converter (ADC) after a low pass filter. The non-overlapping clock signals for switches $\mathrm{ph_1}$, $\mathrm{ph_2}$ and $\mathrm{ph_3}$

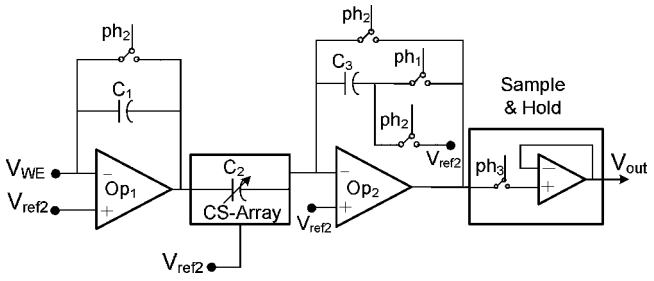


Fig. 5. Schematic of amperometric readout circuit.

are generated by an on-chip clock generator block. The output voltage of the current readout circuit is given by

$$V_{out} = \frac{I_{WE}}{f_s \bullet C_1} \bullet \frac{C_2}{C_3} \tag{1}$$

where $I_{WE}$ is the current at the WE and $f_s$ is the frequency of switch $\mathrm{ph}_2$, $\mathrm{C}_1$ is the integrating capacitor. Thus, the input current range can be adjusted to output of different biosensors through programmable selection of the clock frequency and the PGA gain. These programmable features can be used to calibrate sensors over time.

Several improvements have been implemented in the new readout circuit to increase measurement sensitivity. In the CDS technique, the noise reduction factor is typically determined by device matching, timing errors, charge injection and clock feedthrough. To curtail charge injection, all switches were realized with minimum size transistors. To reduce clock feedthrough errors, the NMOS switches were replaced by a structure with one NMOS switch and two NMOS dummy transistors. An on-chip clock generator was developed to provide precise time sequence control for switch activation.

Noise in the amplifier also directly affects the sensitivity of the readout circuit. A folded cascode amplifier was chosen because it provides high DC gain and wide dynamic range. According to the noise analysis in [10], the size of the input transistors is critical. Increasing the value of WL and W/L can reduce the 1/f noise and thermal noise. However, larger input transistors will lead to larger input bias current, which limits the sensitivity of the readout circuit. An input bias current of hundreds of fA at $25^{\circ}\mathrm{C}$ was reported for an input NMOS of $\mathrm{W/L} = 150\,\mu\mathrm{m}/1.8\,\mu\mathrm{m}$ [10]. To optimize the tradeoff between noise, speed and input bias current, this design sets $\mathrm{W/L} = 72\,\mu\mathrm{m}/1.8\,\mu\mathrm{m}$ for the NMOS inputs transistors. To further improve noise performance, all of the analog circuits were surrounded by capacitors between $\mathrm{V_{DD}}$ and GND to minimize power supply noise, and the analog and digital power routings were separated over the whole chip to minimize digital clock noise coupling onto analog signals. Through these improvements, the sensitivity was increased by a factor of six compared to prior work [10].

## IV. Post-CMOS Electrode Arrays and Packaging

Realizing a single-chip biosensor array with embedded instrumentation circuitry requires the synergistic integration of CMOS design, electrode fabrication and packaging while simultaneously meeting requirements set by 1) IC process compatibility, 2) biointerface self assembly, 3) electrochemical analysis capability and 4) operation in a liquid environment. Fabrication processes such as metal vapor and chemical vapor deposition, wet chemical and plasma dry etching, and photolithography maintain the reliability of active circuits within the CMOS substrate when conducted at temperatures lower than $400^{\circ}\mathrm{C}$ [33], forming a limited microfabrication tools set. Similarly, requirements for biointerface assembly and operation in a liquid environment constrain the materials and structures available for electrodes and packaging. To meet these complex constraints, a scheme combining electrode fabrication and chip packaging was developed that utilizes complementary die-level and package-level process steps.

### A. Insulation and Packaging Materials

Operation of the CMOS biosensor array in an aqueous environment establishes a critical requirement to insulate all surfaces of the CMOS device in contact with the liquid. The small surface area available on a CMOS chip necessitates either a complex fluid handling system or packaging of the entire chip for immersion in liquid. Because the chip's surface must remain accessible for biointerface formation and sensor operation, flip-chip packaging and other approaches that similarly bury I/O bondpads cannot be employed in a straightforward manner. Alternatively, a chip-in-package approach utilizing wirebonded die was adopted in this work, establishing a need for a protective insulating material capable of coating all surfaces of the 3D chip structure, including chip sidewalls and wirebonds. At the same time, the packaging approach must permit patterning of the 2D chip-electrode surface and cleaning of electrodes to remove any metal ions or contaminants before biointerface assembly. For example, our experiments have shown that aggressive electrode cleaning by piranha solution and organic cleaning are required for reliable self assembly of nanostructured biointerfaces. The packaging material must therefore withstand the strong corrosiveness of piranha solution. Several materials were studied to meet these demands.

SU-8 photoresist is widely used in MEMS fabrication; it is available in a wide range of viscosities and is suitable to form thick layers and high aspect ratio structures [34]. However, when tested experimentally, cracks were observed after prolonged soaking in an aqueous environment. Fig. 6(a) shows a CMOS chip with a thick SU-8 passivation layer, and Fig. 6(b) shows cracks that developed near the pad area and caused corrosion of the bonding pads that rendered the chip useless.

Polyimide is another insulating polymer material widely used in bioMEMS packaging applications, although it cannot achieve layers as thick as SU-8. Polyimide can be applied by spin coating and curing in a low temperature oven. It is easy to pattern using either wet or dry etching, and our tests indicate it provides excellent coverage and uniformity on 2D flat surfaces and survives prolonged use in an aqueous environment. However, when tested for coverage of 3D structures like a wirebonded chip, cracks in the polyimide layer due to shrinkage during curing were observed. Fig. 6(c) shows a polyimide-coated CMOS chip with large cracks (light color

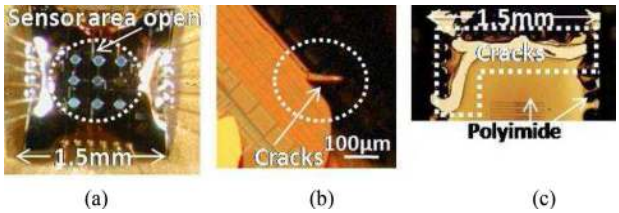


Fig. 6. (a) A CMOS chip packaged using SU8 with electrodes exposed. (b) A crack in SU8 observed at the interface of the chip and SU8 where leakage occurs. (c) A polyimide coating on the surface of a packaged chip that cracked after hard baking.

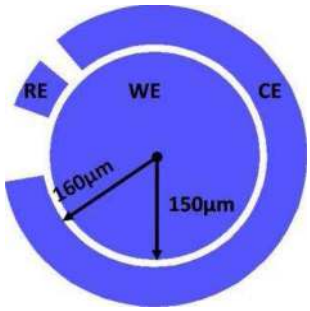


Fig. 7. Single element of an electrode array consisting of WE, RE and CE.

within the dotted line) where the polyimide layer approaches wirebonds on the chip's periphery (dark color within dotted line).

Parylene, or poly (p-xylylene), is a thin film polymer that is also popular for insulating electronics. Parylene is chemically inert, permits conformal coating and has excellent barrier properties. Parylene C (poly(monochloro-p-xylylene)) has the highest possible biocompatibility rating among polymers for long term implants and has an extensive history of use in the medical industry. Because of its biocompatibility, biostability, low cytotoxicity and resistance against hydrolytic degradation, Parylene C has been widely used in micro/nano-fabricated devices and microfluidics. Parylene C utilizes a simple chemical vapor deposition method with low process temperature and is compatible with standard microfabrication processes. Our experiments have shown that parylene successfully overcomes the problems associated with SU-8 and polyimide, providing an excellent and long-lasting coating of 3D structures like wirebonded chips.

### *B. CMOS Design for Surface Electrodes*

The amperometric instrumentation circuit described above was designed in 3M, 2P, $0.5\ \mu\mathrm{m}$ CMOS and implemented on a $3 \times 3\ \mathrm{mm}^2$ chip. The chip layout includes overglass openings that permit connection between CMOS metals and an array of electrodes formed directly on the surface of the chip using post-CMOS processing. These contact openings are placed away from the desired electrode area so that the electrode surface can remain flat without a metal planarization step. To support self assembly of nanostructured protein interfaces, the surface electrodes must be flat to the scale of nanometers. Because the CMOS process is not planarized following deposition of the top metal, the circuit was routed without the top CMOS metal layer to ensure a flat chip surface for electrode formation.

### *C. Die-Level Fabrication*

To form an on-chip microelectrode array, gold is an outstanding metal because it can readily be deposited and patterned, is inert and biocompatible in a biosensing liquid environment, and permits immobilization of biointerfaces using well established adhesion chemistry. The on-chip electrode could be fabricated using an electroless nickel immersion gold process that replaces the aluminum layer from a standard CMOS process [35]. However, the deposition thickness of gold is difficult to control with this method due to its deposition mechanism, and the process is prone to poor reproducibility because of variable aluminum alloy composition across a chip and between different chips. Our experimental efforts with this deposition process have resulted in a non-uniform gold layer with high surface roughness. Alternatively, the on-chip microelectrode array could be fabricated using conventional physical vapor deposition (PVD) and photolithography, which provides precise control of electrode thickness and area. With this method, the roughness of the gold is subject to the surface profile of the CMOS chip, which is typically passivated by a flat silicon dioxide layer. For many protein-based biosensors, the electrode roughness is a critical parameter. For example, a biosensor utilizing a biomimmetic tethered lipid bilayer membrane [12] must have a very smooth surface to prevent pinholes in the self assembled lipid bilayer.

To enable electrochemical measurement, each element of the on-chip array includes a WE, CE and RE. Development of a reliable planar reference electrode remains a research challenge, and a pseudo RE was chosen so that all electrodes could be formed using Au. Fig. 7 describes the electrode pattern that was designed to maximize the electrochemical response current and realize uniform ion flow by arranging the electrodes concentrically. The distance between WE and CE is kept small to minimize errors due to potential drop in the solution. The working electrode is relatively large to maximize sensor area, and the size can easily be modified to suit different biosensor interfaces based on the electrochemical current level (which is a function of WE area) and desired array density.

The die-level post-CMOS fabrication process begins with formation of the electrode array on the CMOS MAIC chip. We refer to this as die-level processing because we receive from the foundry and process individual die, but the same processes can be applied at a wafer scale. The electrodes are formed by thermal evaporation of titanium/gold (50 Å/1000 Å) and patterning by wet etching. This metallization step also creates routing between electrodes and surface contacts to CMOS electronics, and it covers all surface CMOS metal, including bondpads, to eliminate chemical reactions between the CMOS aluminum alloy and the alkali photoresist developer, which has been observed to contaminate the surface electrodes. Polyimide is then spin coated on the CMOS chip surface and patterned to insulate surface routings and define the electrode area while leaving bonding pads open for subsequent wire bonding. Polyimide was chosen because it provides good coverage of 2D surfaces and is much easier to pattern than the parylene applied later in the package process. The die-level process steps are

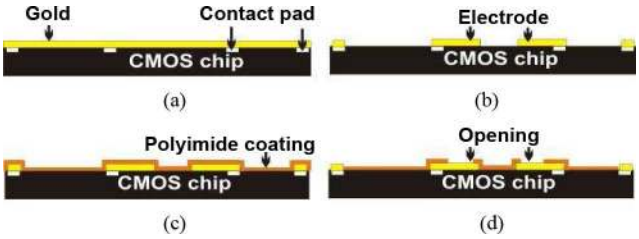


Fig. 8. Process flow for post-CMOS electrode fabrication: (a-b) Ti/Au is deposited and patterned; (c-d) Polyimide is spin coated and patterned.

illustrated in Fig. 8. At the end of this process, the electrode array has been formed and the chip surface has been passivated everywhere except the desired electrode areas and the wire bond pads.

Die-level microfabrication introduces several challenges that are worth noting. While performing photolithography on individual die, such as the $3 \times 3\ \mathrm{mm}^2$ chips used in this study, photoresist builds up at the edge of the chip during spin coating due to surface tension. This leads to uneven coating across the substrate that makes proper exposure extremely difficulty. However, we have developed a modified procedure to enable successful photolithography for die-level processing. To mitigate thick-edge effects, the chip was bonded using photoresist to the outer perimeter of a silicon wafer. This permits the die to spin at maximum speed for a given spin rate, minimizing photoresist buildup at the edges of the chip. The orientation of the die was observed to have a significant impact on photoresist buildup, with more buildup on the sides parallel to the spin radius and less on the sides orthogonal to the spin radius. It was also observed that photoresist buildup is worse at bonding pads where the overglass contact openings provide a reservoir to hold photoresist. Thus, to provide the most uniform coating of photoresist during die-level processing, the CMOS chip was designed to use bonding pads on only two parallel sides of the chip, and those sides were placed orthogonal to the spin radius. In addition, the electrode array was located near the center of the chip to avoid any edge buildup effects. As a result, the entire chip surface could be properly patterned to define the Au and polyimide layers. The same methods can be applied to pattern any small substrate for millimeter sized MEMS devices and microsystem applications.

### *D. Package-Level Fabrication*

To meet packaging demands while keeping cost and complexity low, a solution was developed using a chip-in-package approach, where the MAIC chip was mounted and wire bonded to a standard dual in-line package (DIP) and the package body was used as a liquid reservoir. Fig. 9 describes the package-level post-CMOS process for the chip-in-package approach. Following the die-level processing described above, the MAIC chip was wire bonded to a ceramic DIP package. The packaged chip was then coated with a 5ìm layer of parylene using PVD (PDS 2035CR, Specialty Coating Systems). This process covers all surfaces within the package, including bond wires, package contact pads and the electrode array chip. Next, parylene needs to be removed from the electrode array area while leaving all

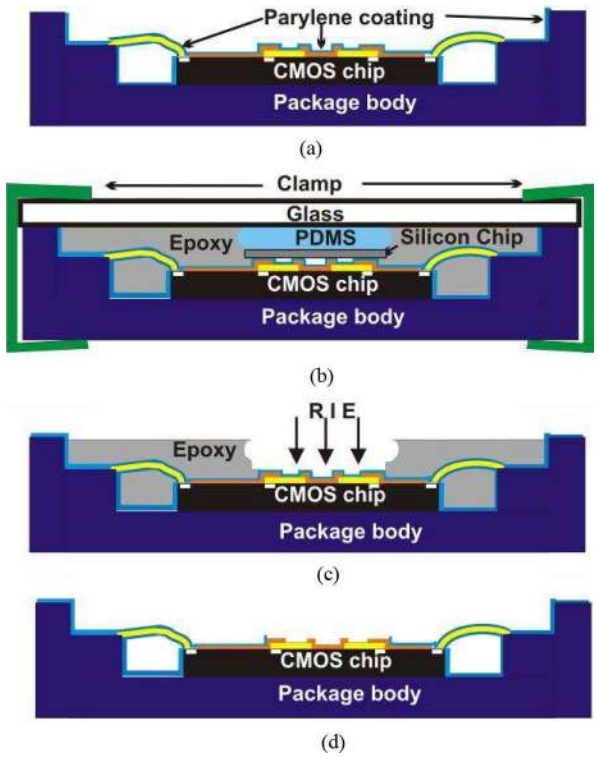


Fig. 9. Process flow of chip-in-package sealing for liquid environment. (a) Chip is wire-bonded to package and coated by $5\ \mu\mathrm{m}$ parylene. (b) A PDMS cylinder and silicon chip are attached to a glass slide and clamped to the package to cover the center of the CMOS chip before crystal adhesive is melted to fill the cavity. (c) Glass slide is detached and parylene is etched away by oxygen RIE. (d) Crystal adhesive removed to form final package with all non-electrode surfaces insulated.

other surfaces coated. Parylene is generally etched by reactive ion etching (RIE) using oxygen gas with photoresist or another solid layer deposited and patterned to form a masking layer. However, in this complex three-dimensional structure, such methods cannot meet masking requirement, and a customized, non-traditional process was developed to overcome this challenge. First, a hole punch was used to create a cylinder of PDMS sized to match the area of the chip's surface from which parylene would be removed, $\sim 1.5\ \mathrm{mm}$ diameter in this case. A silicon chip of slightly smaller diameter was also cut from a wafer using a dicing saw. The cylinder was then attached, on one side, to the silicon chip using oxygen plasma assisted bonding and, the other side, to a glass slide. The silicon chip was included to eliminate direct contact of PDMS with parylene, which was observed to leave unwanted particle contaminants that were difficult to remove. The glass slide was then clamped to the parylene-coated chip-in-package with the silicon chip pressed down over the electrode area. Crystal adhesive was then inserted into the cavity beneath the slides and melted at $120^{\circ}\mathrm{C}$ to fill the cavity except where the PDMS/silicon cylinder was held [Fig. 9(b)]. Later, the slide/PDMS/silicon assembly was removed leaving parylene everywhere except the interior of chip's surface where previously deposited polyimide remains to insulate surface routing and leave only the electrodes exposed. Parylene was then etched using RIE, with 300 W RF power and 500 sccm oxygen flow rate, to expose the desired electrode surfaces [Fig. 9(c)]. Once the crystal adhesive was removed

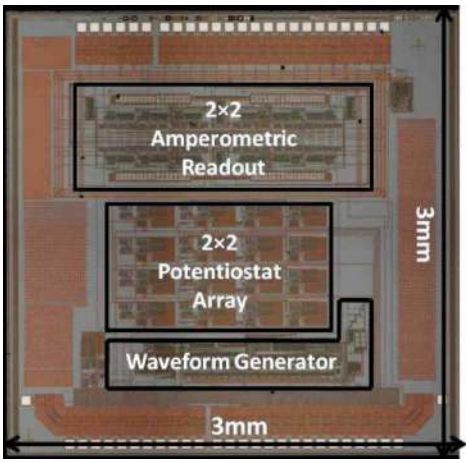


Fig. 10. The $3 \times 3\,\mathrm{mm}^2$ CMOS amperometric instrumentation chip with waveform generator and 4-channel potentiostat and amperometric readout array.

TABLE I
WAVEFORM GENERATOR CHARACTERISTICS

| | |
|---|---|
| Area | $0.44\mathrm{mm}^2$ |
| DAC Resolution | 10 bit |
| Scan range | 0- 2V pk-pk, 10-bits |
| Scan rate | 1mV/sec-1000V/sec |
| Step size | 2mV |

using acetone, the final package provides exposed electrode with all other surfaces coated with parylene [Fig. 9(d)].

## V. RESULTS

A version of the MAIC with the multi-function waveform signal generator and a 4-channel potentiostat and amperometric readout circuit array was fabricated in $0.5\ \mu\mathrm{m}$ foundry CMOS. The $3 \times 3\ \mathrm{mm}^2$ die shown in Fig. 10 was thoroughly tested to verify functionality and characterize performance. Table I summarizes the characteristics of the waveform generator suitable for various cyclic, linear sweep, constant potential and pulse voltammetry electrochemical techniques. To characterize the range and resolution of the amperometric readout circuit, the input current was swept using a Keithley 6430 sub-femtoamp source meter at different update clock frequencies and gain settings to span the functional input current range. Within each range, the maximum deviation between measured current and the linear input source was recorded as the linearity error. Table II shows a set of test results spanning the circuit's functional input range, with range settings from $\pm 47\mathrm{pA}$ to $\pm 47\ \mu\mathrm{A}$. Within each setting, the input range defines the max current before op-amps become nonlinear and create significant distortion. The 200 Hz to 2 MHz data show that the resolution decreases roughly linearly with clock frequency, and at 2 kHz and above the resolution is about 0.3% of the range. Fig. 11 shows test results where the maximum resolution of $\pm 500\ \mathrm{fA}$ is achieved with gain setting of 2 at 20 Hz clock; leakage currents prevent operation at lower frequencies. The power consumption of the 4-channel instrumentation circuit could not be measured independently of test circuits but was simulated to be 22.5 mW at a maximum clock frequency of 200 kHz.

TABLE II
CHARACTERISTICS OF THE CURRENT READOUT CIRCUIT

| Clock frequency | 20 Hz | 200 Hz | 2 KHz | 20 KHz | 200 KHz | 2 MHz |
|---|---|---|---|---|---|---|
| Gain setting | 2 | 1 | 1 | 1 | 1 | 1 |
| Input current range | ±47 pA | ±1.8 nA | ±48 nA | ±489 nA | ±4.8 μA | ±47 μA |
| Linearity error | 1pA | 13pA | 150 pA | 1.5nA | 15nA | 190 nA |

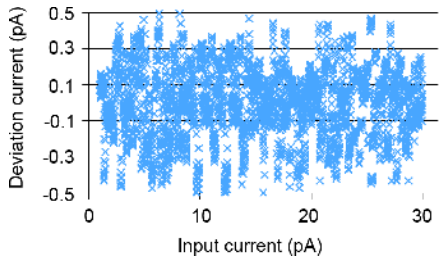


Fig. 11. The deviation between input current and measured current for 1 pA to 30 pA inputs at 20 Hz updating clock and gain=2 setting.

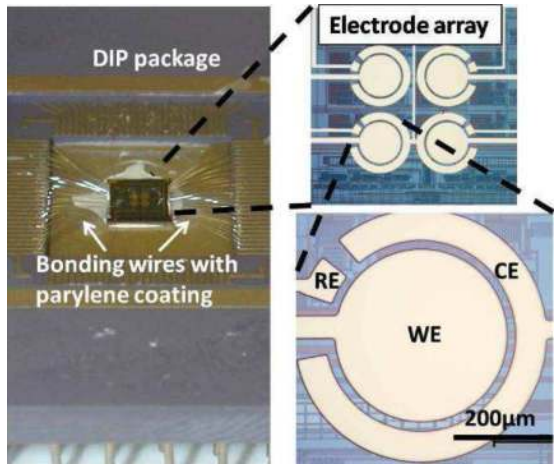


Fig. 12. Photograph of a CMOS biosensor array chip-in-package and close up views of the post-CMOS surface electrode array.

A $2 \times 2$ electrode array was fabricated on chip, and the chip was packaged by methods described in Section IV. The final packaged CMOS chip with electrode array is shown in Fig. 12. This package scheme is suitable for subsequent integration with microfluidic channels mounted either to the chip or to the package. The wire bond contact pads are the most vulnerable area in this type of packaging. To evaluate the package sealing, the chip was powered up and successfully tested after a water drop was dispensed on the chip. Subsequently, the packaged chip was exposed to piranha solution to clean the electrode array, verifying the capability to withstand the aggressive chemical processing necessary before protein biosensor interface formation on the electrodes.

To verify electrochemical measurement capability of the integrated system, a test setup composed of an MAIC chip, a packaged on-chip electrode array, and a PC with a DAQ card and a

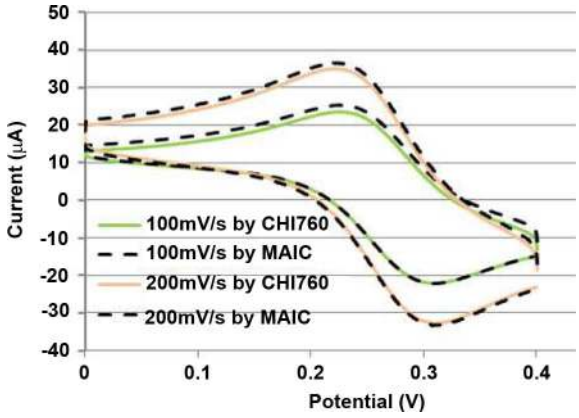


Fig. 13. CV measurement of 0.5 mM potassium ferricyanide at 100 mV/s and 200 mV/s for both CHI 760 commercial instrument and proposed circuit.

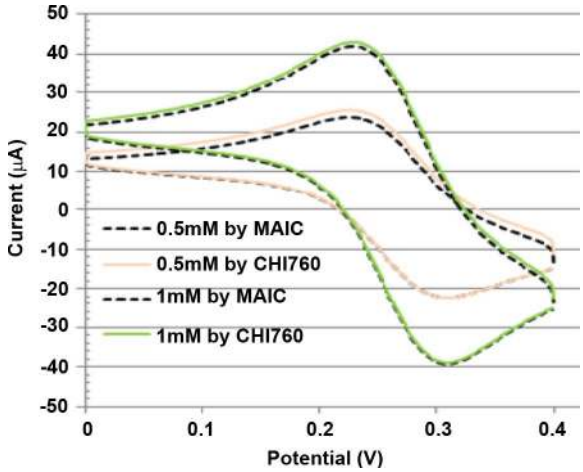


Fig. 14. CV measurement of potassium ferricyanide at 0.5 mM and 1 mM for both CHI 760 commercial instrument and proposed circuit.

LabVIEW user interface was prepared. A typical electrolyte solution with 1 M potassium chloride and 0.5 mM potassium ferricyanide was prepared, and cyclic voltammetry measurements were performed at $25°\mathrm{C}$ using an on-chip WE, a commercial liquid junction Ag/AgCl RE and a platinum CE. Fig. 13 shows the results from both a commercial potentiostat (CHI760C, CH Instruments Inc.) and the MAIC at scan rates of 100 mV/s and 200 mV/s. In cyclic voltammetry, the peak locations give important information for biochemical identification, and these results demonstrate that the peak locations and amplitudes of the CMOS system compare extremely well with the commercial system even at different scan rates. In another experiment, a second solution with 1 mM potassium ferricyanide was prepared and cyclic voltammetry measurements were performed. Fig. 14 shows results from both the commercial potentiostat and the reported CMOS amperometric system at two different electrolyte concentrations. As expected, the peak current increased with electrolyte concentration, and again the peak locations and amplitudes of the CMOS system compare extremely well with the commercial system. These experiments verify the proper operation of the MAIC, the functionality of the post-CMOS electrodes, and the suitability of the parylene-based packaging for operation in liquid environments.

Tests were also performed to characterize the measurement variation arising from differences in readout channels and electrodes across the array. Variation results will be reported as $\mu(1 \pm \sigma/\ \mu)$ where $\mu$ and $\sigma$ are mean and standard deviation, respectively. Variations in readout channels will occur due to intra-chip process variations. When four readout channels on one chip were tested with a $20\ \mu\mathrm{A}$ input current, the results were $20(1 \pm 0.8\%)\mu\mathrm{A}$. Variations in electrodes could be caused by variations in the photolithography process, alignment errors, or differences in the cleanliness of electrodes. When four electrode on the same array were tested electrochemically, oxidation and reduction peak separations were found to be $0.09(1 \pm 2.2\%)\mathrm{V}$. For comparison, peak separation was measured for a single electrode while sweeping the potassium ferricyanide potential for 15 cycles, and variation in peak separation was recorded as $0.074(1 \pm 4\%)\mathrm{V}$. These results indicate that the observed intra-chip variations in circuits and electrodes are less significant than variations caused by electrochemical solution.

The long term stability of CMOS biosensor arrays are potentially limited by a) electronics, b) packaging, c) biointerface. Absent radiation and temperature extremes that are not common to biosensor applications, CMOS electronics stability will be limited by chemical interactions with the liquid environment, which must be protected by the packaging. The reported parylene packaging was chosen specifically for its ability to provide this protection, and a parylene coated CMOS chip has been reported to remain stable in $77°\mathrm{C}$ saline for more than six months [36]. Thus, stability of biosensors based on the reported CMOS array will likely be limited by the performance of specific biointerfaces chosen to implement the sensor.

## VI. Conclusion

A CMOS amperometric instrumentation system with on-chip electrode array and packaging for biosensor arrays was presented. This system can generate multiple voltage waveforms with programmable scan rates of 400 V/sec to 1 mV/sec and a scan range of 0–2 V in 2 mV steps to support a variety of electrochemical voltammetry techniques. The chip contains a 4-channel single-ended potentiostat and amperometric readout circuit that was tested to provide a $\pm 47\ \mu\mathrm{A}$ range and $\pm 500\ \mathrm{fA}$ linear resolution. A post-CMOS fabrication process was described for forming an on-chip electrode array suitable for protein-based biosensors and parylene packaging suitable for operation in a liquid environment. Functionality of the overall system was verified by performing cyclic voltammetry in a potassium ferricyanide solution. The on-chip instrumentation circuits successfully performed electrochemical measurements at different scan rates and electrolyte concentrations. The instrumentation circuitry and post-CMOS fabrication processes reported here are suitable for forming single-chip electrochemical analysis microsystems with a wide range of biological and chemical sensor interfaces.

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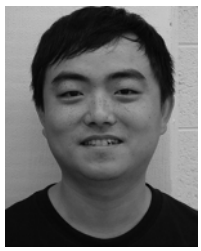

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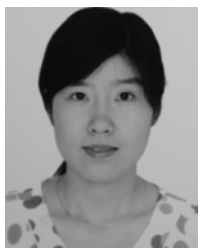

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