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CMOS Analog AGC for Biomedical Applications

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Abstract: In this paper, we present the design of an analog Automatic Gain Control with a small silicon area and reduced power consumption using a 0.5 µm process. The design uses a classical approach implementing the AGC system with simple blocks, such as: peak detector, difference amplifier, four-quadrant multiplier, and inversor amplifier. Those blocks were realized by using a modified Miller type OPAMP, which allows indirect compensation, while the peak detector uses a MOS diode. The AGC design is simulated using the Tanner-Eda environment and Berkeley models BSIM49 of the On-Semiconductor C5 process, and it was fabricated through the MOSIS prototyping service. The AGC system has an operation frequency of around 1 kHz, covering the range of biomedical applications, power consumption of 200 µW, and the design occupies a silicon area of approximately 508.8 µm × 317.7 µm. According to the characteristics obtained at the experimental level (attack and release time), this AGC can be applied to hearing aid systems.

Keywords: CMOS; non-linear systems; analog AGC

1. Introduction

Chronic diseases are considered the main cause of death in the world, with cardiovascular, oncological and respiratory diseases, as well as cerebrovascular accidents and diabetes comprising 54% of deaths in 2016 [1]. In recent years, mobile technologies, in conjunction with biomedical systems, have been used to aid in the recognition of diseases and patient management. These systems provide direct and regular monitoring of important vital signs, such as heart rate, blood oxygen saturation level, body temperature, respiratory rate, blood pressure in the circulatory system [2], and can be used as clinical tools to observe a particular disease or provide a better understanding of a user's health status. Since the electronics industry is in continuous advance, there is a tendency in the monitoring of biological signals towards reducing device size and power consumption. As shown in Table 1, these signals range from a few microvolts (µV) to hundred of millivolts (mV), which makes it difficult to obtain an accurate reading, especially when assessment is done in a noisy environment. The block diagram of a portable biomedical system for ECG signals is shown in Figure 1 [3]. The low frequency electrode signal (0.01–300 Hz), is injected into an instrumentation amplifier coupled in AC, which amplifies the signal up to a range of 32 dB to 40 dB, and filters the common-mode noise and electrode offset [4]. Subsequently, the filter (Reject Band) rejects the power line noise (50 Hz–60 Hz) [5]. The next stage is a variable gain amplifier (VGA) [6], which changes its gain in order to maintain the output signal within optimal values for an analog-to-digital converter (ADC). This paper proposes the

use of an Analog Automatic Gain Control (AGC) to handle amplitude changes in biomedical signals to adequate the signal into the input range of the ADC.

Table 1. Characteristics of biomedical signals.

Biomedica Signal	Frequency (Hz)	Amplitude
ECG (Electrocardiogram)	0.01–300	0.05–3 (mV)
EEG (electroencephalogram)	0.1–100	0.001–1 (mV)
EOG (Electro-oculogram)	0.1–10	0.0001–0.03 (mV)
EMG (Electromyogram)	50–3000	0.001–100 (mV)
PPG (Photoplethysmography)	<10	>95% (Levels of SpO_2)
Body temperature	0–0.1	32–40 (C)
Blood pressure	0–50	10–400 (mm Hg)
Respiratory rate	0.1–10	2–50 (Breaths/min)

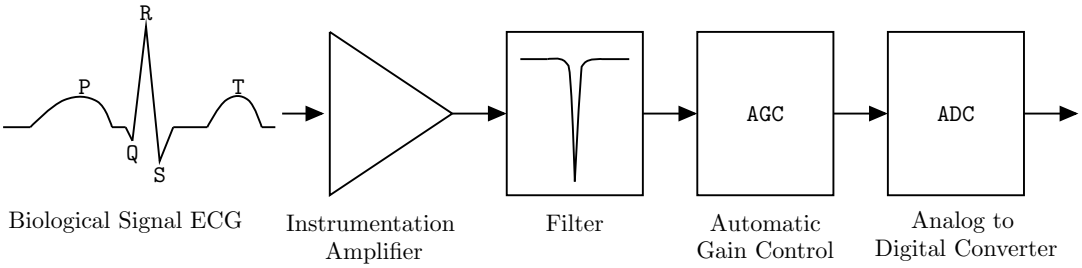


Figure 1. Basic diagram for a biomedical system.

An AGC is an essential component in many electronic systems in fields such as communications [7–9], audio, sensor calibration [10], disk drives and charge-coupled device (CCD) type imaging equipment. The main contributions in AGCs for biomedical applications are in Cochlear Implant [11–14], control of the amplitude of biomedical signals [15], hearing aids [16], and bionic ears [17]. References [16,17] report a circuit design integrated into a silicon area less than 4.41 mm^2 and power consumption less than 100 µW. Its main purpose is maintaining the amplitude of a given signal in a range such that the following blocks can process it. If the input signal shows large variations in its amplitude, it may cause the circuit to malfunction. For example, in a communication system where the transmitter-receiver are too far apart, the signal is weaker when it reaches the receptor and, according to probability, failure to transmit tends to decrease the signal-to-noise ratio of the transmission channel [18]. Despite being a well-known block, AGC is still heavily worked on by circuit designers to improve their power consumption, raise their response speed, minimizing size, etc. [18,19].

In this paper, we present an analog AGC, in a small area of silicon, low power consumption, a high output voltage swing (1.2 V), a programmable operating frequency between 1 Hz and 1 kHz, release times, attack time and reconfigurable reference voltage with a simple AGC structure for handling biomedical signals shown in Table 1. The proposed amplifier is a variant of the conventional Miller amplifier, which use an indirect compensation loop that reduces the area consumption in silicon, improves the product gain bandwidth, and the setting-time of the opamp with reduced power consumption compared to a class A amplifier. The peak detector was built by using the modified Miller opamp and a diode. This structure is proposed because presents better output voltage swing compared to [8,20]. Despite a diode is a simple device, the selected technology does not provide this element as part of the available library, so it was necessary to fabricate several diode structures in order to obtain its electrical characteristics.

2. Automatic Gain Control (AGC)

Ideally, an AGC will keep the amplitude of its output signal constant despite amplitudes changes at its input [19]. An AGC is typically a feedback system, which can be represented in terms of

a nonlinear transfer function. The ideal transfer function for an AGC scheme is depicted in Figure 2. With an input signal lower than a voltage threshold V_1, the AGC will not work and the output signal is a linear function of the input. When the output signal passes the threshold value (V_1), the AGC works and maintains an approximately stable level at the output until it enters a second threshold value (V_2). After passing this threshold it stops functioning correctly due to the saturation of the output signal. The operation thresholds discussed above are determined by a reference voltage V_{REF}, which regulates the amplitude of the output signal.

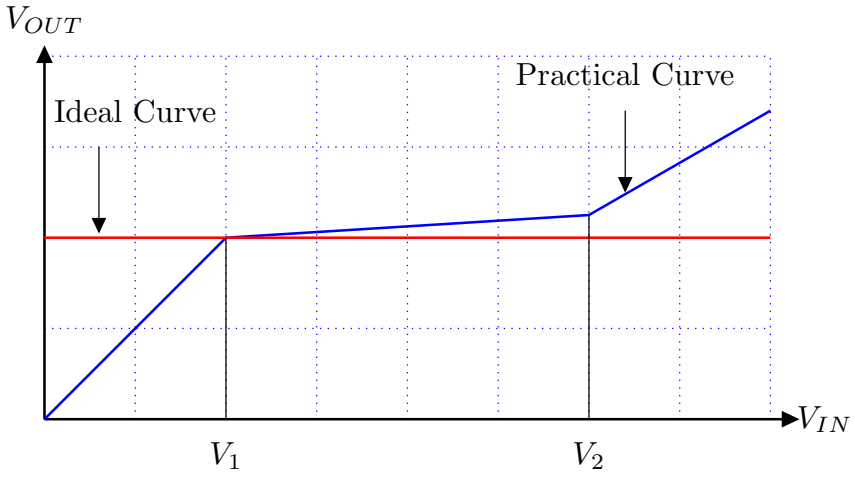


Figure 2. AGC ideal and practical transfer function.

There are two ways to implement an AGC: by feeding the output signal to an internal block (feedback) [21,22] or by feeding the input signal to more than one internal block (feed-forward) [23]. This work will analyze the analog version of the first option, which is shown in Figure 3.

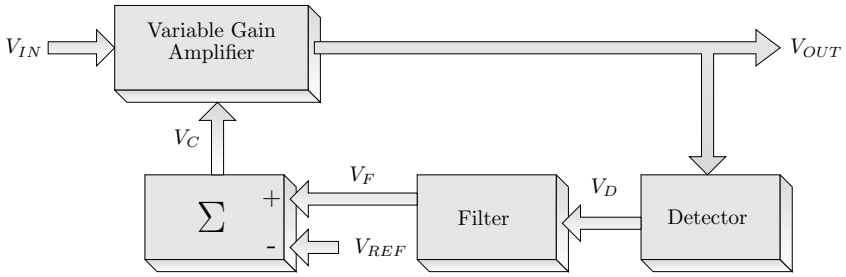


Figure 3. Analog AGC feedback configuration [23].

Some important parameters for AGCs are:

- Settling time (τ): Set time needed by the circuit to regulate the loop gain in the AGC in response to a variation in amplitude in the input signal.
- Attack time (A_T): Time necessary for the AGC to respond to an abrupt increase in the amplitude of the input signal. It is quantified from when the input signal changes until the AGC attenuates the output amplitude to a value close to the V_{REF} with a tolerance.
- Release time (R_T): Time required for the AGC to respond to an abrupt loss in amplitude. It is quantified from when the input signal changes up until it amplifies the output signal to a value close to the V_{REF} with a tolerance.

Operating Principle

The main feature of the configuration shown in Figure 3 is its requirement of a single detector with a low dynamic range, as well as its high linearity. The input signal V_{IN} is injected into a variable gain amplifier (VGA) controlled by the V_C signal, which closes the loop. Some parameters of the output signal, such as amplitude, carrier frequency, modulation index or frequency, are sensed by the peak detector, after which the undesirable components are filtered. The V_F signal is then subtracted by voltage reference V_{REF} to generate the V_C signal, which controls the VGA to adjust the loop gain and therefore keep the amplitude of the output signal V_{OUT} at a constant level. The mathematical description of the transfer function is taken from [24].

3. Analog AGC

The proposed CMOS analog AGC is shown in Figure 4a, and implements the Variable Gain Amplifier (VGA) with a four-quadrant multiplier. As to the selected CMOS multiplier uses differential input and output signals, a differential-to-single (D2S) and single-to-differential (S2D) converters are required. A peak detector was selected in order to extract the output signal amplitude and a simple RC circuit was used as the filtering block. Finally, a difference amplifier closes the feedback loop.

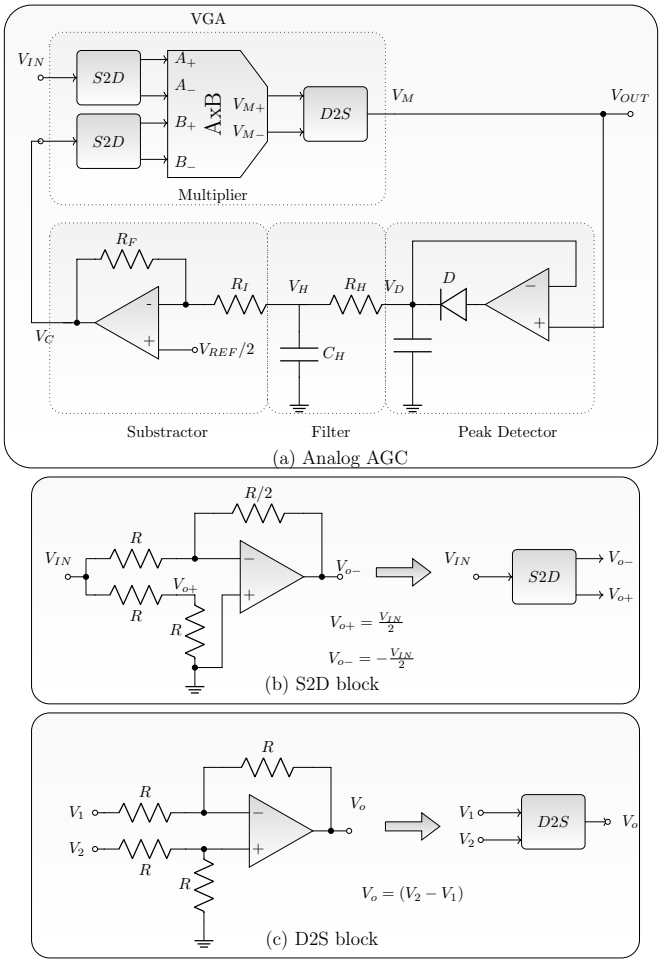


Figure 4. Proposed AGC for this work.

3.1. Operational Amplifier

The AGC design is based on an modified Miller type operational amplifier (OPAMP) with indirect compensation and a class-A output as shown in Figure 5, which is composed of a differential pair (M_3–M_4), followed by an output stage comprising a type-A amplifier (M_9–M_{10}) and a capacitor (C_c).

The non-inverting input is connected to the gate of M_3, which works as a voltage to current transconductor, connected to M_5–M_{10}, these transistors constitute a current mirror that copies the current from M_3 to the output branch v_o. The inverter input (V_{in-}) is connected to the gate of M_4, which works as a voltage-to-current transconductor, and is converted to voltage by $(r_{04} \| r_{06})$. This voltage is connected to the gate of M_7 and is converted in current through gm_7. The M_8–M_9 transistors copy this current to the output node v_o and this loop is used to perform indirect compensation with the capacitor (C_c) connected between v_x and v_o nodes. Indirect feedback compensation [25] is achieved by feeding the feedback current indirectly from the output high impedance node of the first stage (v_y). In this technic, the compensation capacitor (C_c) is placed at a low impedance node in the first stage (v_x) allowing indirect feedback current compensation from the output (v_o) to the internal high impedance node of the output of the OPAMP thus obtaining pole splitting and hence frequency compensation. Besides the advantage of eliminating the right-hand plane zero, the operational amplifier with indirect feedback compensation exhibits a significant reduction in the layout area.

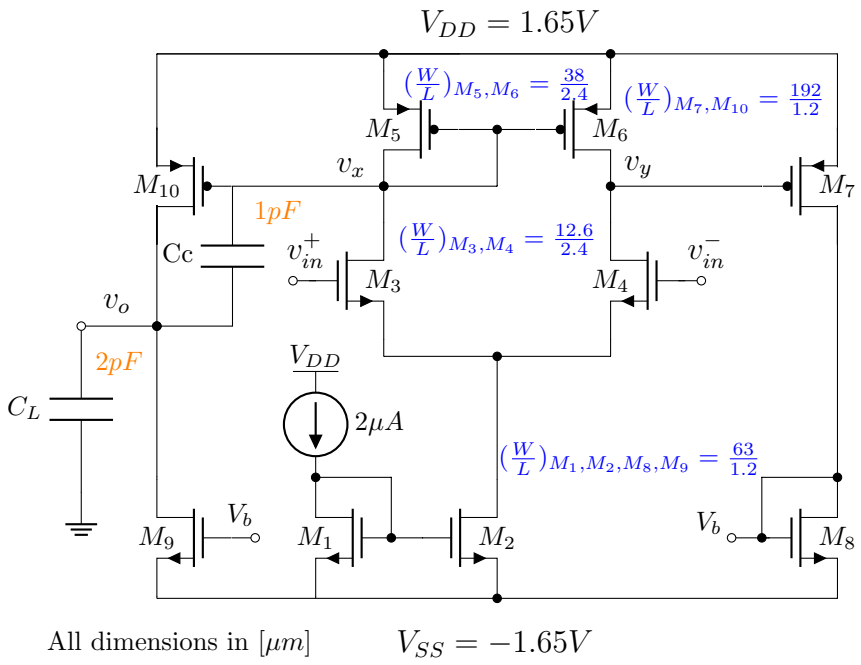


Figure 5. Proposed OPAMP.

The amplifier design process is:

1. We determine the necessary transconductance of differential pair $(gm_{(M_3,M_4)})$ for a GBW = 2 MHz and a lod capacitance(C_L) of 2 pF as shown in Equation (1).

$$gm_{(M_3,M_4)} = GBW \times 2\pi C_L = 25.1\ \mu S \tag{1}$$

2. We find the aspect ratio of transistor N for a V_{Dsat} = 0.08 V, $\frac{\mu_N \times C_{ox}}{2}$ = 57 µA/V^2 = and I_{bias} = 2 µA, as shown in Equation (2).

$$(W/L)_{M_3,M_4} = \frac{I_{bias}}{\frac{\mu_N \times C_{ox}}{2}(V_{Dsat})^2} = 5.4 \tag{2}$$

3. Using Equation (3), we propose an L_{M_3,M_4} = 2.4 µm and obtain a W_{M_3,M_4}.

$$W_{M_3,M_4} = (5.4)(2.4\ \mu m) \approx 12.6\ \mu m \tag{3}$$

4. Due to the difference between $\frac{\mu_N \times C_{ox}}{2}$ = 57 µA/V^2 and $\frac{\mu_P \times C_{ox}}{2}$ = 18 µA/V^2, W_p is calculated using Equation (4).

$$W_{M_5,M_6} = (3.16)(12.6\ \mu\text{m}) \approx 38.4\ \mu\text{m} \tag{4}$$

5. The dimensions of $(W/L)_{M_7,M_{10}}$ = 192 µm/1.2 µm and $(W/L)_{M_8,M_9}$ = 63 µm/1.2 µm are proposed to handle $8I_{bias}$, as shown in Figure 5.
6. Finally, Cc = 1 pF was chosen to obtain a phase margin PM ≈ 60°. The DC gain is determined by Equation (5) if $gm_8 = gm_9$. Equation (6) shows the expression for P_1 (low-frequency pole) and Equation (7) for P_2 (high-frequency pole).

$$A_v = gm_4(r_{04} \parallel r_{06})gm_7(r_{09} \parallel r_{10}) \approx 87\text{dB} \tag{5}$$

$$P_1 = -\frac{1}{(r_{04} \parallel r_{06})[C_L + (C_C + C_{gd10})gm_{10}(r_{09} \parallel r_{10})]} \approx 130\text{Hz} \tag{6}$$

$$P_2 = -\frac{C_L + gm_{10}(r_{03} \parallel r_{05})(C_{gd10} + C_c)}{C_L[C_{gd3} + C_{db3} + C_{db4} + C_{gs5}](r_{03} \parallel r_{05})} \approx 2.2\text{MHz} \tag{7}$$

Figure 5, all transistors operate in the saturation region and results of this amplifier present a DC open-loop gain (OL_{GAIN}) of 87 dB, gain-bandwidth product (GBW) of 2.2 MHz and phase margin of 62° as shown in Figure 6. Experimental voltage offset (V_{offset}) refered to input of 1.2 mV and power consumption of 6.6 µW.

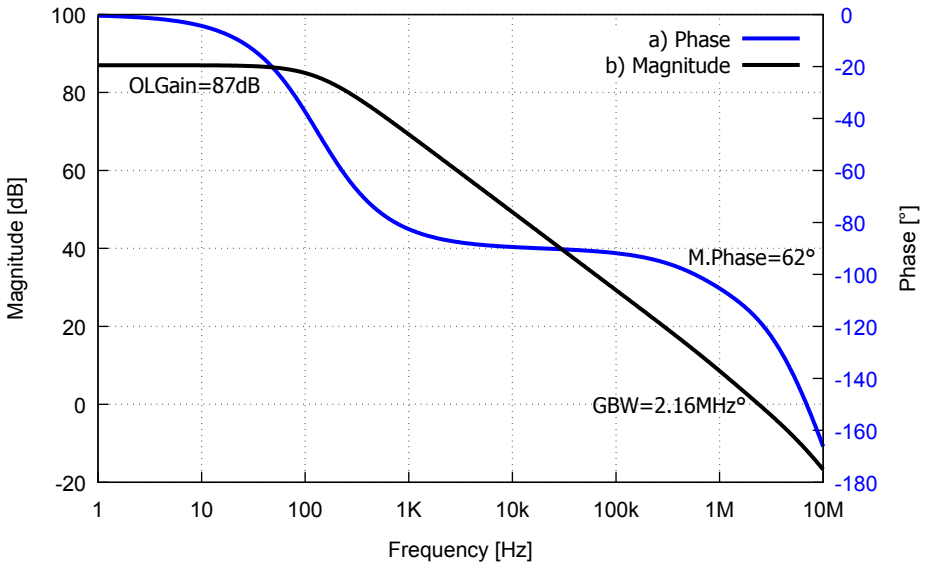


Figure 6. OPAMP frequency response.

3.2. Four-Quadrant Analog Multiplier

The multiplier used for this work is the well-known Gilbert cell [26] shown in Figure 7, which is comprised by 6 transistors operating in the saturation region (M_3–M_8) and a bias current mirror (M_1–M_2).The design of this circuit was proposed using equation 1 for a GBW = 4 MHz and a capacitance of 10 pF due to the load represented by an internal pad, thus obtaining a gm_1 = 251.32 µs. The aspect ratio was obtained by means of Equation (2) with values of V_{Dsat} = 0.1 and current through M_5 = 12.5 µA, obtaining (W/L) = 23. The same Figure 7 shows the transistor sizing and bias conditions. This multiplier presents a gain of 7.4 dB, a GBW of 4 MHz, a linear range of 150 mV and a power consumption of 165 µW. For the transient simulation of this circuit two differential signals were used: a sinusoidal of 100 mVp amplitude at 10 kHz frequency, and a triangular signal of 100 mVp amplitude

at 1 kHz frequency. The output voltage of this multiplier is shown in Figure 8, where a gain of ≈2.5 and a DC level of ≈1.2 V can be seen.

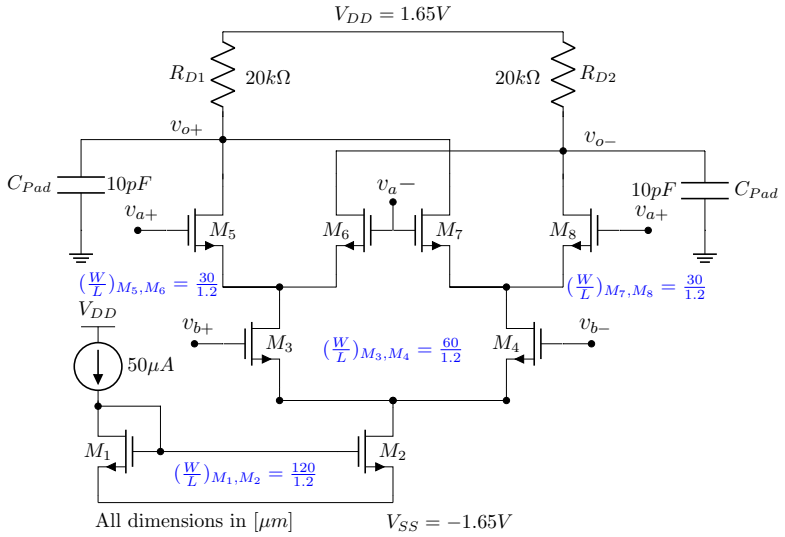


Figure 7. Analog Four-Quadrant Multiplier (MOS Gilbert cell).

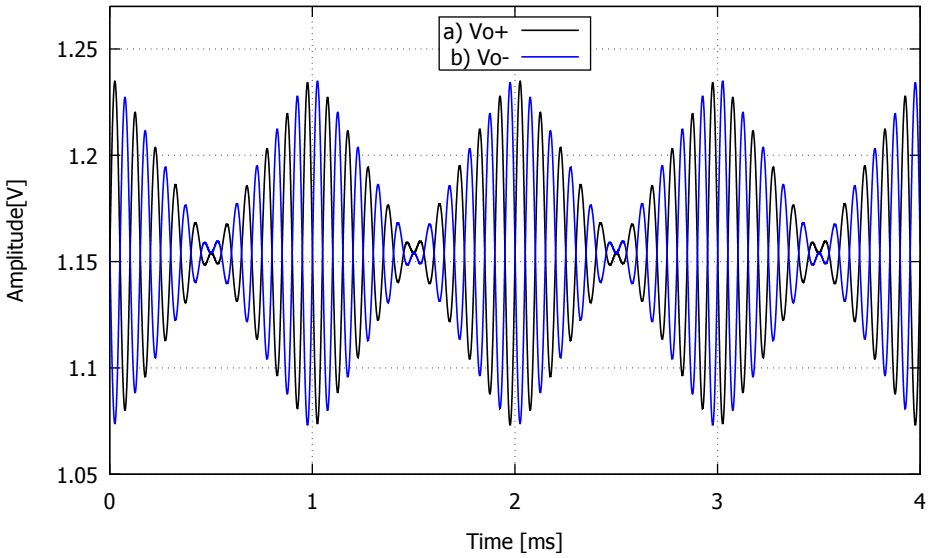


Figure 8. Multiplier transient response.

3.3. Peak Detector

There are a wide variety of peak detectors, which can realize by diodes or by MOS transistors [8,20]. The diode is constituted of 3 structures within a well type N, which is located into the substrate (type P) of the IC; in the well, there is a main P-type diffusion, surrounded by an N-type diffusion ring and enclosed by another P-type diffusion ring as shown in Figure 9. A super diode structure was used for realizing the peak detector. This structure is essential as the threshold voltage of the diode (for silicon Vth = 0.7 V) is divided by the open-loop gain of the OPAMP and reduced to a value close to 0 volts. The operating frequency of the peak detector is determined by the expression $f_c = 1/(6.283 \times R_D C_D)$. If the operating frequency changes, R_D and C_D must be recalculated. The maximum frequency of the AGC is mainly restricted by the OPAMP. Since the 0.5 µm technology does not provide characterized diodes nor their models, it was necessary the diode characterization. The transient response of the peak detector when applying a sine wave signal with a frequency of 1 kHz with different amplitude values,

between 0.15 V–1.2 V is shown in Figure 10. It can be seen that the settling time depends on the signal amplitude. The next block is the filter, which is a simple RC circuit, hence it does not need any discussion. However, this block along with the peak detector determines the maximum operating frequency.

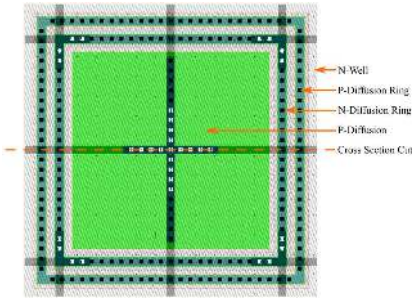


Figure 9. Diode layout.

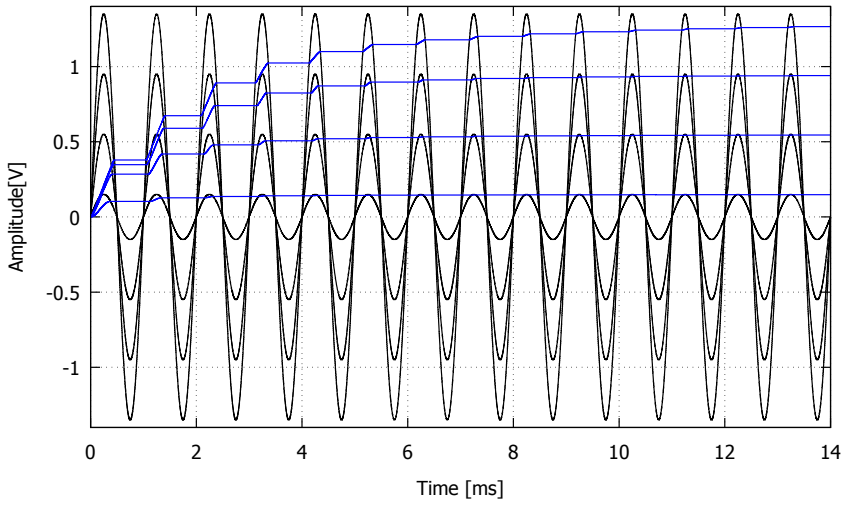


Figure 10. Peak detector transient response.

3.4. Subtractor

A subtractor circuit used as a comparator is shown in Figure 4a. The circuit generates a signal proportional to the difference between V_{REF} and the filter output V_H. This circuit is composed of an OPAMP and two 10 kΩ resistors.

Figure 4b shows the implementation of the single-to-differential (S2D) converter, while Figure 4c shows the differential-to-single circuit (D2S). These blocks are used before and after the analog multiplier because the Gilbert cell requires differential input and output signals. Both blocks are based on the OPAMP circuits discussed in Section 3.1. It can be noticed that the DC level is canceled by using these blocks. Because of the limited dynamic range obtained by the four-quadrant multiplier, it is necessary to attenuate its input signals. This is achieved by modifying the values of the resistors in block S2D. In the same way, block DS2 is also used to amplify the output signal of the multiplier up to a suitable amplitude for the peak detector. In this case, the input/output signals are attenuated/amplified by a factor of 4.

4. Analog AGC Simulation Results

Simulation results of the Analog AGC were obtained using a sinusoidal signal which amplitude varies from 300 mV to 180 mV at a frequency of 1 kHz, as shown in Figure 11 (In the upper and lower of this figure the input and output signal are shown respectively). Settling time is calculated by Equation (8), V_{ref} is a voltage reference, the constant k_{AM} = 2.45 mV indicates linear gain control slope and g_m, C are the transconductance and capacitance of the peak detector. Figure 11, we use

V_{REF} = 500 mV and get a release (R_T) and attack (A_T) time of 220 ms and 5 ms respectively. Under the same input signal conditions and with an increase of C, is obtained a R_T of 32 ms and A_T negligible, as shown in Figure 12. Figure 13 shows the simulation results for a sinusoidal input signal at a frequency of 1 Hz. The AGC controls the output signal at V_{ref} = 220 mV, obtaining a R_T of 6.2 s and A_T negligible. The results can be applied to amplitude control an electrocardiogram (ECG) signal.

$$\tau = \frac{C \times V_{ref}}{k_{AM} \times g_m} \tag{8}$$

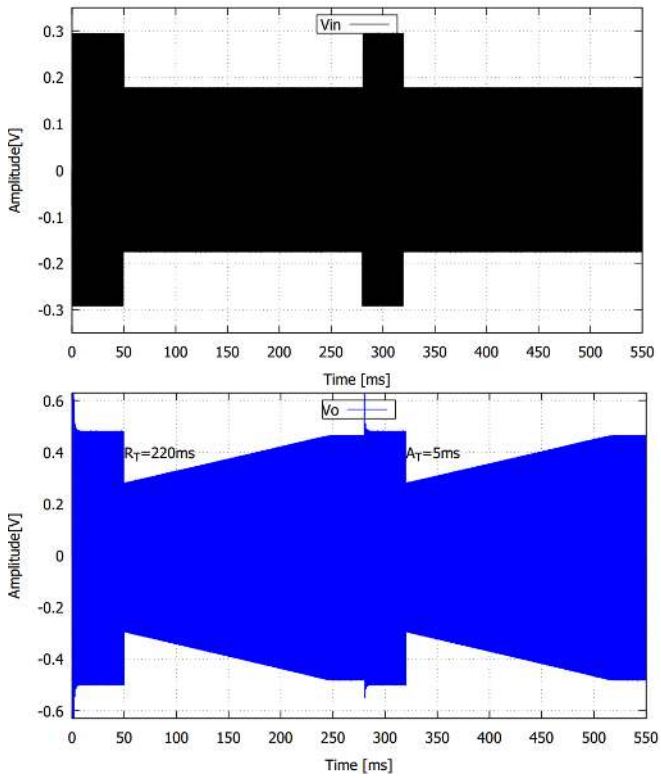


Figure 11. Analog AGC transient response for V_{REF} = 500 mV, with R_T = 200 ms.

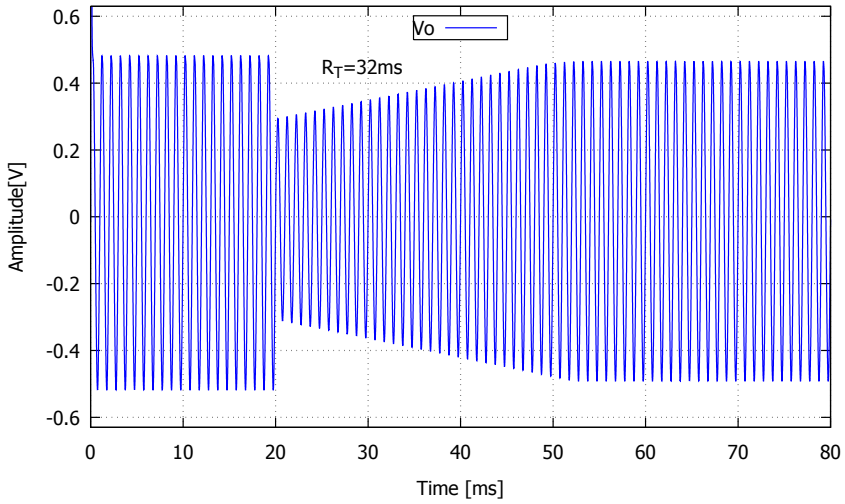


Figure 12. Analog AGC transient response for V_{REF} = 500 mV, with R_T = 32 ms.

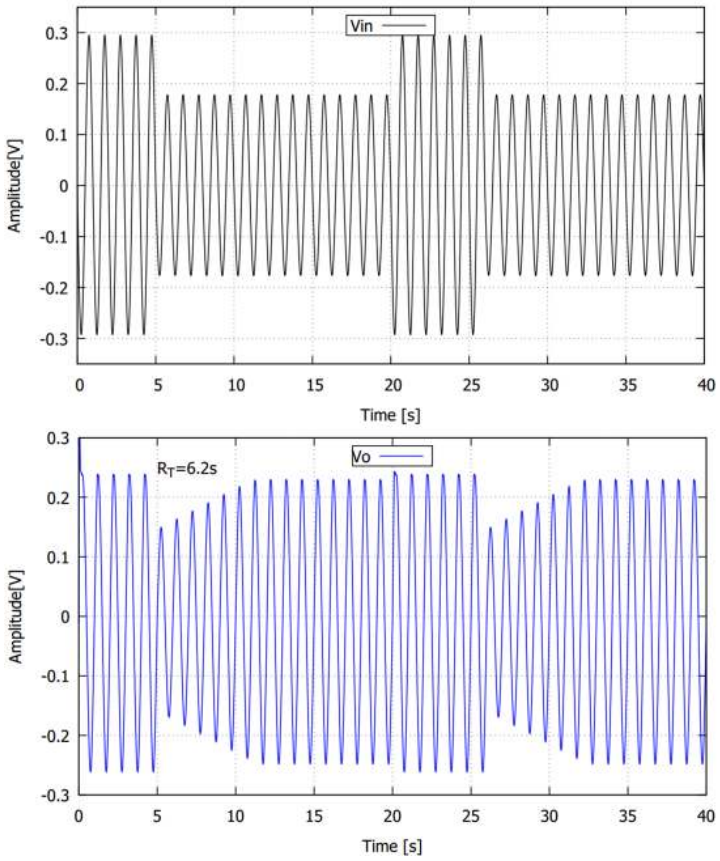


Figure 13. Analog AGC transient response for V_{REF} = 500 mV, with R_T = 6.2 s.

5. Experimental Results and Discussions

Figure 14 shows the microphotograph of the analog AGC fabricated in On-Semiconductor 0.5 µm technology. Section A is the peak detector, 280 µm × 90 µm, section B shows the inverting amplifier (138 µm × 90 µm), section C shows the S2D converter 180 µm × 90 µm, section D is the subtractor circuit 213 µm × 90 µm, section E is the four-quadrant multiplier 87 µm × 88.80 µm and section F shows the D2S circuits with 397 µm × 90 µm. The total dimension of the analog AGC is 508 µm × 317 µm. The experimental results of each block are shown independently.

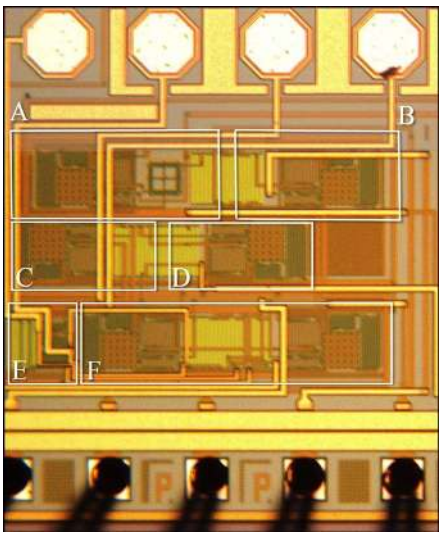


Figure 14. Fabricated circuit.

5.1. Analog Four-Quadrant Multiplier

Operating conditions for this circuit are given in Figure 7. A transient simulation shows similar behavior to the post-layout simulation, seen in Figure 15. Two input signals were used: a triangular and sinusoidal waveform with 400 mV of peak amplitude at 100 Hz and 4 kHz, respectively.

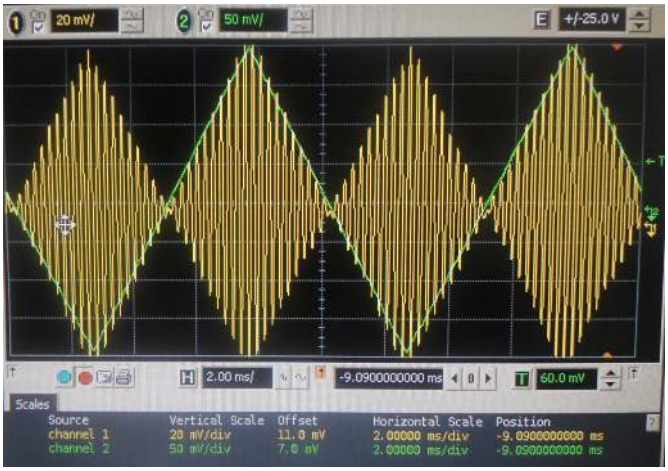
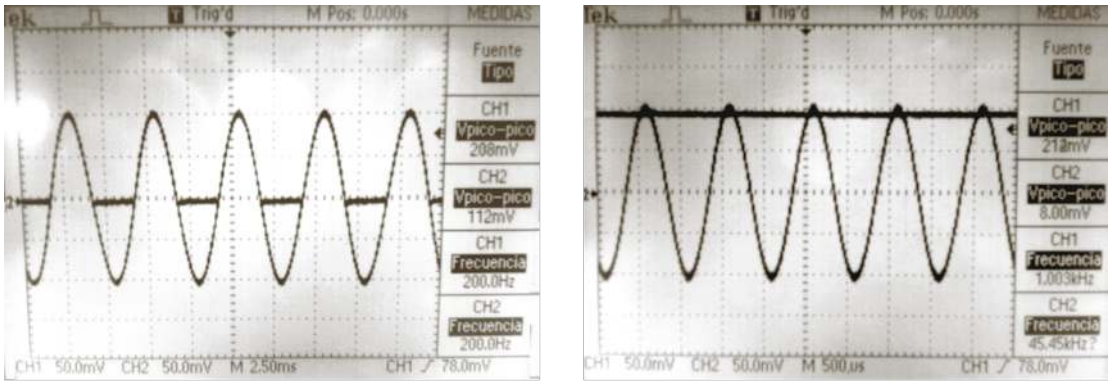


Figure 15. Experimental results of the analog multiplier.

5.2. Peak Detector

The diode was experimentally measured with a Keithley 4200-SCS Semiconductor Characterization System, obtaining a reverse bias current of 10 pA. A dual supply of Vdd = 1.65, Vss = −1.65 V and a bias current Ib = 2 µA were used for the experimental characterization of the peak detector. For the Opamp-Diode configuration, a sinusoidal input signal of 200 mVp at a frequency of 200 Hz was introduced. The obtained result is shown in Figure 16a, where a half-wave rectifier is observed. When an external capacitor is connected at the super-diode output, a peak detector is obtained. Figure 16b shows the peak detector output for a 0.75 V sinusoidal input signal at 1 kHz and an 50 nF capacitance. As expected, the output signal is held at the peak value.



(a) (b)

Figure 16. Experimental results of the peak detector: (**a**) half-wave rectifier and (**b**) peak detector.

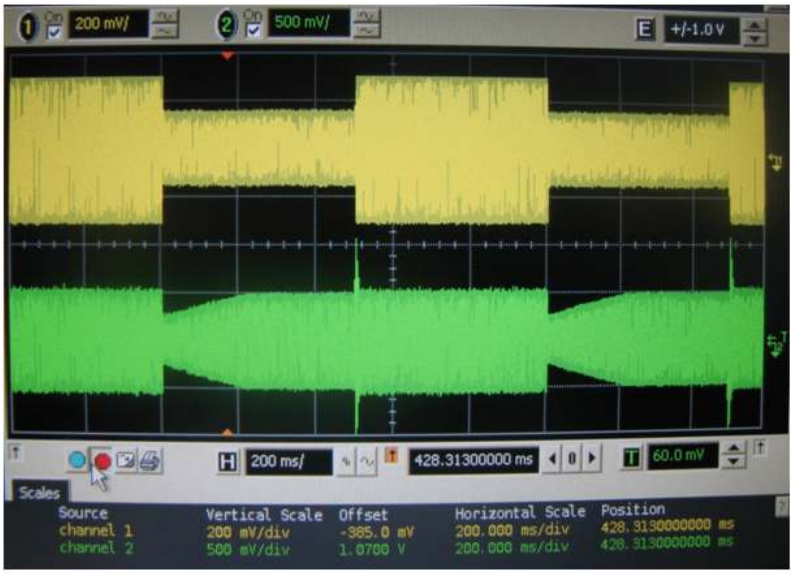
5.3. Complete Analog AGC

The electrical characterization of the analog AGC was performed under the same conditions as the schematic simulation level shown in Figure 4a. In Figure 17a a V_{REF} = 500 mV with a release time of 210 ms and attack time of 10 ms is used while in Figure 17b, V_{REF} is equal to 700 mV with a release time of 200 ms and an attack time of 20 ms is used. Table 2 shows a comparison of simulation and

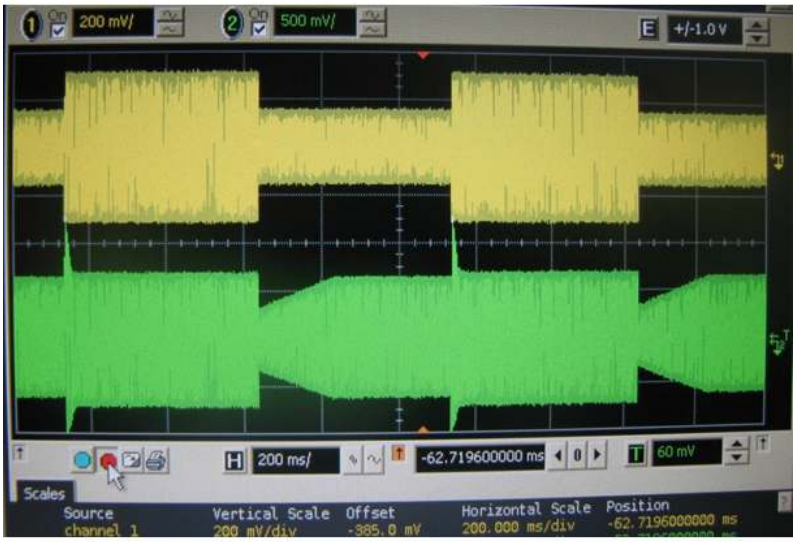
experimental results. A summary of the characteristics of the operation of different AGCs is shown in Table 3. They were used for hearing aids [16], sensor calibration [10], and Bionic Ears [17]. This work presents a lower power consumption, configurable operating frequency, lower consumption of silicon area despite being designed in technology of longer channel length [10,16,17] and reconfigurable frequency of operation, attack time and release.

Table 2. Analog AGC experimental result.

V_{IN} [V]	V_{REF} [V]	Simulations V_{OUT} [V]	Simulations R_T, A_T [s]	Experimental V_{OUT} [V]	Experimental R_T, A_T [s]
300 m, 180 m	500 m	≈500 m	200 m, 1 m	≈500 m	210 m, 10 m
300 m, 180 m	700 m	≈700 m	300 m, 1 m	≈700 m	200 m, 20 m
550 m, 180 m	750 m	≈750 m	430 m, 1 m	≈700 m	350 m, 20 m



(a)



(b)

Figure 17. Analog AGC experimental results by setting: (**a**) V_{REF} = 500 mV and (**b**) V_{REF} = 700 mV.

Table 3. Comparison with others AGC.

Parameter	Kim [16]	Hu [10]	Baker [17]	This Work
Technology	0.18 µm	0.35 µm	1.5 µm	0.5 µm
Power consumption	<71 µW	4.8 mW	32 µW	200 µW
Type AGC	Digital	Analog	Analog	Analog
Vin	12.5 mV/180 mV	40 mV to 72 mV	—	180 mV to 330 mV
V_{ref}	62.5 mV–197.5 mV	97.6 mV	—	500 mV–700 mV
Test frequency	1 kHz	200 kHz	1 kHz	1 kHz
Release time	—	1 ms	70 ms–140 ms	200 ms
Attack time	—	1 ms	1 ms–3 ms	20 ms
Supply voltage	0.9 V	3.3 V	2.8 V	3.3 V
Total die area	—	0.37 mm^2	4.41 mm^2	0.16 mm^2
AGC control	Voltage-mode	Voltage-mode	Voltage-Mode	Voltage-mode
Applications	Hearing aid	Sensor calibration	Bionic Ears	Biomedical signals

6. Conclusions

In this article, we have presented a practical implementation of an Analog Automatic Gain Control in an integrated circuit. The proposed modified Miller type OPAMP with indirect compensation have excellent experimental characteristics such as a reduced area in silicon, better gain band-width, and setting time of the op-amp with a minimal power consumption compared to a class A amplifier, those characteristics improve the attack and release time in the AGC system. The proposed diode had good experimental measurements which allowed the peak detector to function properly. In the experimental results of AGC, we applied analog signals with different amplitudes (180 mV–300 mV) for voltage reference =500 mV, so that the best release time was 210 ms, with 10 ms of attack time. The AGC has a voltage output swing ≈1.2 V, attack and release time can be increased or decreased by the peak detector capacitor and reference voltage can be adjusted for voltages between 100 mV to 1.2 V. The design is simple, occupies a small silicon area of 0.16 mm^2, has power consumption ≈200 µW. According to the characteristics obtained at the experimental level (attack and release time), this AGC can be applied to hearing aid systems [11,12].

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