CMOS Circuit Performance Enhancement by Surface Orientation Optimization

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Abstract

With the advent of novel device structures that can be easily fabricated outside of the traditional (100) plane, it may be advantageous to change the crystal orientation to optimize CMOS circuit performance. The use of alternative surface orientations enhances hole mobility while degrading electron mobility. By optimizing the surface orientation, up to a 15% improvement in gate delay can be expected. This technique is especially attractive in the FinFET device structure, in which orientation optimization can be performed by trading off layout area.

1 Introduction

CMOS circuits have traditionally been fabricated on (100) silicon substrates due to high electron mobility and reduced interface trap density. Hole mobility, however, is low, but can be improved by changing the orientation [1-3]. The potential use of alternative surface orientations has been studied in the past [2,4,5] and shown to improve PFET performance. However, practical application of such a scheme has been limited by the degradation of device reliability due to interface traps. Furthermore, to obtain different orientations, it was necessary to fabricate devices on trench sidewalls [4,5]. Recently, it was reported that with gate dielectrics thicknesses now in the direct-tunneling regime, reliability is no longer dependent on the silicon crystal orientation [6]. This removes the primary limitation of non-(100) surfaces, thus making them a viable option for CMOS circuits. With the potential adoption of novel vertical device structures such as the FinFET [7], which can be fabricated outside of the (100) plane, orientation optimization becomes an intriguing possibility.

In this work, the benefits of adjusting electron and hole mobilities by surface orientation optimization are investigated. By calibrating models to measured mobility data for different orientations [8], mixed-mode device simulation [9] is used to study the tradeoff between NFET and PFET drive currents in terms of gate delay. The simulated device structure is a double-gate MOSFET; similar trends, however, can be expected for bulk MOSFETs. In these simulations, the drift-diffusion carrier transport model was used. At small gate lengths, this model may underestimate on-state current, but can still yield reliable trends.

2 Circuit Performance Enhancement

With non-(100) surface orientations, the electron and hole field-effect mobilities are modified due to asymmetry of the carrier ef-fective masses [1]. By shifting from (100) to (111) or (110) orientations, hole mobility is improved while electron mobility is degraded (Fig. 1), thus presenting a tradeoff between the two carrier types. Despite

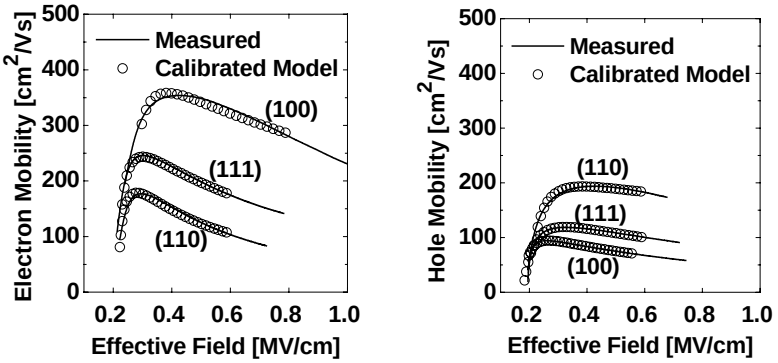

Figure 1: Electron and hole field effect mobilities for different silicon surface orientations with an oxynitride gate dielectric. The calibrated mobility models used in device simulation match well with measured data [8].

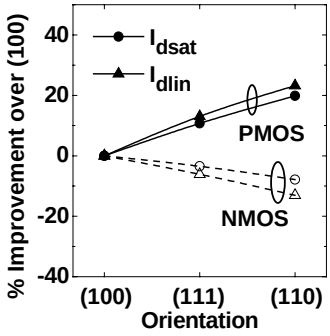

Figure 2: Due to velocity saturation, the impact of mobility on short-channel devices is diminished. L_g=35nm, L_{eff}=25nm, V_{DD}=0.9V, T_{inv}=18Å, T_{body}=10nm, I_{off}=100nA/μm

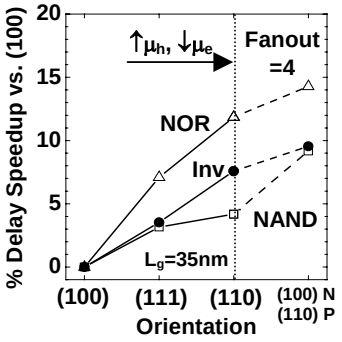

Figure 3: Since PFET enhancement is larger than NFET degradation, an improvement in CMOS gate delay can be achieved, especially for NOR gates due to the series PFET stack.

a change of over a factor of two in mobility, however, velocity saturation limits the change in drain current to 10-20% at 35nm gate lengths (Fig. 2). The effect is larger in the linear region because a smaller lateral electric field reduces the impact of velocity saturation, which makes mobility is more important. Similarly, PFETs experience a larger effect because velocity saturation is less important for holes. As a result, when using (111) or (110) orientations, the PFET enhancement is larger than the NFET deg-radation. Because of this, circuit performance, which depends on the performance of both device types, may be enhanced.

Simulated gate delay trends for inverter, NAND, and NOR gates with FO4 loading are shown in Fig. 3. The (110) orientation shows a large improvement for the NOR gate because the delay of the two series PFETs is very sensitive to an improvement in hole mobility. Only a small improvement is observed for the NAND gate since electron mobility degradation weakens the NFET stack. This emphasizes the notion that orientation optimization will change the way circuits are designed since PFET evaluation stacks become more attractive. An optimum technology would consist of

(100)-oriented NFETs and (110)-oriented PFETs. In this case, the delay improvement can be 9-14% depending on the logic gate.

As gate lengths scale, both series resistance and velocity saturation become more prevalent, which makes mobility adjustment from orientation optimization less important. Scaling the gate length to 18nm (along with other aspects of the technology in accordance with [10]) drops the maximum change in drain current to 5-15% (Fig. 4) and the inverter delay improvement to 6% (Fig. 5). Nevertheless, orientation optimization is still beneficial for sub-20nm gate length devices.

3 FinFET Orientation Optimization

Because the conducting channel of the FinFET lies on the sidewall of a silicon pillar, the surface orientation can be changed by simply rotating the device layout in the wafer plane (Fig. 6). The optimum mobility scheme with (100) NFETs and (110) PFETs, can thus be accomplished by rotating the layout of one of the two device types by 45°. Using simple assumptions for design rules, the area requirements for inverter layouts were estimated for different surface orientation schemes (Fig. 7). The layout area is then the minimum bounding box around the transistor, which is

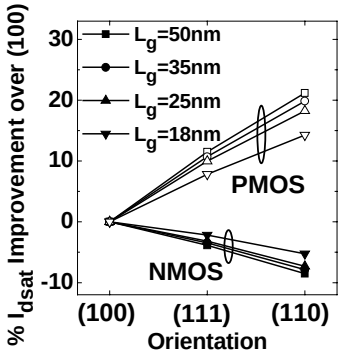

Figure 4: As technology scales, velocity saturation and series resistance becomes more important, thus reducing the effect of mobility.

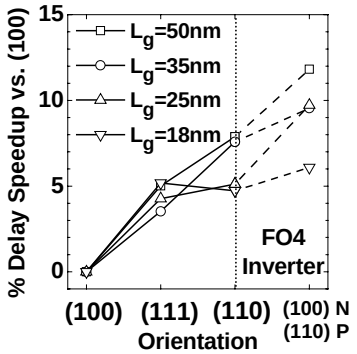

Figure 5: Even at 18nm gate lengths, a noticeable performance improvement can still be obtained by orientation optimization.

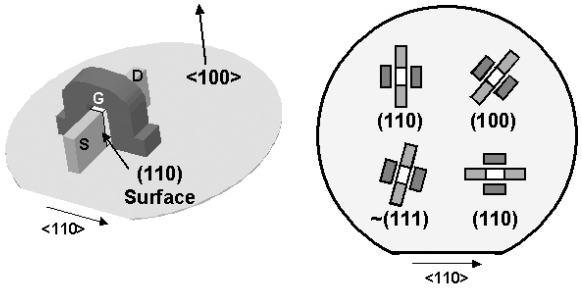

Figure 6: Because the FinFET is vertical in nature, rotation in the plane of a (100) wafer allows for modification of the surface orientation. When the device is oriented parallel or perpendicular to the wafer flat, the device lies in the (110) plane. At a 45° angle, the device is in the (100) plane. An intermediate rotation yields mobilities that approximate the (111) plane.

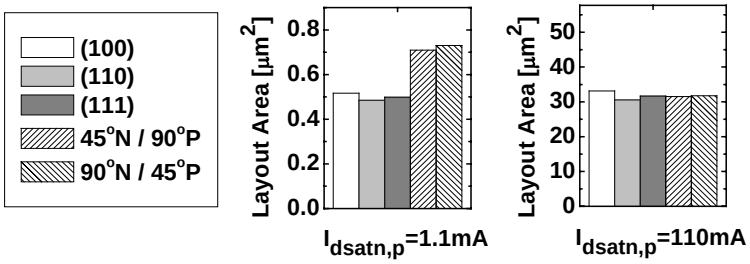

Figure 7: Because of the stronger PFET in (110) and (111) orientations, the layout area required for a FinFET-based inverter can be reduced. For a FinFET technology with (110) PFETs and (100) NFETs, a large area penalty is incurred for a small-sized inverter (1.1mA I_{ds}, W~1.5μm) because one transistor type must be laid out at a 45° angle. This area overhead becomes negligible when the transistor width is large (110mA I_{ds}, W~150μm).

determined by the achievable fin pitch (assumed to be 100nm), fin height (100nm), and the desired device width (number of parallel fins). For 45° devices, fins are placed such that a rectangular bounding box can be drawn. (110) and (111) orientations can improve area efficiency because of the larger PFET current drive per unit width. Schemes that achieve (100) NFETs and (110) PFETs incur an area penalty due to the overhead required for implementation of a device oriented at 45°. For small devices, this penalty is significant (~40%). For large-width devices, this penalty is eliminated since improved current drive per unit width overshadows the area overhead required for the 45° device layout.

4 Summary

The use of alternative surface orientations as a method to improve circuit performance has been investigated by simulation. Because the enhancement in hole mobility is larger than the degradation in electron mobility, an improvement in gate delay can be achieved. A technology that could allow for different orientations for NFETs and PFETs could provide up to a 14% improvement in gate delay at 35nm gate lengths. This margin will shrink as device dimensions scale, but could still be greater than 5% at 18nm gate lengths. This technique is especially attractive in vertical transistor structures such as the FinFET.

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