CMOS-Compatible Surface-Micromachined Suspended-Spiral Inductors for Multi-GHz Silicon RF ICs

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***Abstract*—Fully CMOS-compatible, highly suspended spiral inductors have been designed and fabricated on standard silicon substrate (1∼30 Ω·cm in resistivity) by surface micromachining technology (no substrate etch involved). The RF characteristics of the fabricated inductors have been measured and their equivalent circuit parameters have been extracted using a conventional lumped-element model. We have achieved a high peak Q-factor of 70 at 6 GHz with inductance of 1.38 nH (at 1 GHz) and a self-resonant frequency of over 20 GHz. To the best of our knowledge, this is the highest Q-factor ever reported on standard silicon substrate. This work has demonstrated that the proposed microelectromechanical systems (MEMS) inductors can be a viable technology option to meet the today's strong demands on high-Q on-chip inductors for multi-GHz silicon RF ICs.**

***Index Terms*—High Q, microelectromechanical systems (MEMS) inductor, on-chip inductor, RF MEMS, silicon RF IC, surface micromachining, suspended spiral inductor.**

I. Introduction

As THE operating frequency of recent silicon RF ICs moves to the multi-GHz frequency range, it becomes difficult to achieve affordable Q-factors ($>$15) from on-chip inductors fabricated using conventional thin-film, planar IC processes. Recently, research has been actively carried out to find alternative technology options to address this issue including bulk micromachining [1]–[3], surface micromachining [4]–[12], and electrochemical processes [13]. Most recently, a couple of papers have reported nonconventional on-chip inductors successfully integrated with operational RF circuitries, such as a voltage-controlled oscillator (VCO) [9], [10] and a power amplifier [11]. These on-chip inductors have been fabricated without any substrate etch, utilizing surface micromachining technology. Several variations of surface-micromachined inductors have been investigated including monolithic solenoid inductors [4], [7], [11], suspended spiral inductors [5], [6], [8], [10], and a vertical spiral inductor [12]. Among these, the suspended spiral inductors have shown higher Q-factors on silicon substrates so far [8].

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TABLE I
(a) Physical Dimension With Major RF Performance and
(b) Lumped-Element Parameters of the Fabricated Inductors

Device Number	N number of turns	D (μm) outmost diameter	W width (μm)	P pitch (μm)	L @ 1GHz (nH)	L predicted* (nH)	Peak Q	Peak-Q frequency (GHz)
1	1.5	330	30	80	1.38	1.32	70	6
2	1.25	430	30	80	1.86	1.56	49	3.4
3	2.25	430	30	80	2.59	2.44	38	2.6
4	3.25	430	30	50	4.10	3.74	32	2.2

(a)

Device Number	Ls (nH)	Rs (Ω) f in GHz	Cf (fF)	$Ci1$ (fF)	$Rsi1$ (Ω)	$Csi1$ (fF)	$Ci2$ (fF)	$Rsi2$ (Ω)	$Csi2$ (fF)
1	1.34	$0.27\sqrt{f}$	1.14	11.6	275	1.0	90.5	332	10.2
2	1.77	$0.39\sqrt{f}$	0.82	20.2	193	27.6	92.2	222	21.2
3	2.52	$0.64\sqrt{f}$	0	25.8	230	34.4	160	167	20.3
4	3.90	$0.99\sqrt{f}$	0	40.0	199	43.8	184	148	16.7

(b)

*The predicted L is calculated from [15]

Other previous techniques for improving Q-factors were listed and compared in our earlier publication [7].

Recently, we have reported a new microelectromechanical systems (MEMS) fabrication process developed for RF and microwave applications [14]. This process allows the fabricating of arbitrary-shaped, highly suspended metal microstructures that are fully CMOS-compatible and manufacturable in terms of process stability and structural robustness. In this letter, we newly report the RF performance and model parameters of the suspended spiral inductors fabricated on the standard silicon substrate using our new fabrication technology.

II. Design and Fabrication

In order to evaluate and extract model parameters, various rectangular spiral inductors have been designed and fabricated. Table I lists their number of turns (N), outmost diameter (D), line pitch (P), and line width (W). These inductor structures are suspended by two signal posts of 20 μm in diameter without any additional mechanically supporting posts in order to minimize substrate coupling [8], sacrificing structural robustness. However, we have observed that even a 10 000-μm-long meander line is suspended well by only two signal posts without any structural deformation and instability after being fabricated by using all the standard routine processes such as dipping, rinsing, and blowing. The inductors have been suspended by 50 μm (based on the suggested height in [8]) over the 1∼30 Ω·cm silicon substrate passivated by 1-μm-thick thermal oxide for electrical isolation. The inductors have been made of 10-μm-thick

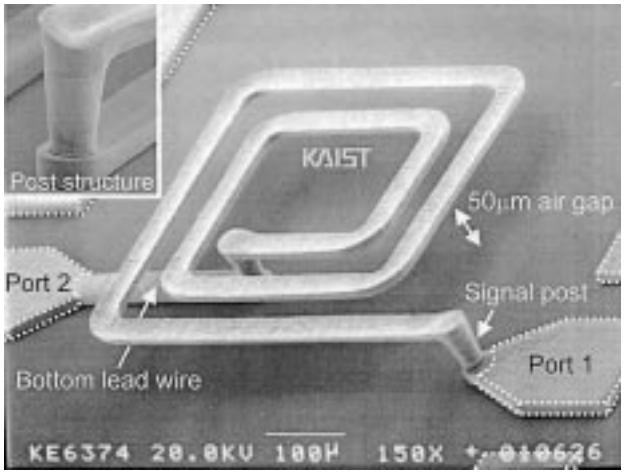

Fig. 1. SEM microphotograph of the highly suspended MEMS spiral inductor fabricated on standard silicon by using a new CMOS-compatible surface micromachining technology. The white dotted line illustrates the open-pad pattern utilized in de-embedding procedure.

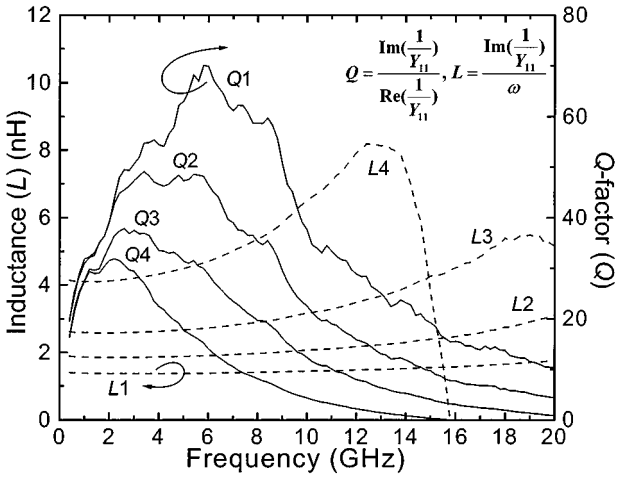

Fig. 2. Measured, de-embedded characteristics of inductance (L) and Q-factor (Q) of the fabricated inductors. The definitions of L and Q used in this work are also shown.

electroplated copper in order to significantly minimize metal ohmic loss and ensure structural robustness. We observed that 5-μm-thick copper inductors were occasionally deformed after the fabrication process.

The proposed fabrication process has utilized a special three-dimensional (3-D) photoresist mold, which is made of a single-coated positive-tone thick-photoresist layer (AZ9260) with a deep recess for signal posts and a shallow recess for suspended inductor structure, utilizing a double exposure (deep and shallow) and a single development [14]. The shallow exposure depth, which will determine the suspension height of the spiral inductor, has been controlled within $\pm$10% process variation, repeatedly. Once the 3-D photoresist mold has been fabricated, the two recess regions can be sequentially filled up with copper by a combination of electroplating, vacuum deposition, and mechanical polishing. Finally, the 3-D photoresist mold has been removed in acetone to release the air-suspended spiral inductor. The process variation in inductor thickness has been measured less than $\pm$15%, which might cause inductance variation of less than $\pm$3% [15]. The overall run-to-run inductance variation has been measured as less than $\pm$5%. All the processes have been completed at low temperature below 120 °C without any substrate etch, making the technology fully CMOS-compatible. More details about the fabrication process can be found in [14].

III. Results and Discussion

Fig. 1 shows the SEM microphotograph of the fabricated inductor, clearly revealing the flat and smooth surface of the suspended inductor together with robust post structure. Due to the excellent planarization capability of the sacrificial photoresist mold, the suspended structure has not shown any imprint of the bottom lead wire on the suspended metal lines, while these imprints can be found in the previous work [5]. For structural robustness, chip-dropping tests have been carried out and have shown no damage in the suspended structure from SEM inspection. Rigorous industrial reliability tests for shock and vibration are being undertaken and will be reported elsewhere.

The on-wafer RF measurement has been performed from 0.2 GHz to 20 GHz using an HP 8510C network analyzer, coplanar GSG probes, a Cascade microwave probe station, and a CS-5 calibration substrate. The calibration has been performed up to the probe tips. The de-embedding of pad parasitics has been carried out with special care since the pads occupy large contact areas on the lossy silicon substrate. These pads are used only for inductor characterization and will not be included in the real on-chip integration. Fig. 1 also illustrates the open-pad pattern (white dotted line) employed in this work. Note that the open-pad pattern excludes the substrate-contact area of the posts and the bottom lead-wire, making the de-embedded data realistic. The pad de-embedding procedure has been done by subtracting measured two-port Y-parameters of the open-pad pattern from those of the pad-embedded inductor [16].

Fig. 2 shows the de-embedded inductance (L) and Q-factor (Q) characteristics of the four sample inductors accompanying with their definitions used in this work. Owing to the thick metal line and sufficient air gap from the lossy substrate, two major losses (ohmic and substrate) have been reduced remarkably. In consequence, we have achieved the highest peak Q-factor ever reported on the standard silicon substrate, which is 70 at 6 GHz with inductance of 1.38 nH (at 1 GHz) and a self-resonant frequency of over 20 GHz. The predicted inductance values listed in Table I has been calculated from [15]. As inductance increases, Q-factor decreases at a given frequency. This is because capacitive coupling increases between the substrate and the longer suspended metal lines, ultimately degrading both the peak Q value and peak-Q frequency simultaneously. All the inductors show fairly flat inductance and high Q-factor ($>$20) up to 5 GHz, which is a desirable characteristic required in today's multi-GHz silicon RF ICs.

The fabricated inductors have been modeled using a conventional on-chip inductor model [17], [18], as shown in Fig. 3. All the model parameters were extracted using HP-EEsof Libra and they are listed in Table I. In this model, Ls and Rs represent the series inductance and resistance, respectively. The metal skin-depth effect is taken into account in Rs. Cf models the

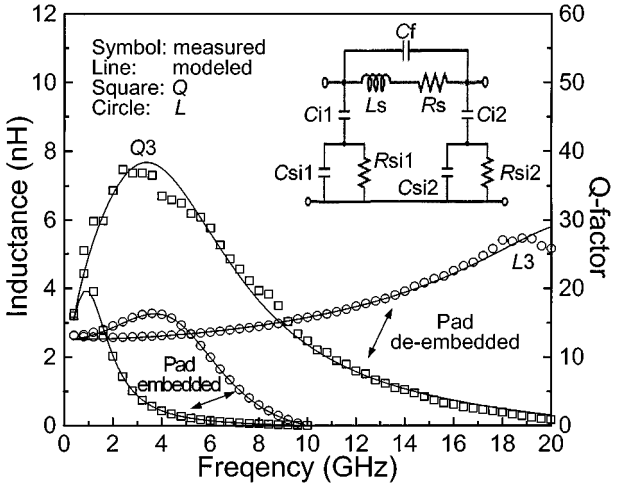

Fig. 3. Measured and modeled, pad-embedded and de-embedded characteristics of the fabricated inductor. The conventional lumped-element model used in this work is also shown.

overlap capacitance between the suspended spiral metal lines and the underlying bottom lead wire, which is negligible in this highly suspended structure as can be seen in Table I. $Ci1$ and $Ci2$ represent the air–gap capacitance between the spiral and the substrate, each of which increases as the length of the spiral increases. Note that $Ci2$ is fairly greater than $Ci1$ for the bottom lead wire. The silicon substrate losses are modeled by $Rsi1$, $Csi1$ and $Rsi2$, $Csi2$.

Fig. 3 shows both measured and modeled characteristics of the sample inductor as well as pad-embedded and de-embedded characteristics. As can be seen in Fig. 3, the conventional model represents L and Q characteristics of the fabricated MEMS inductors very well up to over 10 GHz, which is important for the fabricated MEMS inductors to be utilized in designing MEMS-integrated RF circuits in multi-GHz frequencies.

For a packaging issue, we have tested an encapsulation of the suspended inductor in a transparent silicone encapsulant, which has been spincoated into the finished and freestanding inductors. It is observed that the fabricated suspended structures maintain their original shape without any deformation after encapsulation. More substantial characteristic impact on Q-degradation due to the finite dielectric constant of the encapsulant is now being investigated.

IV. Conclusion

Highly suspended MEMS spiral inductors have been fabricated and fully characterized with a conventional lumped-element model. The fabricated inductors have shown high Q-factors of up to 70 on standard silicon substrate in multi-GHz frequency ranges. The fabrication technology developed in this work is fully CMOS-compatible and does not involve any substrate etch. We believe the integration of these inductors onto the conventional RF circuits will lead a quantum leap for next-generation high-performance single-chip silicon RF ICs.

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