CMOS differential difference current conveyors and their applications

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Abstract: The authors present a new versatile circuit building block called a differential difference current conveyor (DDCC). An IC technique for implementing the DDCC is also presented. The DDCC-based frequency-selective circuits and nonlinear building blocks such as multiplier, squarer and square rooter are developed. Experimental results are given to demonstrate the feasibility of the proposed techniques, and they show that DDCC-based circuits offer a competitive design choice to CCII-based and DDA-based circuits.

1 Introduction

Current-mode circuits have begun to emerge as an important class of circuits, with properties of accuracy, good high-frequency performance, and versatility in a wide range of applications. Since the second generation current conveyor (CCII) was introduced in 1970 [1], several applications, such as amplifiers, filters, oscillators, and signal-processing circuits using CCII have been proposed in the literature [2–5]. Recently, the differential difference amplifier (DDA) was proposed [6] and numerous applications have been found [7–9]. Because of the high input impedance and arithmetic operation capability of the DDA, the component count of the circuits using DDAs can be lower than that of the circuits using CCII.

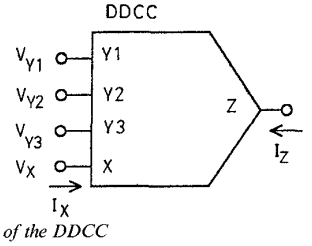

Fig. 1 *Symbol of the DDCC*

The advantages of the CCII and DDA will now be combined and extended to a new building block, called a differential difference current conveyor (DDCC). A DDCC, whose symbol is shown in Fig. 1, is a five-terminal network with terminal characteristics described by

$$I_{Y1} = I_{Y2} = I_{Y3} = 0 \tag{1a}$$

$$V_X = V_{Y1} - V_{Y2} + V_{Y3} \tag{1b}$$

$$I_Z = \pm I_X \tag{1c}$$

where the plus and minus sign indicate whether the conveyor is configured as an inverting or noninverting circuit, termed DDCC– or DDCC+.

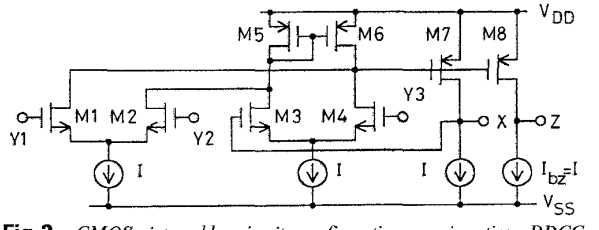

Fig. 2 *CMOS integrable circuit configuration: noninverting DDCC (DDCC+)*

2 Circuit description

The proposed CMOS DDCC+ circuit is shown in Fig. 2. The circuit structure of this CMOS DDCC is similar to that of the CCII+ in [10] and to the DDA realisation in [6]. The input transconductance elements are realised with two differential stages (M1 and M2, M3 and M4). The high-gain stage is composed of a current mirror (M5 and M6) which converts the differential current to a single-ended output current (M7). The output voltage of this amplifier can be expressed as

$$V_X = A_0[(V_{Y1} - V_{Y2}) - (V_{G3} - V_{Y3})] \tag{2}$$

where A_0 is the open-loop gain of the amplifier and V_{G3} is the gate voltage of M3. Negative feedback was then applied from the output node of the gain stage (node X) to the input node (gate of M3). If the open-loop gain of the amplifier is much larger than one, the relationship between the four input terminal voltages can be obtained as

$$V_X = \frac{A_0}{A_0 + 1}(V_{Y1} - V_{Y2} + V_{Y3}) \cong V_{Y1} - V_{Y2} + V_{Y3} \tag{3}$$

The output terminal Z is constituted with a current source I_{bz} and the transistor M8 which duplicates the current of the transistor M7. It can be clearly seen that both I_X and I_Z flow simultaneously towards or away from the DDCC. Therefore, the circuit in Fig. 2 realises a DDCC+.

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Fig. 3 shows the negative version of a DDCC or a DDCC–, which is directly adapted from the circuit in Fig. 2. The current mirror formed by M9 and M10 changes the direction of the output current at terminal Z.

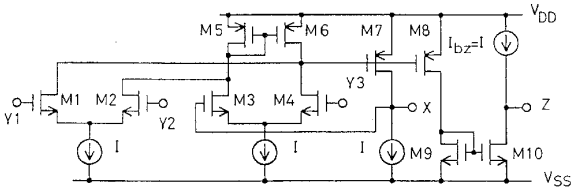

Fig.3 *CMOS integrable circuit configuration: inverting DDCC (DDCC–)*

3 Circuit performance analysis

In the discussion so far, we have assumed that the current mirrors have unity gain, and transistors are perfectly matched. However, in practical realisations, several nonidealities must be present. The major factors we will consider here are finite transconductance g_m of the transistors, and transistor mismatch.

The relationship between V_{Y1}, V_{Y2}, V_{Y3} and V_X can be obtained using small-signal analysis. The transistors in Fig. 2 are replaced by appropriate equivalent circuits and the node equations can be derived. To simplify discussion, the body effect has been neglected and the two differential pairs are assumed to be identical. Then, by solving the equations, we obtain

$$V_X \approx \frac{g_{m7}g_{meq}}{g_{m7}g_{meq} + (g_{d12} + g_{d34} + g_{d6})(g_{d7} + g_{dI})} \times (V_{Y1} - V_{Y2} + V_{Y3}) \quad (4)$$

with

$$g_{meq} = \frac{2g_{m1}g_{m2}}{g_{m1} + g_{m2}} = \frac{2g_{m3}g_{m4}}{g_{m3} + g_{m4}}, \quad g_{dij} = \frac{2g_{di}g_{dj}}{g_{di} + g_{dj}}$$

where g_{di} and g_{mi} denote the drain conductance and transconductance of transistor M_i, respectively, and g_{dI} is the drain conductance of the current source. It is clear that the voltages at port Y1, Y2, and Y3 will be accurately transferred to port X only if $g_{m7}g_{meq} >> (g_{d12} + g_{d34} + g_{d6})(g_{d7} + g_{dI})$.

Similarly, the terminal impedance looking into X can be derived by setting V_{Y1}, V_{Y2}, and V_{Y3} to zero, applying a test voltage V_X at node X, and calculating the current I_X. The result is

$$r_X \approx \frac{(g_{m3} + g_{m4})(g_{d12} + g_{d34} + g_{d6})}{2g_{m3}g_{m4}g_{m7}} \quad (5)$$

The terminal impedance at Z can also be derived as

$$r_Z \approx \frac{1}{g_{d8} + g_{dI}} \quad (6)$$

The resistance can be further increased if a Wilson current mirror or a cascode current mirror is employed.

For high-frequency operation, the major limitation is due to the stray capacitances at terminal X. The high-frequency response can be expressed in terms of V_{Y1}, V_{Y2}, V_{Y3} and V_X as

$$\frac{V_X}{V_{Y1} - V_{Y2} + V_{Y3}} \approx \frac{g_{m7}g_{meq}}{g_{m7}g_{meq} + (g_{d12} + g_{d34} + g_{d6})(g_{d7} + g_{dI})} \frac{1}{\tau_1 s + 1} \quad (7)$$

with

$$\tau_1 = \left[C_{gs7} + C_{gs8} + C_{gd8}\left(1 + \frac{g_{m8}}{g_{dI} + g_{d8}}\right) + 2C_{gd6}\right] \times \left(\frac{1}{g_{d12} + g_{d34} + g_{d6}}\right)$$

where C_{gdi} and C_{gsi} are the gate-to-drain capacitance and gate-to-source capacitance of device M_i, respectively. The pole frequency is quite low and will be the dominant frequency limiting factor of the circuit.

The input offset voltage (V_{os}) is defined as the differential input voltage required to cause the voltage across a resistor between terminal X and ground to be exactly zero. Large signal analysis is performed to solve the node equations. Then the offset voltage can be obtained as

$$V_{os} = (V_{T2} - V_{T1} + V_{T3} - V_{T4}) - \sqrt{\frac{I}{K_1 + K_2}}\left(\frac{K_2 - K_1}{K_2 + K_1}\right) - \sqrt{\frac{I}{K_3 + K_4}}\left(\frac{K_3 - K_4}{K_3 + K_4}\right) \quad (8)$$

where V_{Ti} and K_i are the threshold voltage and the transconductance parameter of the device M_i, respectively. The first term is due to the mismatch among the threshold voltages, which is bias-current independent and is a strong function of process cleanliness and uniformity. The second term is caused by geometrical mismatch and can be reduced by increasing (W/L) or reducing bias current I.

The input signal range is quite limited due to the use of simple differential pairs as input stage, it can be improved by using the wide range linear V–I converter as discussed in [7] or some other techniques.

4 Nonlinear circuit applications

The DDCC-based nonlinear building blocks including multiplier, squarer and square rooter are presented in the following sections.

4.1 Differential squarer

The drain current of a MOS transistor biased in the nonsaturation region can be expressed by

$$I_D = K\left[2(V_{GS} - V_T)V_{DS} - V_{DS}^2\right] \quad (9)$$

with

$$K = \frac{1}{2}\mu C_{OX}\frac{W}{L}$$

where V_T is the threshold voltage, W and L are channel width and length, respectively, μ is the effective channel mobility, C_{OX} is the gate oxide capacitance per unit area.

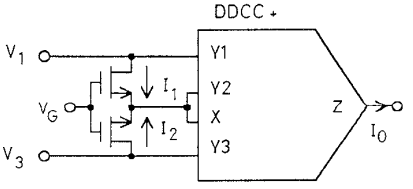

Fig.4 *Circuit of the proposed squarer*

A differential squarer with output current I_O can be constructed as shown in Fig. 4. Assuming the pair of the transistors in Fig. 4 are well matched and V_G is high enough to ensure that both transistors operate in triode region, the transfer function of the squarer can

be derived as

$$I_o = -(I_1 + I_2)$$
$$= -K\left[2\left(V_G - \frac{V_1+V_3}{2} - V_T\right)\left(V_1 - \frac{V_1+V_3}{2}\right) - \left(V_1 - \frac{V_1+V_3}{2}\right)^2\right]$$
$$- K\left[2\left(V_G - \frac{V_1+V_3}{2} - V_T\right)\left(V_3 - \frac{V_1+V_3}{2}\right) - \left(V_3 - \frac{V_1+V_3}{2}\right)^2\right]$$
$$= \frac{K}{2}(V_1 - V_3)^2 = K_s(V_1 - V_3)^2 \quad (10)$$

where K_s is the squarer constant. The operation constraint of this circuit is

$$V_1, V_3 \leq V_G - V_T \quad (11)$$

It should be noted that this circuit uses only one DDCC, but a similar circuit using CCII or DDA always needs two components. On the other hand, the body effect of both transistors will be cancelled, so their substrate and source do not have to be connected together. If a DDCC– is used in this circuit, a similar squarer can be obtained with

$$I_o = -\frac{K}{2}(V_1 - V_3)^2 \quad (12)$$

Therefore, the squarer constant can be either positive or negative. The symbols of both types of squarer are shown in Fig. 5.

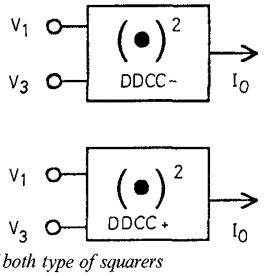

Fig.5 *Symbol of both type of squarers*

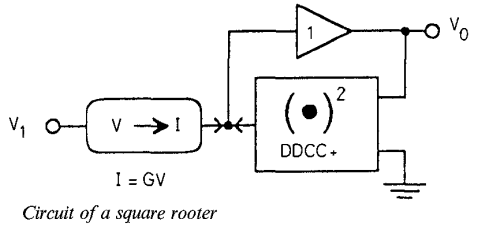

Fig.6 *Circuit of a square rooter*

4.2 Square rooter

We can synthesise a square rooter circuit using the proposed squarer and a linear voltage-to-current (V–I) converter. A linear V–I converter can be easily implemented using a CCII or a DDCC. Consequently, a simple square rooter circuit can be constructed as shown in Fig. 6. Routine circuit analysis yields

$$GV_1 + K_S V_o^2 = 0$$

or

$$V_o = \sqrt{-\frac{G}{K_s}V_1} = \sqrt{\left|\frac{G}{K_S}\right|}\sqrt{|V_1|} = K_R\sqrt{|V_1|} \quad (13)$$

for $V_1 G < 0$

where G is the transconductance of the V–I converter, K_R is the square rooter constant. For the sake of stability, the output voltage should be negative. Since the squarer input terminals are not high impedance nodes, a voltage buffer is needed.

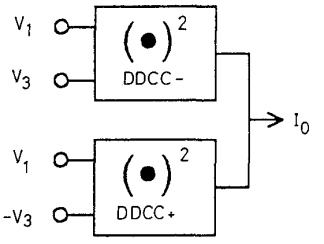

Fig.7 *Proposed multiplier circuit using squarer*

4.3 Multiplier

A threshold-independent four-quadrant multiplier can be implemented using the proposed squarer as shown in Fig. 7. The square-difference technique is used to construct this circuit and its transfer characteristics can be obtained as

$$I_o = \left[\frac{K}{2}(V_1+V_3)^2 - \frac{K}{2}(V_1-V_3)^2\right] = 2KV_1V_3 = K_M V_1 V_3 \quad (14)$$

where K_M is multiplier constant. The operation constraint of the multiplier is

$$V_1, |V_3| \leq V_G - V_T \quad (15)$$

If we exchange the DDCC type of squarer, a similar multiplier can be obtained with

$$I_o = -2KV_1V_3 \quad (16)$$

Therefore, the sign of K_M can be either positive or negative.

It should be noted that this circuit is simpler than the DDA-based multiplier shown in [7] and CCII-based multiplier shown in [4]. The input signals V_1 and V_3 both connect to the drain/source of the transistors, so it is not necessary to use additional circuits to synthesise the '$V_G + V_1$' signal at the gate of the transistors in the circuits of multipliers shown in [4, 7].

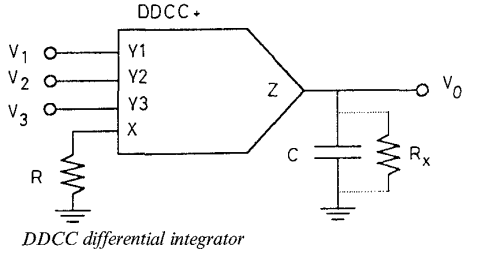

Fig.8 *DDCC differential integrator*

5 DDCC-based frequency selective circuits

5.1 Differential integrator

Differential integrators are key components in many frequency-selective analogue networks such as filters and oscillators. Fig. 8 shows a DDCC-based lossless differential integrator (excluding R_X). The input impedance of the circuit is quite high, and there is no need to match passive components. Both the resistor and the capacitor are grounded, so it is simpler and easier to implement using MOS techniques. The output of the circuit can be derived as

$$V_o = \frac{V_1 - V_2 + V_3}{sRC} \quad (17)$$

A lossy integrator can be achieved by connecting a resistor R_X across the capacitor in a lossless integrator. The resultant output is then

$$V_o = \frac{1/RC}{s + 1/R_X C}(V_1 - V_2 + V_3) \tag{18}$$

5.2 DDCC-based filters

In system level applications, DDCC-based filters can be built by using the basic blocks discussed in previous sections. A DDCC-based voltage-mode biquad filter can be constructed by cascading a lossy integrator and a lossless integrator, as shown in Fig. 9. If the DDCCs

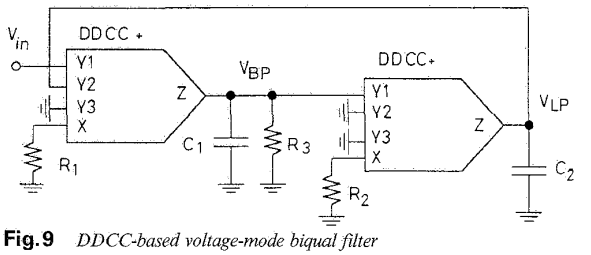

Fig. 9 *DDCC-based voltage-mode biquad filter*

are assumed to be ideal, the transfer functions at the bandpass and lowpass outputs are given by, respectively,

$$\frac{V_{BP}}{V_{in}} = \frac{\dfrac{s}{R_1 C_1}}{s^2 + \dfrac{1}{R_3 C_1}s + \dfrac{1}{R_1 R_2 C_1 C_2}} \tag{19}$$

$$\frac{V_{LP}}{V_{in}} = \frac{\dfrac{1}{R_1 R_2 C_1 C_2}}{s^2 + \dfrac{1}{R_3 C_1}s + \dfrac{1}{R_1 R_2 C_1 C_2}} \tag{20}$$

so that

$$\omega_o = \frac{1}{\sqrt{R_1 R_2 C_1 C_2}} \quad \text{and} \quad Q = R_3\sqrt{\frac{C_1}{R_1 R_2 C_2}}$$

A DDCC-based current-mode biquad filter can also be constructed by paralleling grounded resistor, capacitor and DDCC simulated inductor, as shown in Fig. 10.

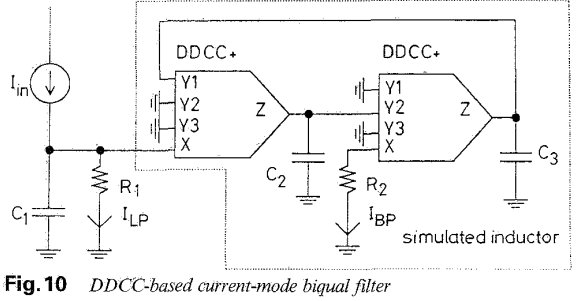

Fig. 10 *DDCC-based current-mode biquad filter*

The transfer functions can easily be derived as

$$\frac{I_{BP}}{I_{in}} = \frac{\dfrac{1}{C_2 R_2}s}{s^2 + \dfrac{C_1}{R_2 C_2 C_3}s + \dfrac{1}{R_1 R_2 C_2 C_3}} \tag{21}$$

$$\frac{I_{LP}}{I_{in}} = \frac{\dfrac{1}{R_1 R_2 C_2 C_3}}{s^2 + \dfrac{C_1}{R_2 C_2 C_3}s + \dfrac{1}{R_1 R_2 C_2 C_3}} \tag{22}$$

so that

$$\omega_o = \frac{1}{\sqrt{R_1 R_2 C_2 C_3}} \quad \text{and} \quad Q = \frac{1}{C_1}\sqrt{\frac{R_2 C_2 C_3}{R_1}}$$

6 Experimental results

To verify the theoretical results of the CMOS DDCC and the proposed applications, CMOS transistor arrays CD4007 are used to implement the DDCC circuits in Figs. 2 and 3. The parameters of this DDCC circuit are summarised in Table 1. The supply voltage used in the experiments is quite high (+7.5V and −7.5V) because discrete components are used. However, the proposed circuits can also operate at lower voltage. Fig. 11 shows simulation results of a DDCC inverter whose supply voltage is +2.5V and −2.5V. The input signal is a 1kHz sinusoidal wave applied at port Y2, port Y1 and Y3 are connected to ground, and the resistances at port X and Z are 10kΩ and 5kΩ, respectively. The experimental results are described below.

Table 1: Summary of the DDCC parameters

Parameters	Experimental results
Bias current (μA)	720
V_{DD} and V_{SS} (V)	7.5 and −7.5
Voltage transfer ratio (V_X/V_1, V_2, V_3)	0.99[a]
Current transfer ratio (I_z/I_x)	0.94[a]
Bandwidth (MHz)	2.2[a]
Input common mode range (V)	−1.35 to 1.3[b]
Output swing (V)	−5.2 to 4.4[c]
r_z and r_x	47Ω and 2.2MΩ
Slew rate (V/μs)	8.71[b]
Power consumption (mW)	60

[a] measured with a load resistor (R_L = 1kΩ) at port X and port Z
[b] measured with a load capacitor (C_L = 220nF) at port X
[c] measured with a load resistor (R_L = 10kΩ) at port Z

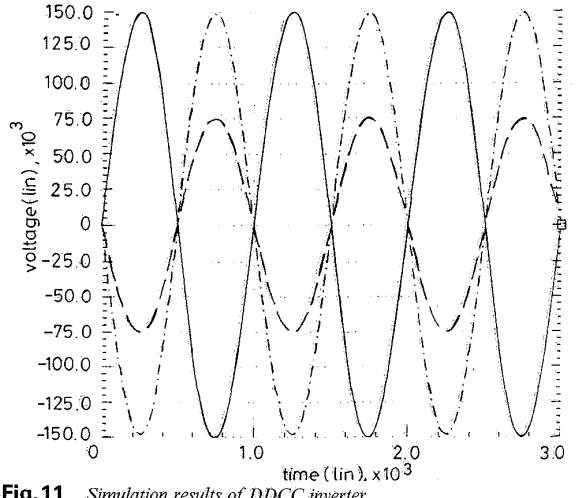

Fig. 11 *Simulation results of DDCC inverter*

6.1 Squarer, square rooter and multiplier

The proposed squarer circuit as presented in Fig. 4 is implemented. The observed waveforms are shown in Fig. 12. The input signals V_1 and V_3 are 10kHz sinusoidal waves with 180° phase difference, V_G is connected to V_{DD} (+7.5V) and a load resistance of 2kΩ is

connected at port Z. The square rooter, as shown in Fig. 6, is also implemented. The *V–I* converter used in this experiment is constructed using a DDCC+ with Y1 being the input terminal, Y2 and Y3 are connected to ground and a 2kΩ resistor is connected at port X. A triangular waveform varying from –500mV to 0V at a frequency of 10kHz is applied to the input terminal of the *V–I* converter. The time-domain response is shown in Fig. 13. The proposed multiplier, as shown in Fig. 7, is also implemented. The DC transfer curves are shown in Fig. 14, where V_1 is a 1kHz triangular waveform varying between –200mV and +200mV and V_3 is a DC signal varied between –0.5V and 0.5V in 0.2V steps. It is well known that a four-quadrant multiplier can be used as a modulator. Fig. 15 shows the modulation results, where two 1V peak-to-peak sinusoidal signals with different frequencies (1kHz and 16kHz) are applied to the multiplier input terminals and a load resistance of 2kΩ is connected at the output port.

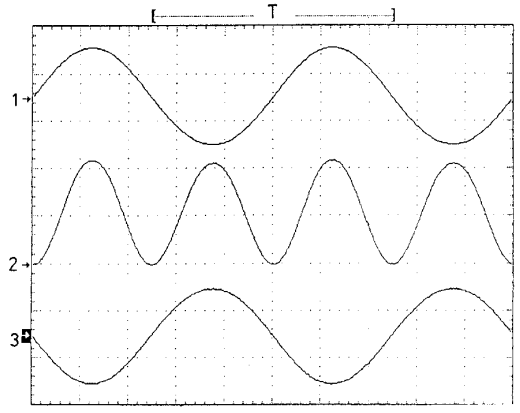

Fig. 12 *Experimental results of the squarer*
Upper and lower traces are input of the squarer V_1 and V_3, respectively, middle trace is output of the squarer
The horizontal scale is 20μs/div and vertical scale is 500mV/div

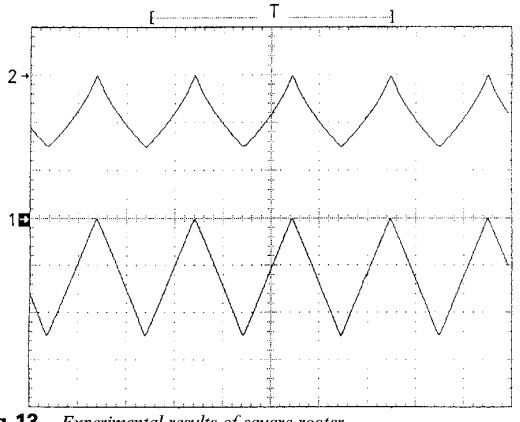

Fig. 13 *Experimental results of square rooter*
Upper trace (500mV/div), output of the square rooter
Lower trace (200mV/div), input of the square rooter
The horizontal scale is 50μs/div

6.2 Voltage-mode and current-mode biquad filter

The voltage-mode and current-mode biquad filters shown in Figs. 9 and 10 are both implemented. With $R_1 = R_2 = R_3 = 430\Omega$, $C_1 = C_2 = 22$nF in the voltage-mode biquad filter, and $R_1 = R_2 = 3\text{k}\Omega$, $C_1 = C_2 = C_3 = 47$nF in the current-mode biquad filter, the measured frequency responses are shown in Figs. 16 and 17, respectively, where both experimental results and theoretical curves are presented.

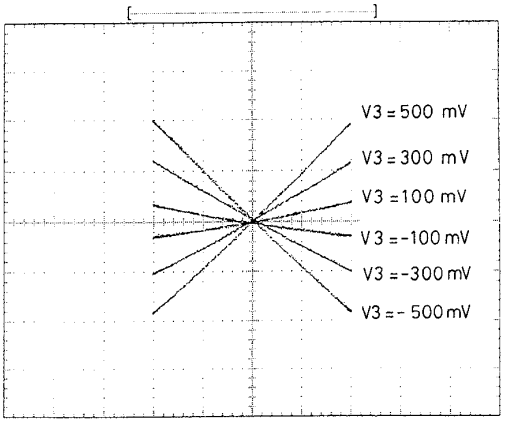

Fig. 14 *DC transfer curves of the multiplier*
Horizontal and vertical scales are 100mV/div

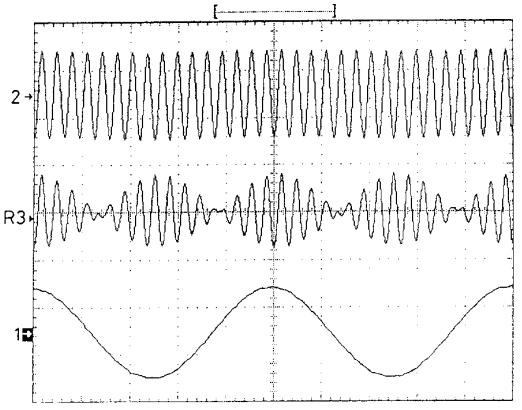

Fig. 15 *Modulation function of the multiplier*
Upper trace, 16kHz (500mV/div)
Lower trace, 1kHz (500mV/div)
Middle trace, modulation output (250mV/div)
Horizontal scale is 200μs/div

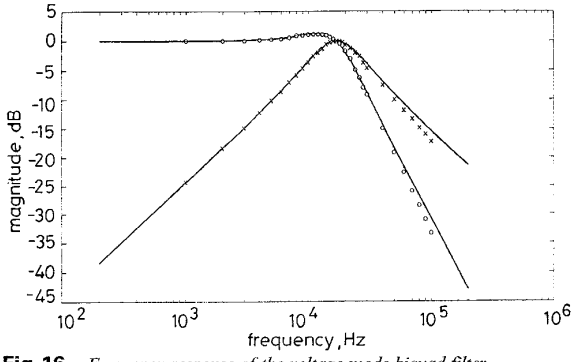

Fig. 16 *Frequency response of the voltage-mode biquad filter*
——— theoretical
○○○○ VLP experiment
×××××× VBP experiment

7 Conclusions

Integrable positive and negative DDCCs are presented. It should be noted that the DDCC is a circuit similar to a DDA at the input side and a CCII at the output side. Consequently, one is able to design DDCC-based circuits which combine the properties of DDAs, such as high input impedance, low output impedance and low component count, with the higher usable gain, accuracy and bandwidth of the CCII.

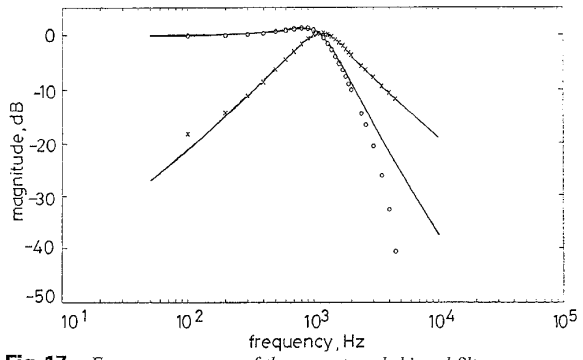

Fig. 17 *Frequency response of the current-mode biquad filter*
——— theoretical
○○○○ VLP experiment
×××××× VBP experiment

Several integrable nonlinear building blocks using DDCCs and DDCC-based frequency selective circuits are also introduced. To verify the feasibility of proposed circuits, DDCC constructed by discrete transistor arrays (CD4007) are used in the experiments and several applications are demonstrated experimentally. The measurement results clearly verify the feasibility of our proposed application circuits using DDCCs.

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