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CMOS LOW NOISE AMPLIFIER FOR MICROSTRIP READOUT DESIGN AND RESULTS

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ABSTRACT

A low noise preamplifier and shaper chip has been designed and built in 1.5 μm CMOS technology to be used for readout of Si μ-strip detectors. The chip is optimized w.r.t. noise. Measurements on the performance of the prototype chip are presented. A noise performance of ENC = 160 e^- + 12 e^- / pF has been achieved.

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1. INTRODUCTION

The application of Si microstrip detectors for position and energy measurement in high energy physics experiments becomes increasingly important since they were first used about 10 years ago for heavy flavour searches in fixed target experiments [1,2]. In particular, their potential as high precision vertex detectors around high energy colliders [3], both for e^+e^- and p–p machines, has initiated further development of high performance detectors and associated VLSI readout electronics.

With the introduction into experiments of Si strip detectors with readout on both sides, taking signals from both pn junction strips and n^+ strips, the requirements on the performance of integrated preamplifiers has become more stringent. Examples where improved noise performance of the preamplifier is required would be :

a) The use of Landau correlations in the case of multihit events to associate signals on both sides of the detector uniquely to a particle.

b) Optimal spatial resolution for particles traversing the detector under a large angle.

The first generation of VLSI readout chips [4] has a noise performance which allows the detection of minimum ionizing particles (MIP giving 25,000 e^- in 300 μm Si) with signal to noise ratios under experimental conditions, around 10:1 to at best 25:1. In this paper we will present the first results from a new front-end chip development for Si detector readout motivated by the need for better noise performance. Two particular detector developments initiated the attempt to build yet another CMOS amplifier :

a) A double-sided readout detector for the DELPHI μ-vertex detector upgrade,

b) A double-sided readout detector with parallel strips on both sides for X-ray detection down to energies of about 2 keV [6,7].

In addition, beyond the improvement in noise over existing readout chips, this development aims at a time-continuously sensitive amplifier with self-triggering capability. Time continuous amplifiers are needed for application in fixed target experiments. Self-triggering is imperative for experiments where there is only one particle present, which is fully absorbed in the detector. Both time-continuous operation and self-triggering are not available with existing microstrip readout chips, which are all of the switched capacitor type.

In the following, we describe the design of a preamplifier and shaper prototype to be used in such a new multipurpose readout chip. The prototype has been produced using the new 1.5 μm CMOS process of MIETEC [8] and has been extensively tested. Results from these tests will be presented.

2. NOISE ANALYSIS OF THE INPUT TRANSISTOR

By proper design, the total noise of the system without the associated detector capacitance and leakage current is dominated only by the noise of the input transistor [8,9,10]. The noise is caused by three different independent mechanisms [8,11].

Flicker noise ($S_{1/f}$)	1/f noise behaviour.
Channel noise (S_{ct})	White noise behaviour.
Bulk-resistance noise (S_{br})	White noise behaviour.

When referred to the gate, their respective noise voltage spectral density can be expressed as [8,11] :

$$S_{1/f}(\omega) = \frac{2\pi F_k}{W\ L_{eff}\omega} \quad \left[V^2/rad/s\right] \tag{1}$$

$$S_{ct}(\omega) = \frac{4\Gamma\ (\eta + 1)\,kT}{3g_m\,\pi} \quad \left[V^2/rad/s\right] \tag{2}$$

$$S_{br}(\omega) = \frac{2R_{bulk}\,\eta^2\,kT}{\pi} \quad \left[V^2/rad/s\right] \tag{3}$$

where :

W	is the transistor width
L_{eff}	is effective transistor length
F_k	is a process dependent constant.
Γ	is an excess noise factor depending on channel length and source-drain voltage.
η	is the ratio between the bulk to channel and gate to channel transconductances, g_{mbs}/g_m.
R_{bulk}	is the bulk resistance.

The total noise voltage spectral density at the input consequently becomes :

$$S_{nt} = S_{1/f} + S_{ct} + S_{br} \tag{4}$$

To minimize this value, the following design considerations must be taken :

- Highest possible g_m
- Lowest possible η
- Lowest possible Γ
- Optimizing the dimensions with respect to the input capacitance.

In strong inversion $g_m \sim \sqrt{\frac{W}{L_{eff}} I_d}$. L_{eff} should be kept as short as possible, except for the possible constraint discussed below concerning Γ. W should be as large as possible with an upper limit given by an optimal matching of the transistor dimensions to the input capacitance. I_d should be kept as high as possible within the limit set by the power consumption specification.

The higher the source to bulk voltage is, the lower becomes h. Consequently, this voltage should be kept as high as possible.

The factor Γ cannot be controlled in an evident way. However, it should be kept in mind that for submicron channel length it has been shown [12] that this factor is increased significantly, which might put a lower limit on L_{eff}.

For a charge amplifier, the final noise figure will be proportional to the total capacitive load at the input, i.e. the detector capacitance and the gate capacitance of the input transistor itself (discussed in the next section). Equations (1) and (2) show, however, that the origin of the noise is inversely proportional to the gate capacitance. Because of this, there exists an optimal gate capacitance value with respect to the overall noise performance depending on the value of the detector capacitance. The optimal value, C_{iopt}, can be calculated [13] to (see appendix for details) :

$$C_{iopt(1/f)} = C_d + C_f \tag{5}$$

or

$$C_{iopt\,(ct)} = \frac{C_d + C_f}{3} \tag{6}$$

for the extreme cases of only 1/f noise or only white noise respectively. (C_d is the detector capacitance and C_f is the feedback capacitance of the preamplifier.) The correct choice will be a value between these two, depending upon the ratio between the two different kinds of noise.

Since the gate length of the transistor should (at least for non-submicron processes) be kept to the minimum allowed by the process, the width of the transistor can be calculated if C_{iopt} is known.

3. NOISE FILTERING

The signal from the input stage has to be filtered (see Fig. 1) in order to limit the bandwidth and thus the noise [15]. It has been verified [8] that a very useful approach to this for monolithic charge sensitive amplifiers in high energy particle physics applications is the CR - $(RC)^n$ filter. The transfer function for such a filter has the form :

$$H(s) = \frac{V_o}{V_{si}}(s) = A_{Vs}\frac{s/\omega_c}{\left(1 + s/\omega_c\right)^n} \tag{7}$$

where ω_c is the desired centre frequency, n is the order of the filter, V_o and V_{Si} are the respective output and input voltages and A_{VS} is the gain. It can be shown [14] that very little is gained in noise performance by increasing the filter order (n). Thus, further discussion concentrates on the $n = 2$ filter, i.e. CR - $(RC)^2$. In the appendix, it is shown how the noise can be calculated in the frequency domain for this system. Here, only the resultant equations are shown.

For this filter, the following relationship holds between the centre frequency and the output peaking time, T_p :

$$\omega_c = \frac{1}{T_p} \tag{8}$$

The total noise voltage on the output becomes :

$$\overline{V_{on}^2} = \frac{\omega}{4\pi} S_{1/f} + \frac{\pi}{4T_p}\left(S_{ct} + S_{br}\right) \tag{9}$$

Please note that when the noise voltage spectral densities are substituted the frequency term disappears.

Finally, the equivalent input noise charge in numbers of electrons, ENC, is given by :

$$ENC = \frac{C_t e}{q}\sqrt{\overline{V_{on}^2}}\ \left[r.m.s.\,e^-\right] \tag{10}$$

where $\overline{V_{on}^2}$ is calculated from (1 - 3) and (9), q is the electron charge and C_t is the total input capacitance, i.e. the inherent input capacitance and the feedback capacitance of the preamplifier in addition to the detector capacitance and all stray capacitances.

4. CHIP DESIGN

The amplification chain is designed using the AMPLEX principle [8] and is shown in Fig. 2. It consists of a preamplifier, a shaper, a sample and hold element and a voltage buffer. The bias networks are separate and not drawn.

As shown in (9), the noise due to the input transistor goes down with increased peaking time, T_p [1]. However, this is in contradiction to the desire of adequate high speed operation. Therefore, a reset possibility is included and is performed by the reset switch between the input and output of the shaper. The purpose is to be able to shape the signal over the longest time period available, and then "cut" the tail of the shaped output just after the sampling time.

The operational transconductance amplifier (OTA) stages of the preamplifier and shaper are both of the single-ended folded cascode configuration. This provides simplicity together with sufficient DC gain, high speed operation, low power consumption and the right biasing conditions for the input transistor. The transistors are dimensioned for optimum performance.

4.1 The Preamplifier

From the noise filtering point of view, the charge preamplifier acts, in the frequency domain, as an all-pass filter in such a way that all the filtering is performed by the shaper. This makes the design easier and puts no upper limit on the g_m of the input transistor with respect to the filter characteristic. In fact, it implies that the main concern in the design is the noise performance of the input transistor, described in section 2[2].

The calculations that resulted in equations (5) and (6) indicate also that the feedback capacitance, C_f, should be as small as possible from the noise point of view. Also, the feedback resistor is very big, just small enough to supply the biasing and to avoid pile-up effects. This results in good stability and very good noise performance.

The preamplifier's main figures are shown in Table 4.1.

Table 4.1 Preamplifier Design Figures

Parameter	Value
Input transistor dimensions (W/L)	4300 µm / 1.5 µm
DC drain current (I_d)	200 µA
Transconductance (g_m)	@ 3 mA /V
Feedback capacitance (C_f)	@ 0.6 pF
Feedback resistance (R_f)	> 50 MΩ

1 This is only true for noise in the amplifier itself and not for noise such as detector leakage current and biasing resistor noise. For these noise sources, the noise increases with peaking time T_p (see Appendix).

2 Recent measurements have shown that care must also be taken in order to minimize the Miller equivalent capacitance inherent in the input transistor.

4.2 The Shaper

The filtering is accomplished by the components C_c, C_{fs}, R_{fs} and C_h, in addition to the inherent integrating function of the shaper OTA and its input capacitance, C_{is}. In the frequency range of interest it is only g_m (referred to as g_{ms}) of the shaper's input transistor together with the total output capacitance, C_{os}, that determine the integrator characteristics. The full filter transfer function can be expressed as :

$$H(s) = \left(\frac{g_{ms}C_c}{C_{os}C_{ts}}\right) \frac{s}{s^2 + \frac{1}{C_{ts}}\left(\frac{g_{ms}C_{fs}}{C_{os}} + \frac{1}{R_{fs}}\right)s + \frac{g_{ms}}{C_{os}C_{ts}R_{fs}}} \tag{11}$$

where $C_{ts} = C_c + C_{is} + C_{fs}$
and $C_{os} = C_h + C_{fs}$ + associated parasitic capacitances.

The criterion for this expression to be equivalent to (7) with $n = 2$, i.e. a double real pole is :

$$R_{fs} = \frac{C_{os}}{g_{ms}\,C_{fs}^2}\left(2C_{ts} - C_{fs} + 2\sqrt{C_{ts}\left(C_{ts} - C_{fs}\right)}\right) \tag{12}$$

which gives the pole location :

$$\omega_c = \frac{1}{T_p} = \frac{1}{2\,C_{ts}}\left(\frac{g_{ms}C_{fs}}{C_{os}} + \frac{1}{R_{fs}}\right) \tag{13}$$

and the voltage gain, A_{VS}, of the filter :

$$A_{VS} = \omega_c\, C_c\, R_{fs}\ . \tag{14a}$$

Following the guide-lines in the design, the shaper's main figures become as shown in Table 4.2.

Table 4.2 Shaper Design Figures

Parameter	Value
Peak time (T_p)	1500 ns
Input transistor dimensions (W/L)	390 µm / 1.5 µm
DC drain current (I_d)	10 µA
Transconductance (g_{ms})	@ 220 µA /V
Feedback capacitance (C_{fs})	@ 0.44 pF
Feedback resistance (R_{fs})	@ 6 MΩ
Coupling capacitance (C_c)	@ 6 pF
Hold capacitor (C_h)	@ 10 pF

The feedback resistor consists of a MOS transistor designed to give the highest possible output swing for the shaper.

4.3 Overall Charge Gain

The total charge to voltage gain of the system, from the detector to the output of the shaper, is given by :

$$A_c = \frac{A_{Vs}}{e\ C_f}\ [V/C] \qquad (14b)$$

where A_{Vs} is given by (14a) and C_f is the charge preamplifier feedback capacitor. This gives a value of approximately 15 mV/fC for this design.

4.4 The Reset Option

As mentioned, a reset possibility is included to "cut" the tail of the shaped signal in order to make the data acquisition faster. The main concern in the implementation of this facility is the risk of clock feedthrough, i.e. pick-up of digital control signals, from both on and off chip.

To compensate as much as possible for this, effort is put in the design to use a fully complementary reset control signal, i.e. *reset* and $\overline{reset}$ even if $\overline{reset}$ does not have any specific function. Full compensation implies that the capacitive coupling to each input of the chip is the same to both of the clock lines.

In order to minimize the charge injection from the reset switch at the input of the shaper, a half-size dummy switch is included at this node which is controlled by an internally generated $\overline{reset}$.

5. RESULTS FROM A FIRST PROTOTYPE

A prototype chip containing 12 channels, i.e. 4 channels with 0.5 μsec, 1 μsec and 1.5 μsec peaking time, has been produced in 1.5 μm CMOS technology. Measurements have been performed mainly on the 1.5 μsec and 1 μsec channels. The accuracy of the measurements has been determined to less than 10%, and the dominant error source is believed to be uncertainty in the value of the injected signal. Most of the measurements are repeated several times in order to find the average value for each measured point.

The power consumption has been measured to approximately 1.5 mW for each channel.

The parameters relevant to noise calculations for the 1.5 μm CMOS process that is used are listed in Table 5 below :

Table 5 Noise Figures

Parameter	Value	Condition
Input transistor dimensions (W/L_{eff})	4300µm / 0.8µm	
The transconductance (g_m)	@ 3 mA/V	I_d = 200 µA
Flicker noise coefficient (F_k)	@ $7.6.10^{-22}$	
Excess noise factor (G)	@ 2	
The slope factor (h)	@ 0.15	V_{bs} = -2V
The bulk resistance (R_b)	@ 2 kΩ	

5.1 ENC vs. Total Input Capacitance

Using a peaking time of 1500 ns and the values of Table 5 in the equations (1-3) and (9), the equivalent noise charge versus the total input capacitance is calculated using (10) to :

$$ENC / C_t = 16\ [r.m.s.\ e^- / pF] \tag{15}$$

The inherent capacitance of the input transistor can be calculated from its dimensions to ≅ 4 pF which gives the calculated noise of the system :

$$ENC = 64 + 16\ /pF\ \ [r.m.s.\ e^-] \tag{16}$$

Figure 3 shows the measured and calculated curve of the ENC vs. the input capacitance. The measured noise of the system is :

$$ENC = 160 + 12\ /pF\ \ [r.m.s.\ e^-] \tag{17}$$

The different gradients of the two slopes can be explained by process parameter variations. The excess noise measured with zero input load indicates that the inherent capacitance of the input transistor is higher than first estimated. This has also been verified by a direct measurement. Recent calculations show that if the Miller effect [11] of the gate to drain capacitance of the input transistor is taken into account, it can explain the discrepancy very well.

5.2 ENC vs. Bias Current

From (2) it is clear that the channel thermal noise, S_{ct}, of the input transistor is inversely proportional to g_m and thus to :

$\sqrt{I_d}$ - if it operates in strong inversion
I_d - if it operates in weak inversion.

Consequently, the overall noise dependence on the drain current is :

$$ENC(I_d) \sim \sqrt{K_1 + \frac{K_2}{\sqrt{I_d}}} \tag{18}$$

or

$$ENC(I_d) \sim \sqrt{K_1 + \frac{K_2'}{I_d}} \tag{19}$$

for the two cases respectively. K_1 , K_2 and K_2' are constants for given fixed values of C_t and T_p.

The measured curve together with the calculated curves for the two cases is shown in Fig. 4. It indicates that the input transistor is working close to the strong inversion region.

5.3 ENC vs. Peaking Time

From (9) it is clear that the channel thermal noise, S_{ct}, and the bulk-resistance noise, S_{br}, are dependent upon the peaking time in such a way that the overall noise becomes :

$$ENC(T_p) \sim \sqrt{K_3 + \frac{K_4}{T_p}} \tag{20a}$$

As in the previous section, K_3 and K_4 are constants, but now for given fixed values of C_t and I_d. In Fig. 5 the noise performance is plotted against the peaking time. Measurements have been done for peaking times of 1000 ns and 1500 ns.

5.4 ENC vs. External Bias Resistor

In order to study contributions to the noise originating from a bias resistor when the amplifier is connected to a strip detector, different external resistors (held at a fixed potential) were added to the input of the amplifier. The noise as a function of the external biasing resistor can be written as :

$$ENC(R_p) = \sqrt{ENC_\infty^2 + ENC_{dr}^2} \tag{20b}$$

where ENC_∞ is the noise measured with no parallel resistor and ENC_{dr} is calculated from (48) in the appendix. Figure 6 shows the measured noise values for resistors in the range of 1 MΩ to 100 MΩ, together with the calculated values. The agreement is very good.

It should be noticed that for lower values of C_t the contribution from R_p becomes more important.

5.5 Linearity

The linearity is limited by non-linear behaviour of the feedback resistor (MOSFET) of the shaper. Figure 7 shows the voltage gain vs. injected charge in terms of minimum ionizing particles. There are two ways of measuring the linearity. One way is to measure the pulse height of the output voltage, regardless of at which time point the peak arrives. The other way is to measure the output voltage at a defined period of time after the signal was injected, which typically will be the peaking time for some signal magnitudes but not necessarily all. The correct procedure is dependent on the application. In this measurement the latter method is used.

The charge gain in Fig. 7 differs somewhat from the value estimated in section 4.3. This is due to different values of R_{fs} and g_m than those specified in Table 4.2, which again is due to different biasing of the shaper.

5.6 Resetting

Initially there were two major reasons for concern about the effect on overall performance due to the resetting of the shaper (as described earlier in section 4.4). These were :

a) What would be the effect of the reset clock feedthrough ?
b) What would happen to the noise ?

Figure 8 shows the reset operation. The output of the shaper is reset on every falling edge of the clock pulse and then activated again on the rising edge. The result can be seen in picture 8a, whilst picture 8d shows the fully shaped signal without being reset.

Concerning the effect of clock feedthrough, picture 8a clearly indicates that this will not cause any problem since no distortion is observed. However, if the dummy *reset* method described in section 4.4 is not used, the situation of picture 8a would rather look like that of picture 8c, in which the dummy line is not running.

Measurements indicate that the noise performance is degraded slightly when resetting in the order of 0-30%. However, these numbers are very uncertain and are dependent on several parameters, e.g. reset period, reset duration, arrival of the signal with respect to the reset's falling edge, capacitance load, etc. . This will be looked at in more detail in future studies.

5.7 Effects of Irradiation with a ^{90}Sr Source

First tests of radiation hardness using the 1.5 μsec channel have been performed. The chip was exposed to a ^{90}Sr source giving a dose rate of about 5 krad/hour. After an exposure with a total dose of 135 krad, the chip was still functioning normally. To maintain the same bias current in the preamplifier and the identical shaping, the external bias settings had to be adjusted after each irradiation. The overall deterioration in noise performance after 135 krad amounted to approximately 100% increase in noise (see Fig. 9). More detailed studies on radiation damage are being pursued.

6. CONCLUSIONS

Results on the performance of a very low noise preamplifier shaper chip built in 1.5 μm CMOS technology for use with Si strip detectors have been presented. With a shaping time of 1.5 μsec a noise performance of ENC = 160 e^- + 12 e^- / pF was achieved, somewhat above the value calculated with the parameters of this process. The circuit has a linear response to an input signal charge extending over more than 25 MIPs. A *"fast"* reset of the shaper can be performed without significant increase of the measured amplifier noise. The radiation hardness of the chip has been demonstrated for electromagnetic radiation up to 135 krad. It is believed that the performance of this chip can still be improved and a slightly modified design is under study. It is shown that the good noise performance of this chip, particularly important for X-ray detection, can only be fully exploited with carefully optimized Si strip detectors. Bias resistors above 100 MΩ, low leakage currents in the range below 1 nA/strip and a small interstrip capacitance smaller than 1 pF/cm should be aimed at.

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APPENDIX

A.1 *CR* - $(RC)^n$ Filter Relationships

The transfer function for the CR - $(RC)^n$ filter is given by :

$$H(s) = \frac{s / \omega_c}{\left(1 + s/\omega_c\right)^n} \tag{21}$$

where n is the filter order and ω_c is the desired central frequency. This expression holds for the system shown in Figs. 1 and 2, once the dc gain is normalized.

Multiplying (21) by $\frac{1}{s}$ and taking the inverse Laplace transformation gives the output voltage pulse to a voltage step input as a function of time.

$$V_o(t) = \frac{\left(\omega_c t\right)^{n-1}}{e^{\omega_c t}(n - 1)!} \quad \Delta V_i \tag{22}$$

Using this expression it is now possible to derive an expression for the peaking time T_p.

$$T_p = \frac{n - 1}{\omega_c} \tag{23}$$

From the previous two expressions the peak voltage can be found to be :

$$V_{o\,(peak)} = V_o\left(t = T_p\right) = \frac{(n - 1)^{n-1}}{e^{n-1}(n - 1)!} \quad \Delta V_i \tag{24}$$

A.2 Output Noise Power

The total mean square noise voltage on the output after filtering is given by :

$$\overline{V_{on}^2} = \int_0^\infty S_{nt}(\omega) \left|H(\omega)\right|^2 d\omega \tag{25}$$

where S_{nt} is given by (4).

From (23) the relationship between ω_c and T_p for a two-pole system can be seen to be :

$$\omega_c = \frac{1}{T_p} \tag{26}$$

The integral may now be solved to give :

$$\overline{V_{on}^2} = \frac{\omega}{4\pi} S_{1/f} + \frac{\pi}{4T_p}\left(S_{ct} + S_{br}\right) \tag{27}$$

A.3 Equivalent Input Noise Charge

The equivalent noise at the input, $V_{in_{eq}}$, is amplified by the same factor as the input signal ΔVi. From (24) it can be seen that for a two-pole system this amounts to :

$$\frac{V_{o_{peak}}}{\Delta V_i} = \frac{1}{e} \tag{28}$$

Since the noise at the output, $\overline{V_{on}^2}$ is already known, the above relationship can be used to find $\overline{V_{in_{eq}}^2}$.

$$\overline{V_{in_{eq}}^2} = e^2 \overline{V_{on}^2} \tag{29}$$

therefore the equivalent input noise charge in the number of electrons becomes :

$$ENC = \frac{C_t e \sqrt{\overline{V_{on}^2}}}{q} \; [r.m.s.\, e^-] \tag{30}$$

where C_t is the total input capacitance and $\overline{V_{on}^2}$ is calculated from (1-3) and (27).

A.5 Input Capacitance Optimization

It has already been stated that both $S_{1/f}$ and S_{ct} improve with increased input transistor size and hence increased gate capacitance, C_i. However, the total equivalent noise charge is proportional to C_t, which includes both C_i and the detector capacitance C_d. Thus, for a given C_d an optimum value of C_i exists with respect to noise.

Assuming $C_i = C_{ox}\, L_{eff}$, the two noise sources from (1) and (2) may be rewritten in order to extract C_i.

$$S_{1/f} = \frac{2\pi F_k C_{ox}}{\omega C_i} = \frac{\gamma'}{C_i} \tag{31}$$

$$S_{ct} = \frac{4\Gamma(\eta + 1)\, kTL_{eff}}{3\pi \sqrt{2\mu_o I_d}\sqrt{C_i}} = \frac{\delta'}{\sqrt{C_i}} \tag{32}$$

The latter expression is for strong inversion.

The *ENC* for both noise sources can now be calculated to be :

$$ENC_{1/f}^2 = \frac{\gamma'\sigma\left(C_i + C_d + C_f\right)^2}{C_i} \tag{33}$$

$$ENC_{white}^2 = \frac{\delta'\sigma\left(C_i + C_d + C_f\right)^2}{\sqrt{C_i}} \tag{34}$$

where σ is a constant referring to the filter order.

The ENC expressions of (33) and (34) may now be optimized for C_i, giving the following results :

$$C_{iopt(1/f)} = C_d + C_f \tag{35}$$

$$C_{iopt\,(ct)} = \frac{C_d + C_f}{3} \tag{36}$$

It can be shown [14] by using the figures from this paper, that for peaking times in the order of 1 µs or less the channel thermal noise is normally more dominant than the flicker noise. With this in mind, the dimensions of the input transistor should be chosen so as to give a capacitance value closer to (36) than (35).

A.6 Peaking Time Optimization

If the noise due to the detector is to be taken into account, then new expressions for S_{nt} and $\overline{V}_{on}^2$ can be made resulting in an expression for the optimum peaking time with respect to noise.

It has been shown [16] that two noise sources exist due to the detector leakage current and the bias resistance. Expressed in terms of noise voltage spectral density these are :

$$S_{dl}(\omega) = \frac{q I_{dl}}{\pi C_t^2 \omega^2} \left[V^2/\,rad/s\right] \tag{37}$$

and

$$S_{dr}(\omega) = \frac{2kT}{C_t^2 (R_b \,||\, R_f)\, \pi\omega^2} = \frac{2kT}{C_t^2 R_p\, \pi\omega^2} \left[V^2/\,rad/s\right] \tag{38}$$

where I_{dl} is the detector leakage current, q is the electron charge and R_p is the parallel combination of R_b (the detector bias resistor) and R_f (the feedback resistor across the preamplifier).

The total noise in the system can now be modified to include equations (37) and (38).

$$S_{nTOT} = S_{dl} + S_{dr} + S_{ct} + S_{1/f} + S_{br} \tag{39}$$

Substituting (39) into (25) and solving the integral for a two-pole system, a new expression for total noise power can be found in terms of noise voltage spectral densities to be :

$$\overline{V_{onTOT}^2} = \frac{\pi T_p \omega^2}{4} \left(S_{dl} + S_{dr}\right) + \frac{\omega}{4\pi} S_{1/f} + \frac{\pi}{4T_p} \left(S_{ct} + S_{br}\right) \tag{40}$$

It is now clear from (40) that an optimum value for T_p exists. Optimizing (40) for T_p gives :

$$T_{popt} = \sqrt{\frac{(S_{ct} + S_{br})}{(S_{dl} + S_{dr})\,\omega^2}} \tag{42}$$

Substituting the noise sources gives :

$$T_{popt} = \sqrt{\frac{2kTR_p C_t^2 \left(2\Gamma(\eta + 1) + 3g_m R_{bulk}\eta^2\right)}{3g_m (I_{dl} q R_p + 2kT)}} \tag{43}$$

A.7 ENC for the Individual Noise Sources

Combining (30) and (40) and using the values given by (1), (2), (3), (37) and (38), the *ENC* of the individual noise sources can be calculated for the CR-RC^2 filter. Thus, in terms of [r.m.s. e$^-$] :

The flicker noise :

$$ENC_{1/f} = \frac{C_t e}{q}\sqrt{\frac{F_k}{2WL_{eff}}} \tag{44}$$

The channel noise :

$$ENC_{ct} = \frac{C_t e}{q}\sqrt{\frac{\Gamma(\eta + 1)kT}{3g_m T_p}} \tag{45}$$

The bulk-resistance noise :

$$ENC_{ct} = \frac{C_t e}{q}\sqrt{\frac{R_{bulk}\eta^2 kT}{2T_p}} \tag{46}$$

The diode leakage current noise :

$$ENC_{dl} = \frac{e}{q}\sqrt{\frac{q I_{dl} T_p}{4}} \tag{47}$$

The biasing resistor noise :

$$ENC_{dr} = \frac{e}{q}\sqrt{\frac{T_p kT}{2R_p}} \tag{48}$$

The total noise can then be calculated as :

$$ENC = \sqrt{ENC_{1/f}^2 + ENC_{ct}^2 + ENC_{br}^2 + ENC_{dl}^2 + ENC_{dr}^2}\ [r.m.s.\ e^-] \tag{49}$$

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Figure Captions

Fig. 1 : Charge sensitive preamplifier with filter.

Fig. 2 : Principle of the AMPLEX-type amplification chain.

Fig. 3 : ENC vs. input capacitance.

Fig. 4 : ENC vs. bias current.

Fig. 5 : ENC vs. peak time.

Fig. 6 : ENC vs. biasing resistor value.

Fig. 7 : Linearity.

Fig. 8 : Output of the shaper.
a) Reset every 2.5 μs, signal apparent in one of the periods.
b) As the previous, but no signal apparent.
c) As in a, but the dummy clock line, *reset*, not running.
d) Original output with signal and no reset.

Fig. 9 : ENC vs. radiation dose.

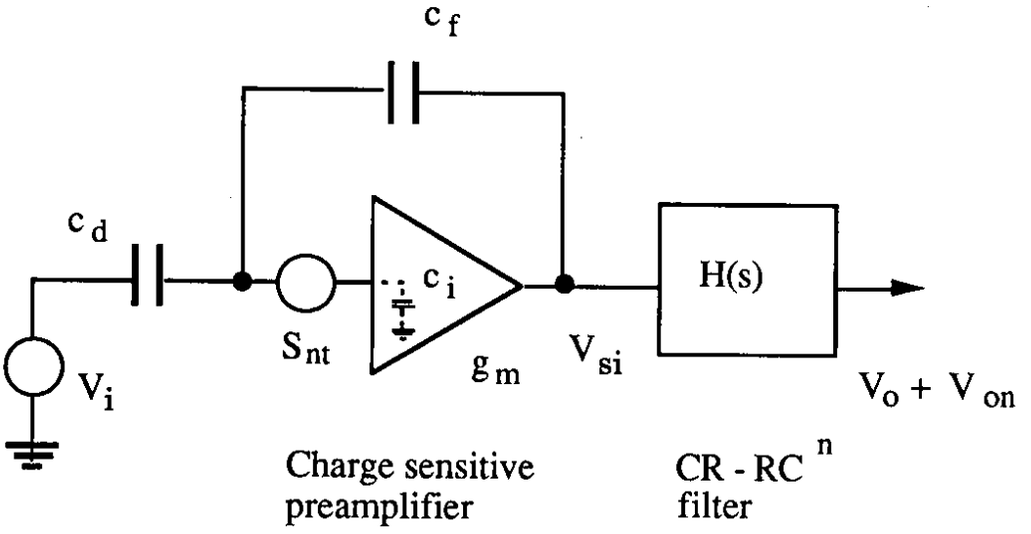

c_f
c_d
c_i
S_{nt}
g_m
V_{si}
H(s)
V_i
$V_o + V_{on}$
Charge sensitive preamplifier
CR - RC ^{n} filter

Fig. 1

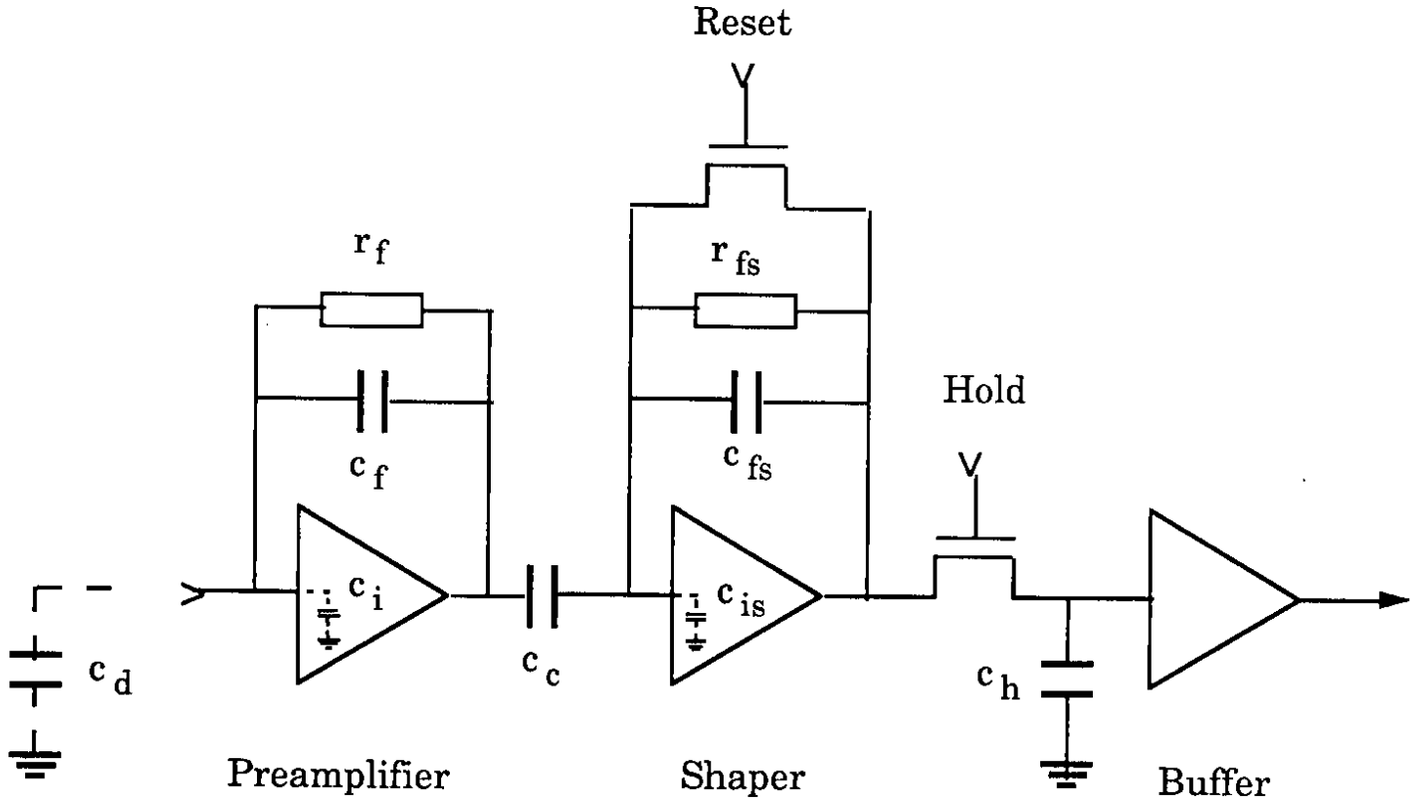

Reset
r_f
r_{fs}
Hold
c_f
c_{fs}
c_i
c_{is}
c_d
c_c
c_h
Preamplifier
Shaper
Buffer

Fig. 2

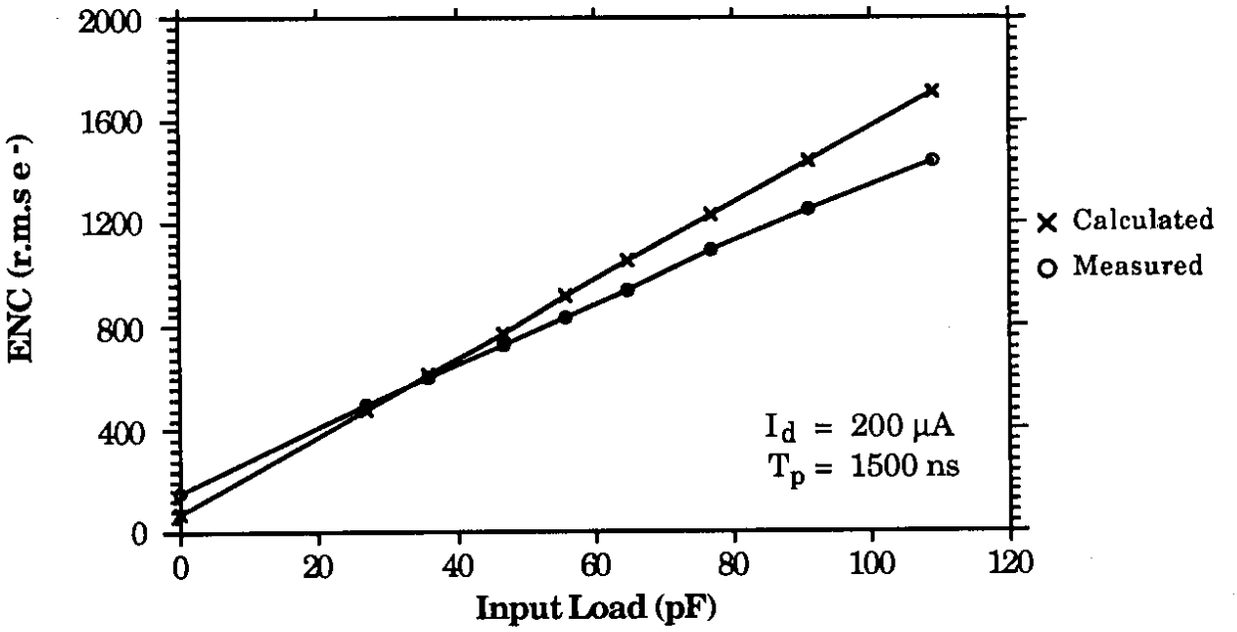

2000
1600
1200
800
400
0
ENC (r.m.s e -)
0
20
40
60
80
100
120
Input Load (pF)
Calculated
Measured
I_d = 200 μA
T_p = 1500 ns

Fig. 3

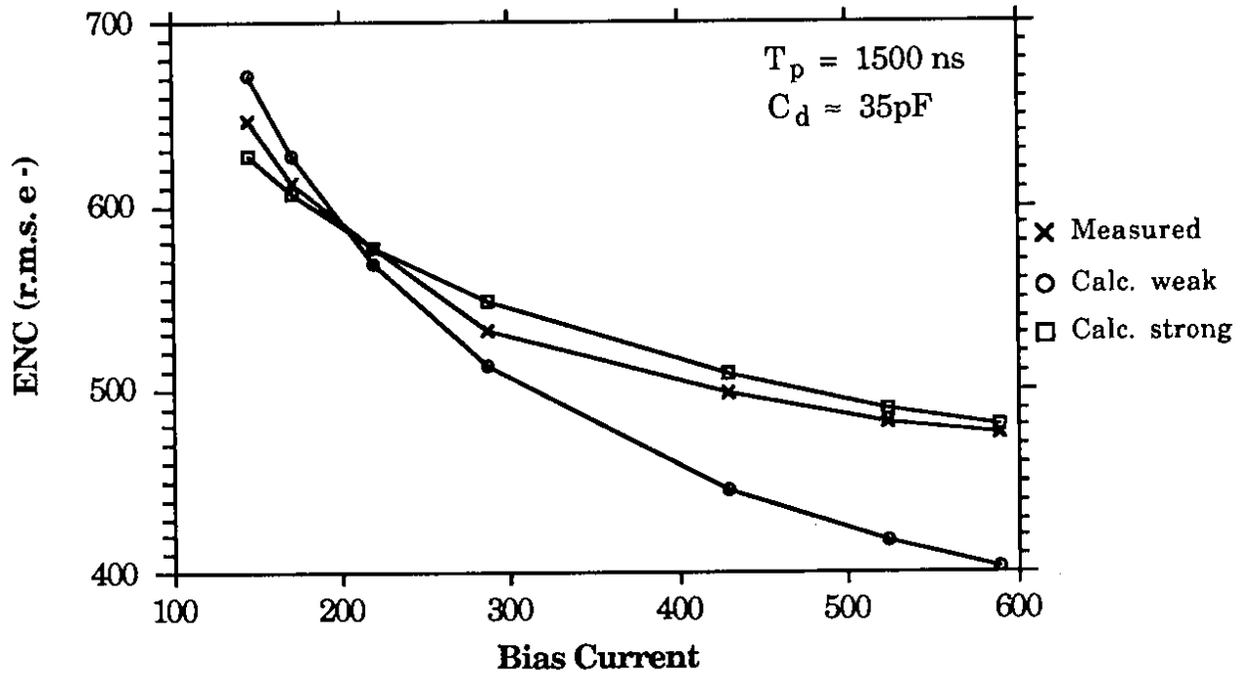

700
600
500
400
ENC (r.m.s. e -)
100
200
300
400
500
600
Bias Current
T_p = 1500 ns
C_d ≈ 35pF
Measured
Calc. weak
Calc. strong

Fig. 4

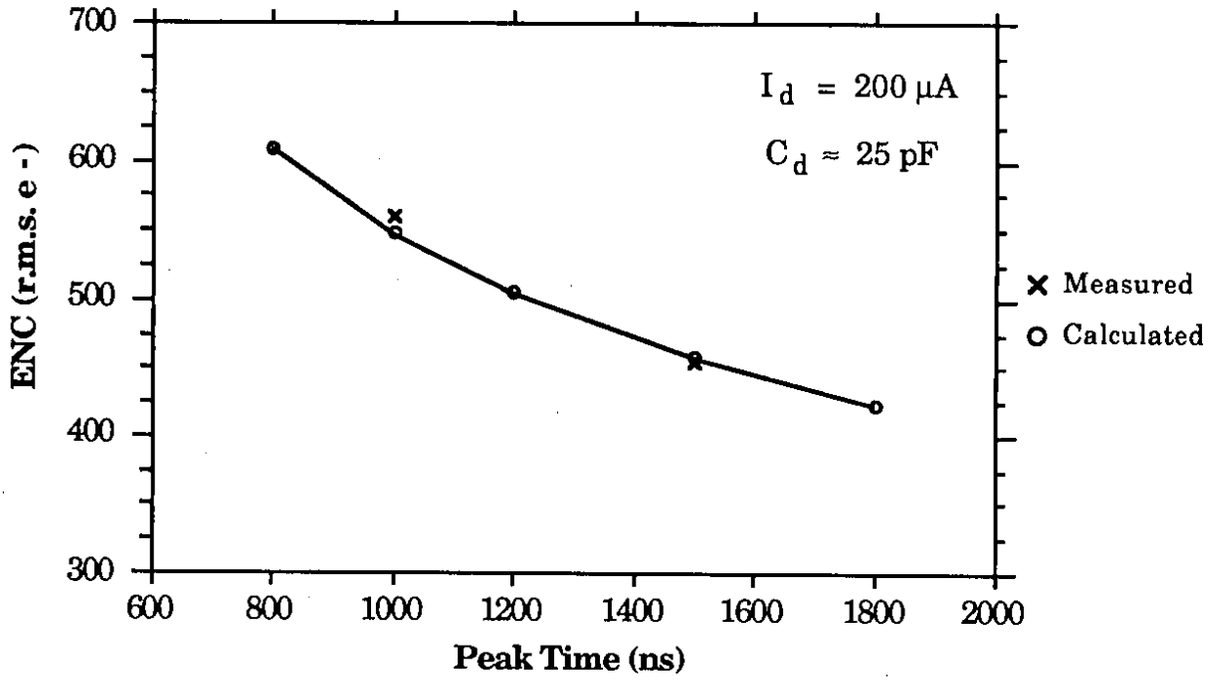

700
600
500
400
300
600
800
1000
1200
1400
1600
1800
2000
ENC (r.m.s. e -)
Peak Time (ns)
I_d = 200 μA
C_d ≈ 25 pF
Measured
Calculated

Fig. 5

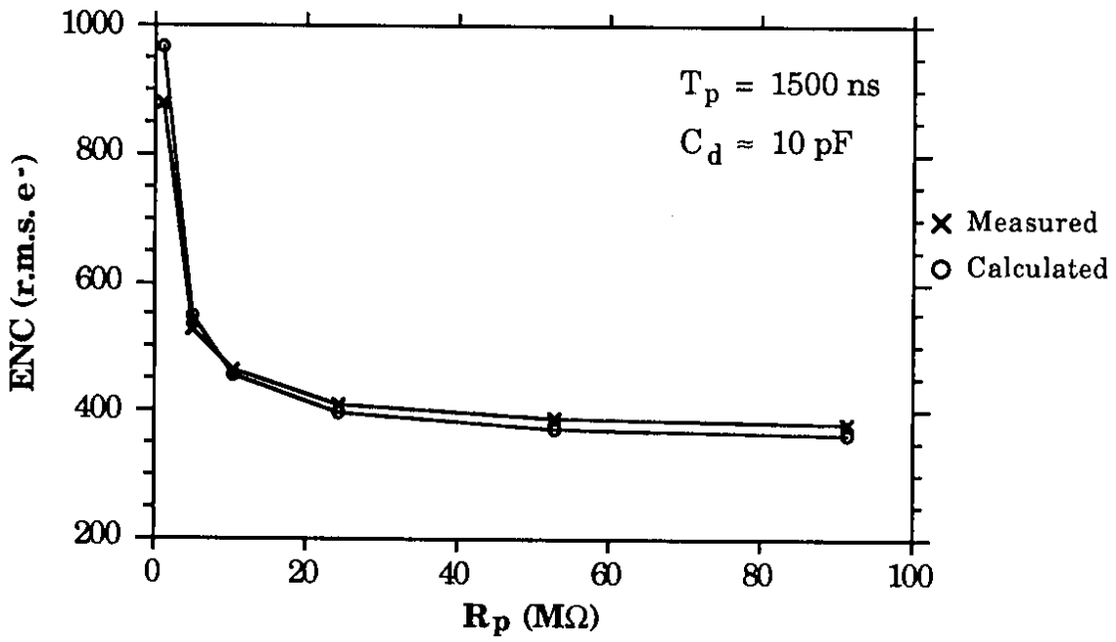

1000
800
600
400
200
0
20
40
60
80
100
ENC (r.m.s. e-)
R_p (MΩ)
T_p = 1500 ns
C_d ≈ 10 pF
Measured
Calculated

Fig. 6

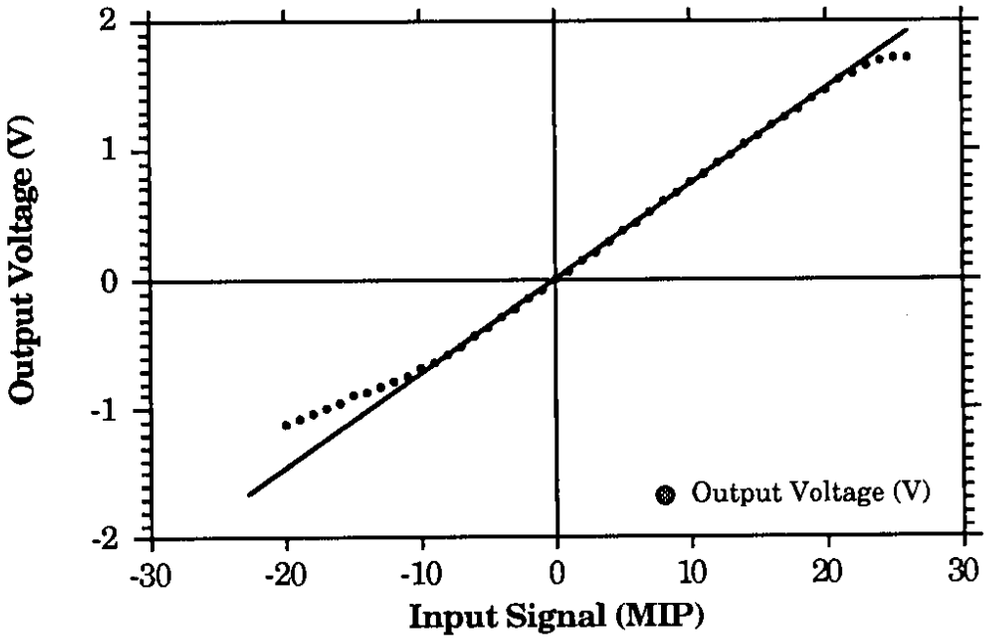
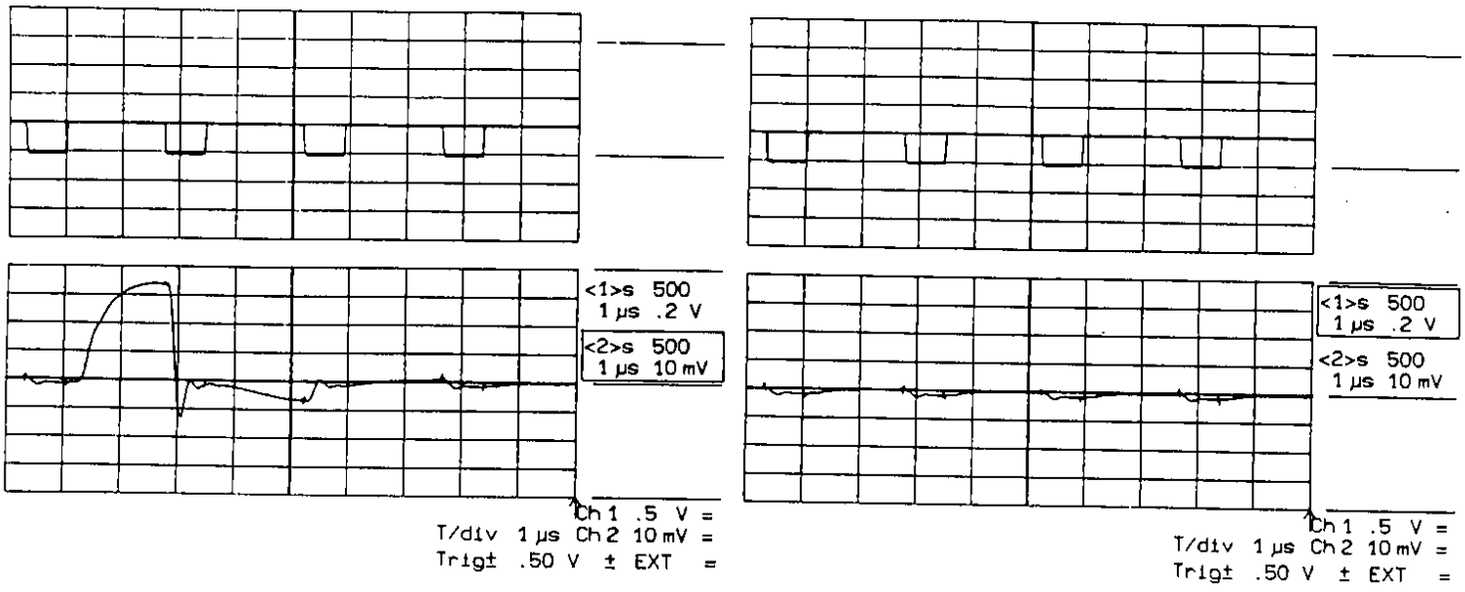
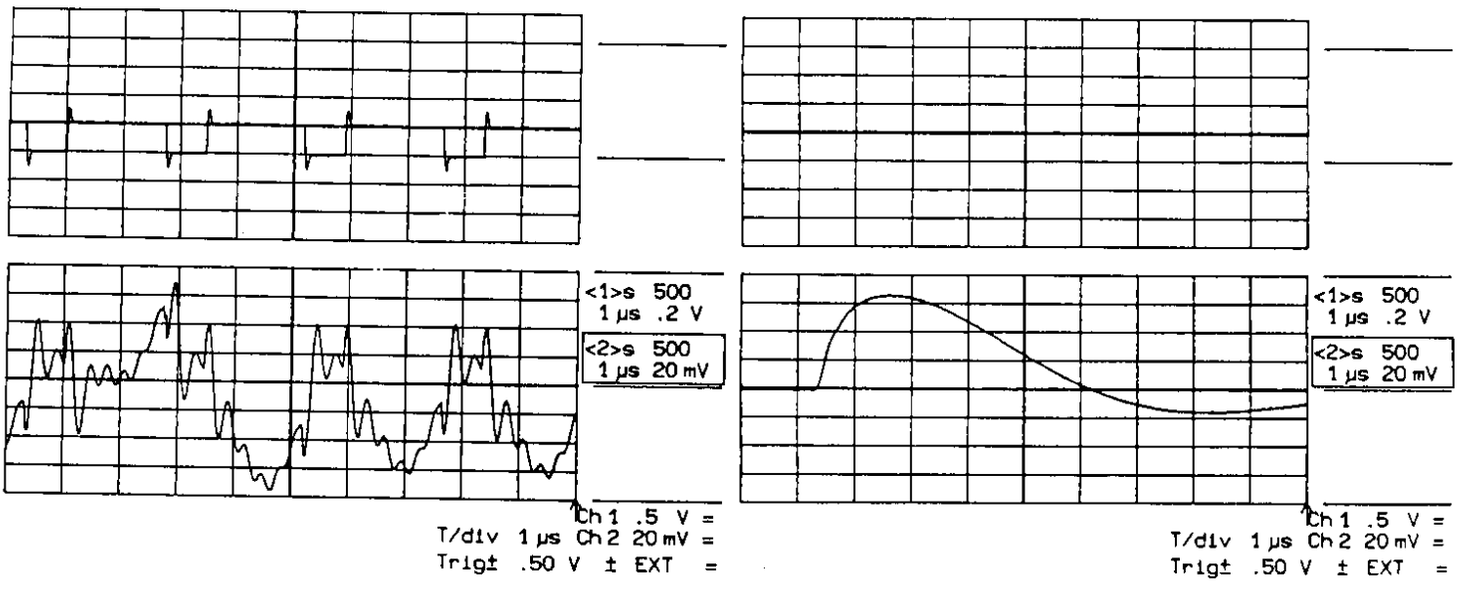

Output Voltage (V)
2
1
0
-1
-2
-30
-20
-10
0
10
20
30
Input Signal (MIP)
Output Voltage (V)

Fig. 7


<1>s 500
1 µs .2 V
<2>s 500
1 µs 10 mV
Ch 1 .5 V =
T/div 1 µs Ch 2 10 mV =
Trig± .50 V ± EXT =

a) b)


<1>s 500
1 µs .2 V
<2>s 500
1 µs 20 mV
Ch 1 .5 V =
T/div 1 µs Ch 2 20 mV =
Trig± .50 V ± EXT =

c) d)

Fig. 8

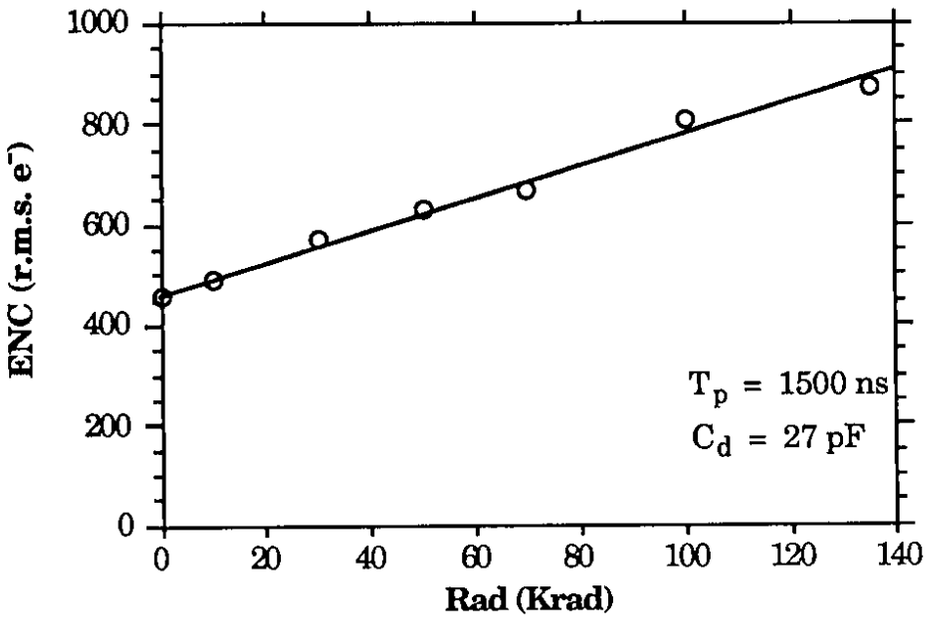


Fig. 9

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