CMOS Mixed-Signal Circuit Process Variation Sensitivity Characterization for Yield Improvement

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Abstract **– A mixed-signal circuit's performance and yield dependency on process variation are investigated with numerical circuit solution, statistical simulation, and implemented circuit measurement in 65nm partially-depleted silicon-on-insulator CMOS process. Increased relative variation in 65nm process is examined with site-to-site and wafer-to-wafer process variations. A current-controlled oscillator's performance and device threshold voltages are cross-correlated using simulation and RF measurement. Up to 93.9% cross-correlation between oscillation frequency and device threshold voltage is obtained, and strong model-to-hardware correlation is observed through statistical analysis of simulation result and circuit measurement. The yield learning process of design, simulation, measurement, and statistical analysis is proposed.**

I. INTRODUCTION

The key to successful semiconductor manufacturing lies in the agile yield learning, which adaptively adjusts technology and design through feedbacks in various stages, to overcome process variation and to optimize the process for higher yield [1]. Research on the yield learning in sub-100nm processes is challenging due to increased relative process variation, limited access to technology, and demanding inline and offline measurements for dc and ac characterizations. To understand the physical device variation, not only wafer-to-wafer variation but also site-to-site variation in a wafer must be addressed, since the process variation inside a wafer is more prevalent than ever because of the increased relative variation [2]. Measurement data need to be analyzed statistically to explore relations among the data, and dominant design parameters should be extracted to enhance circuit design-level yield learning [3]. In this paper, 65nm PD SOI (partially-depleted silicon-on-insulator) CMOS mixed-signal circuit process variation and sensitivity are investigated with analytic circuit solution, simulation, measurement, and statistical analysis. It begins with discussion on process variation in section II, and a test vehicle in section III. The mixed-signal circuit's process variation sensitivity is examined with analytic circuit solution and statistical simulation in section IV. Model-to-hardware correlation and statistical analysis of measurement and simulation data are presented in section V.

II. MIXED-SIGNAL CIRCUIT YIELD LEARNING

A fabricated semiconductor circuit diverges farther from an original design statistically as device feature size shrinks below sub-100nm, since absolute process variation does not decrease proportionally. Because of the increased relative variation, each device shows more variation in parameters than ever as device size scales down. As a result, as described in Fig. 1, the variation inside a wafer (site-to-site variation) surpasses the variation of a given site across wafers (wafer-to-wafer variation) [2].

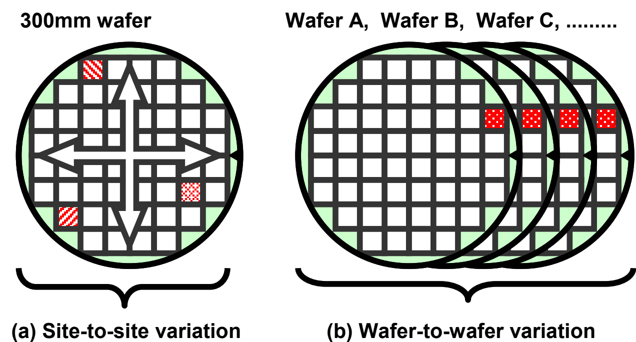

Fig. 1. Site-to-site process variation on a wafer and wafer-to-wafer process variation across wafers.

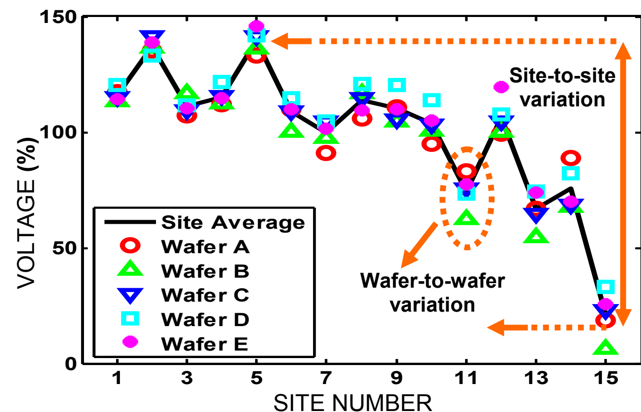

Fig. 2. 65nm PD SOI FET device relative threshold voltages on multiple sites (1-15), ordered as increasing variation, across five consecutive 300mm wafers (A-E).

Fig. 2 shows 65nm PD SOI FET device threshold voltage measurements across multiple sites (1-15) and five consecutive 300mm wafers (A-E). The plot emphasizes that the site-to-site variation is stronger than the wafer-to-wafer variation in 65nm process, and the site-to-site variation will be more dominant with smaller devices, such as in 45nm and 32nm processes. It is therefore essential to characterize device variations in both dimensions, with statistical measurement, analysis, and modeling.

III. MIXED-SIGNAL CIRCUIT YIELD LEARNING

As the yield of microprocessor manufacturing depends more on the mixed-signal circuit performance, the statistical analysis of such system block provides another layer of yield learning feedback interface to both the process technology and the higher-level design activities. The system block performance measurement, device characterization, and circuit design parameters should be statistically analyzed to establish a design-manufacturing interface [4]. For the study of mixed-signal process variation sensitivity, a 3-stage differential current-mode logic (CML) ring oscillator with symmetric loads is used as a test vehicle [5]. A simplified schematic diagram of the differential inverter is in Fig. 3. The differential inverting amplifier is the most common circuit topology of analog design [6], and the symmetric loads have been used as a building block for many mixed-signal circuits, such as voltage-controlled oscillators (VCOs) in phase-locked loops (PLLs). In addition to the process variation, the design of reliable mixed-signal circuit in sub-100nm process is challenged by reduced supply voltage headroom. Specifically, many circuit techniques for yield improvement are constrained by the lowered power supply voltage.

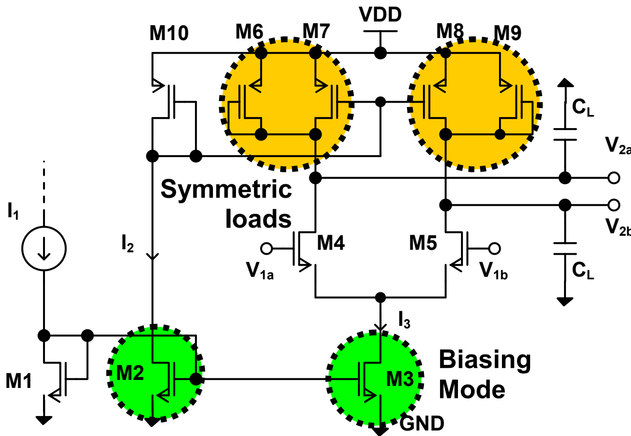

Fig. 3. Schematic diagram of differential current-mode logic inverter with symmetric loads.

Consequently, the fabricated mixed-signal system block performance is affected extensively by the process variation, especially by the site-to-site variation. For example, Fig. 4 shows the measured current-controlled oscillator (ICO) circuit oscillation frequency (fosc) distribution over a 65nm PD SOI CMOS 300mm wafer with a fixed input bias current to I_1. The ICO is a 3-stage ring oscillator built with the differential inverter in Fig. 3. Total 85 ICOs were measured in the wafer. The average oscillation frequency (μf) and standard deviation (σf) are 12.6GHz and 1.29GHz respectively, as arranged in Table I. Further statistical analysis provides several interesting observations. According to Table I, when the ICO and inline device parameter measurement on the same chip site and wafer are compared, there are -14.8GHz/V sensitivity and 93.9% cross-correlation between oscillation frequency and floating-body nFET threshold voltage (Vth_nfet_fb). The obtained correlation is the strongest out of statistical analysis on thousands of measured inline parameters. A validated assumption here is that the inline devices and ICO in the same site are highly correlated by their proximity, as the 93.9% cross-correlation suggests, and again that the chip site-to-site variation is much greater than the variation inside a chip site. Information such as this provides crucial feedback not only to every level of semiconductor manufacturing, but also to the mixed-signal and digital circuit design processes.

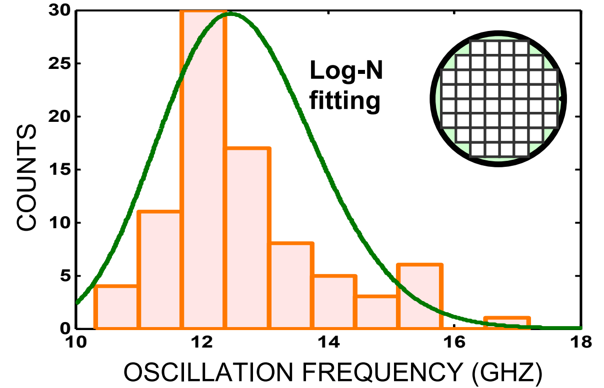

Fig. 4. Operating frequency distribution of current-controlled oscillator with a fixed input bias current. 85 circuits were measured across a 65nm 300mm PD SOI CMOS wafer.

TABLE I
MEASURED ICO STATISTICAL CHARACTERISTICS

Parameter	Measurement
Average oscillation μf	12.6 GHz
Standard deviation σf	1.29 GHz
Cross-correlation with Vth_nfet_fb	-0.939
Sensitivity over Vth_nfet_fb	-14.8GHz/V

IV. ICO PROCESS VARIATION SENSITIVITY ANALYSIS

The FET threshold voltage (Vth) is selected as a design parameter, because it shows the strongest statistical relation with circuit performance among thousands of other measured device characteristics. Besides, it abstracts complex physical process variation phenomena to a single number, and it is readily used as design variable both in analog and digital designs. First, the ICO building block, the differential inverter in Fig. 3 is solved numerically with circuit equations and simple FET models. Current sourcing nFETs (M1-M3) are implemented with thick-oxide nFETs for low-leakage and high output impedance, and all other devices are regular FETs. An approximate oscillation frequency relation with design parameters at operating biasing point is given as (1).

$$f_{osc} \propto \frac{I_3}{N \cdot VDD \cdot C_L} \qquad (1)$$

Assuming the number of ICO stages N and power supply voltage VDD are fixed, the differential pair biasing current I_3

and the load capacitance C_L determines oscillation frequency. The tail current I_3 is rather an actively controlled parameter than the capacitive load C_L, which is more passively adjusted in the design stage. An approximate calculation with long channel FET model in (2) for saturation and (3) for triode region is straightforward.

$$I_{d,sat} = \frac{\beta}{2}\left(V_{gs} - V_{th}\right)^2, V_{gs} - V_{th} > V_{ds} \quad (2)$$

$$I_{d,tri} = \beta\left[\left(V_{gs} - V_{th}\right)V_{ds} - \frac{1}{2}V_{ds}^2\right], V_{gs} - V_{th} < V_{ds} \quad (3)$$

For example, when M2 and M3 are in triode region, the nFET threshold voltage Vth_nfet process variation does not affect current I_2 and I_3. But an increase in |Vth_pfet| decreases M2 drain voltage V_{D2}, drain current I_2, mirrored current I_7, and tail voltage V_{D3}. As a result, the tail current I_3 is reduced. Therefore |Vth_pfet| increase lowers the oscillation frequency according to (1) and the assumed long channel FET model. When calculated for 65nm PD SOI CMOS process, the ICO oscillation frequency sensitivity on |Vth_pfet| is -45.1GHz/V at the average threshold voltage. An assumed loading capacitance C_L is 10fF. Obviously, long channel model is not good enough to examine both pFET and nFET threshold voltage process variation effects, and short channel model in (4) for saturation and (5) for triode would be necessary to get more insights.

$$I_{d,sat} = \frac{\beta}{2}\left(V_{gs} - V_{th}\right)^2\left(1 + \lambda V_{ds}\right), V_{gs} - V_{th} > V_{ds} \quad (4)$$

$$I_{d,tri} = \beta\left[\left(V_{gs} - V_{th}\right)V_{ds} - \frac{1}{2}V_{ds}^2\right]\left(1 + \lambda V_{ds}\right), V_{gs} - V_{th} < V_{ds} \quad (5)$$

When the short channel model is employed, equations are not easily solved in closed forms. Circuit current relations are used to evaluate the V_{d2}, V_{d3}, and the tail current I_3 with a numerical solver. Obtained ICO oscillation frequency sensitivity on device threshold voltages are plotted in Fig. 5. Estimated oscillation frequency sensitivity is obtained as a derivative on each curve at the average threshold voltage.

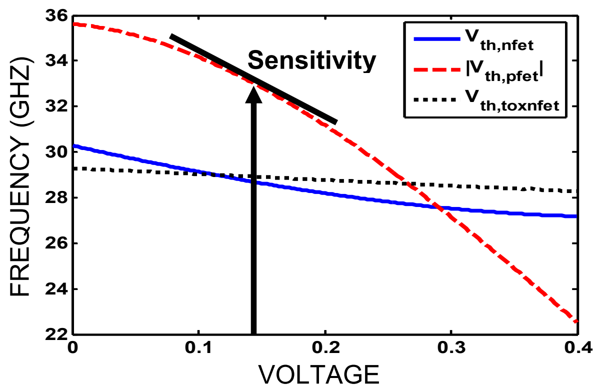

Fig. 5. ICO oscillation frequency dependency on FET devices, obtained with numerical circuit analysis and short channel model.

The simplified numerical circuit analysis is helpful to understand the oscillation frequency dependency on the threshold voltages, and it is used in the early design stage as one of performance evaluation for the process variation. As the mixed-signal design gets finalized, the best-effort circuit performance and yield are estimated with more sophisticated FET models and circuit simulation tools. The ICO design was simulated in 65nm PD SOI technology with 100 statistical process variations. The plot in Fig. 6 shows ICO circuit's simulated oscillation frequency relation on threshold voltages for a given current bias input. Threshold voltages were extracted from separate DC sweep simulation by finding the effective current flow with respect to the device width and length ratio. Obtained cross-correlation and statistical dependency are arranged in Table II.

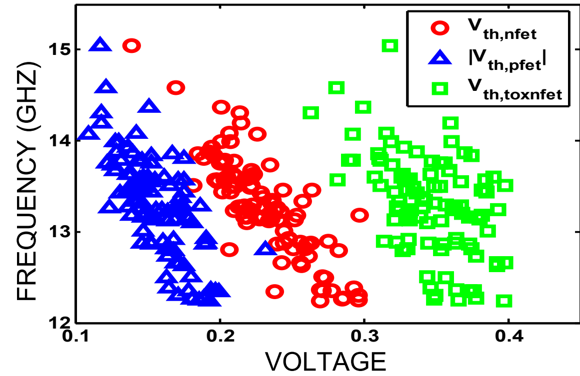

Fig. 6. Current-controlled oscillator frequency and device threshold voltage relation obtained from statistical simulation.

TABLE II
ICO CROSS-CORRELATION AND SENSITIVITY

	Cross-correlation	Sensitivity(GHz/V)
Vth_nfet	-0.835	-15.1
|Vth_pfet|	-0.710	-17.8
Vth_tox_nfet	-0.499	-9.47

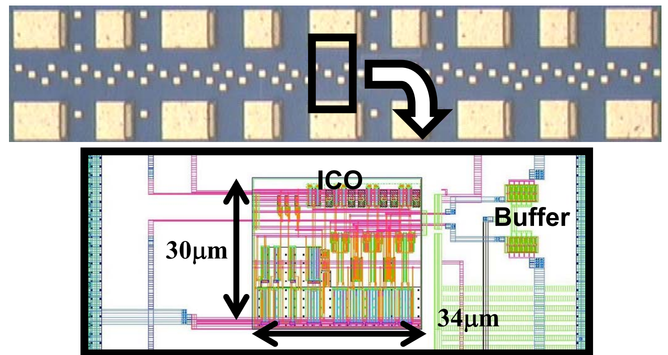

Fig. 7. Die photograph of implemented 65nm PD SOI CMOS 3-stage CML oscillator circuit with dual wedge probe pad sets.

V. ICO Measurement and Statistical Analysis

The designed ICO circuit was fabricated with 65nm PD SOI CMOS process as shown in Fig. 7. On a 300mm wafer, 13 circuits were selected, and the circuit oscillation frequency

was measured with a fixed biasing current input. Also FET device dc parameters characterized in the same chip site and wafer were collected, and matched with corresponding ICO performance measurement. The ICO oscillation frequency and the device threshold voltage are plotted in Fig. 8. Statistical characteristics obtained with the measurement data are arranged in Table III.

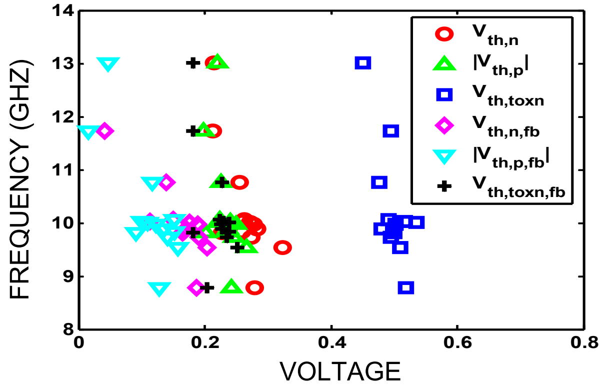

Fig. 8. Measured current-controlled oscillator oscillation frequency and FET device threshold voltage relation

TABLE III
ICO MEASUREMENT STATISTICS

	Cross-correlation	Sensitivity(GHz/V)
Vth_nfet	-0.718	-16.9
Vth_nfet_fb	-0.939	-12.4
|Vth_pfet|	-0.507	-16.9
|Vth_pfet_fb|	-0.885	-11.8
Vth_tox_nfet	-0.705	-27.7
Vth_tox_nfet_fb	-0.547	-24.2

The floating-body nFET threshold voltage showed 93.9% cross-correlation with the oscillation frequency. The floating-body device is equivalent to body-contacted device in terms of the threshold voltage at dc mode except an offset, since the body-contacted device is formed over the floating-body FET with an additional mask to make a body contact [7]. Not like the simulation statistics, physical circuit measurements and characterization are disturbed by noise, and the number of samples is smaller than the simulation, due to limited resources. Using both simulation and measurement data, the model-to-hardware correlation of ICO oscillation frequency and device threshold voltage can be extracted. Table IV shows cross-correlation between the ICO oscillation frequency and the threshold voltages from statistical simulation and circuit measurement. The maximum cross-correlation difference is 20.6%, and the minimum difference is 10.1%. Considering the number of samples and the close model-to-hardware correlation, the result suggests that the models and the physical devices match well.

TABLE IV
MEASUREMENT AND SIMULATION CROSS-CORRELATION DIFFERENCE

	Measurement	Simulation	Difference
Vth_nfet	-0.718	-0.835	0.117
Vth_nfet_fb	-0.939	-0.838	0.101
|Vth_pfet|	-0.507	-0.710	0.203
|Vth_pfet_fb|	-0.885	-0.683	0.202
Vth_tox_nfet	-0.705	-0.499	0.206
Vth_tox_nfet_fb	-0.547	-0.422	0.125

VI. CONCLUSION

The mixed-signal circuit process variation sensitivity was studied with regard to design, simulation, measurement, and statistical analysis for yield learning and improvement.

- Need for sub-100nm yield learning on site-to-site and wafer-to-wafer variation was examined with threshold voltage measurement data
- ICO process sensitivity was estimated with numerical circuit analysis in the design stage.
- ICO circuit was examined with statistical simulations, and the threshold voltage dependency was obtained.
- Implemented ICO performance and device parameter measurements were statistically analyzed.
- The statistical simulation and measurement-based statistical analysis showed good model-to-hardware correlation.

With the discussed design-to-test interface, practical yield analysis of mixed-signal system is enabled, and variation-resistant circuit development is expedited. The entire process as a whole is essential to enhance mixed-signal circuit yield learning and manufacturability.

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REFERENCES

[1] J. A. Carballo and S. R. Nassif, "Impact of design-manufacturing interface on SoC design methodologies," Design & Test of Computers, IEEE, vol. 21, pp. 183-191, 2004.

[2] S. R. Nassif, "Modeling and forecasting of manufacturing variations," CICC, 2001.

[3] J. O. Plouchart, J. Kim, et al., "Performance Variations of a 66GHz Static CML Divider in a 90nm CMOS," ISSCC, 2006.

[4] J. O. Plouchart, J. Kim, et al., "SOI 90-nm ring oscillator sub-ps model-hardware correlation and parasitic-aware optimization leading to 1.94-ps switching delay," IEDM, 2005.

[5] J. G. Maneatis, "Low-jitter process-independent DLL and PLL based on self-biased techniques," Solid-State Circuits, IEEE Journal of, vol. 31, pp. 1723-1732, 1996.

[6] J. O. Plouchart, J. Kim, et al., "A 31 GHz CML ring VCO with 5.4 ps delay in a 0.12-μm SOI CMOS technology," ESSCIRC, 2003.

[7] K. Bernstein and N. J. Rohrer, SOI circuit design concepts. Boston: Kluwer Academic Publishers, 2000.