4 WYSOCKI, P. F., DIGONNET, M. F. J., and KIM, B. Y.: 'Electronically tunable, 1·55 μm erbium-doped fiber laser', *Opt. Lett.*, 1990, **15**, pp. 273–275
5 PERCIVAL, R. M., CARTER, C. F., SZEBESTA, D., DAVEY, S. T., and STALLARD, W. A.: 'Thulium-doped monomode fluoride fibre laser broadly tunable from 2·25 to 2·5 μm', *Electron. Lett.* 1991, **27**, pp. 1912–1913
6 KAMINISKI, A. A.: 'Laser crystals' (Springer-Verlag, 1990)

CMOS ON-CHIP CLOCK FOR DIGITAL SIGNAL PROCESSORS

P. Nilsson, M. Torkelson, M. Vesterbacka and L. Wanhammar

Indexing terms: Digital circuits, CMOS circuits, Oscillators, Integrated circuits, Circuit design, Clocks

An on-chip clock for frequencies up to 190 MHz is presented. This clock generator can be used for application specific digital signal processors which are clocked faster than the off-chip system clock. It is useful for both processors with a few cycles per sample or for high frequency bit-serial processors which need a large number of cycles.

Introduction: An on-chip clock circuit, used in application specific digital signal processors, is vital in high speed and low power applications. When the clock frequencies reach the level of hundreds of megahertz, an off-chip clock is difficult to distribute and feed into the chip. This work shows an implementation of a clock which is to be placed on the chip close to the application. Because the clock works in a restricted area and never leaves the chip, it can operate at very high frequencies. The technique is also useful for low power applications because the clock can be specially designed for that purpose [1]. In addition, there is no need for power consuming drivers to feed the clock on to the chip. The clock precisely provides the required number of cycles and is thereafter turned off, a method which also helps save power. Furthermore, the technique reduces disturbances (clock crosstalk) because the clock is local and therefore is easy to shield.

The clock shown here is useful for two phase designs using, for instance, NORA logic [2]. However, with a simple modification, it can be changed to single phase designs [3]. Only one signal is needed to control the clock. This signal is used as a trigger which starts a well defined burst of cycles. The clock circuit is easy to implement with a module generator and it does not occupy much area; it is even possible to use several clocks at different parts on the chip.

Circuit design: The basic idea is to use a ring oscillator as the oscillating element. A major drawback with this type of oscillator is that it is difficult to control the frequency with high accuracy. However, this is not a necessity in this case where only the number of cycles is of importance. A specific number of cycles must occur within a sample period and after that the clock is put in its inactive mode.

The oscillator, shown in Fig. 1, contains a small buffer stage which provides a clock signal both to the cycle counter and to the clock buffer, which in turn distributes the clock locally on the chip. Of course, the distributed clock has a small delay compared to the start pulse, but that is of no importance because it does not intefere with the clock control. The Figure shows a two-phase clock, but a single phase clock is simply designed if two buffer inverters are removed and the other is redesigned for high driving capability.

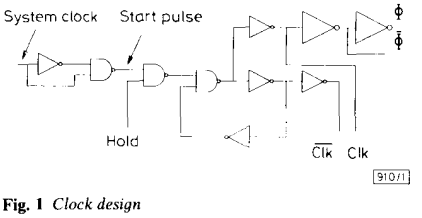

Fig. 1 *Clock design*

A modified ring oscillator with a minimum of three inverting elements is used. It is designed with a NAND gate coupled in a feedback loop through two inverters. The NAND gate is used for start and stop control. The number of inverting elements may of course be increased to slow down the clock, but for low power consumption [1] it is better to use slow inverting elements.

The clock which is resting at the beginning needs a pulse, for instance from the system clock, to start. Unfortunately, a long external clock pulse cannot be used directly. To form a sufficient pulse a flank-trigged monostable flipflop is used. Such a pulse must be long enough to start the clock properly, but shorter than the total time for the cycle burst. This may cause some design problems for short bursts, but in most cases the pulse length is easily achieved.

The clock circuit also needs a signal that keeps the clock running after the start pulse has ended. This pulse has to be active until the correct number of cycles have been generated. The signal is shown as *Hold* in Fig. 1 and it is supplied by the cycle counter (a ring counter) in Fig. 2.

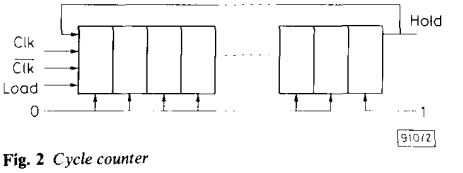

Fig. 2 *Cycle counter*

The ring counter consists of a number of full latches which match the required number of cycles in the burst. Initially, the latches are loaded with a word corresponding to the *Hold* waveform which is zeros in all latches except for the last one. It is important that the latch initialisation is independent of the clock because the clock cannot be properly started before the *Hold* waveform is correct. The start pulse starts the clock which in turn shifts the word around in the cycle counter. The *Hold* signal then holds the clock in running state until the word is shifted a full cycle.

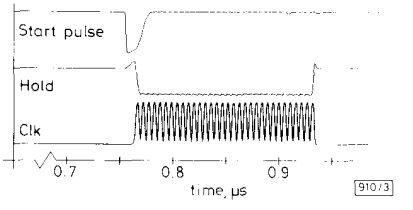

Fig. 3 *Simulation plot*

Simulation example: A high speed clock is shown as an example. Fig. 3 shows a part of the simulation plot of a 190 MHz 32 cycle burst generator running in a 1·0 μm standard CMOS process. The top trace shows the *Start pulse* from the monostable device, the middle is the *Hold* signal from the cycle counter, and the bottom trace is the resulting burst of 190 MHz clock pulses. Note that at least one of the *Start pulse* and the *Hold* signal is low during the active period. The first starts the process and the other takes over and keeps the clock in running mode until all the 32 pulses have been generated.

Floorplan: The design, from where the netlist for the simulation above is extracted, is sent to a 1·0 μm CMOS fabrication. Fig. 4 shows a floorplan of the clock generator. The top block

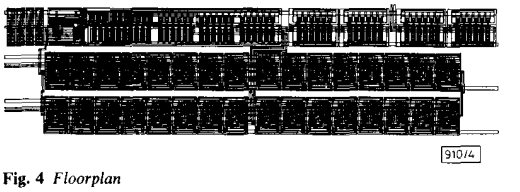

Fig. 4 *Floorplan*

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is the clock generator with its buffers and the two blocks show the ring counter. The size is $0.9 \times 0.2\,mm^2$ in a $1\,\mu m$ process and is, of course, dependent of the number of cycles in the burst. On the other hand, the size will still be a minor part of a DSP chip. The implementation is well suited for module generation where the burst length is simply controlled by a parameter. This floorplan is designed with the ASIC design system decribed in Reference 4.

Summary: A method to generate clock signals on-chip is presented. This method is useful for application specific digital signal processors which use frequencies above the off-chip system clock. In high speed or low power designs, this clock has been shown to be advantageous. The clock is robust and simple to implement. Furthermore, it occupies a small chip area.

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P. Nilsson and M. Torkelson (*Department of Applied Electronics, University of Lund, Box 118, 22100 Lund, Sweden*)

M. Vesterbacka and L. Wanhammar (*Department of Applied Electronics, University of Linköping, 58183, Linköping, Sweden*)

References

1 CHANDRAKASAN, A. P., SHENG, S., and BRODERSEN, R. W.: 'Low-power CMOS digital design', *IEEE J. Solid-State Circuits*, 1992, **27**, (4), pp. 473–484

2 GONCALVES, N. F., and DE MAN, H. J.: 'NORA: A racefree dynamic CMOS technique for pipelined logic structures', *IEEE J. Solid-State Circuits*, 1983, **SC-18**, pp. 261–266

3 AFGHANI, M., and SVENSSON, C.: 'A unified single-phase clocking scheme for VLSI systems', *IEEE J. Solid-State Circuits*, 1990, **25**, (1), pp. 225–233

4 ÖWALL, V., ANDREANI, P., NILSSON, P., WASS, A., and TORKELSON, M.: 'Custom DSP implementation of a GSM speech coder'. Proc. EDAC-EUROASIC, February 1993

MINIATURISED TWO-STAGE BALANCED Ku-BAND CPW MMIC AMPLIFIER USING IMPEDANCE TRANSFORMING COUPLERS

M. Gillick, I. D. Robertson and J. S. Joshi

Indexing terms: Microwave circuits, Amplifiers, Monolithic microwave integrated circuits, Coplanar waveguides

A two-stage balanced Ku-band coplanar waveguide amplifier design is presented which has been miniaturised by using impedance transforming couplers which considerably reduce the required matching networks to the MESFETs. The amplifier, measuring only $2 \times 1.7\,mm^2$, exhibits a gain of 13.7 dB with less than ± 0.2 dB of ripple over the range 14–16 GHz.

Introduction: Coplanar waveguides (CPWs) have recently been receiving widespread attention for GaAs monolithic microwave integrated circuits (MMICs). The CPW medium is favourable because of source inductance reduction, no via-hole requirements, and its inherent property of minimising line-to-line coupling. Recent successful MMICs with CPW as their transmission media include a 5–100 GHz InP distributed amplifier [1], and a Q-band AlGaAs/GaAs HEMT down-convertor [2]. In the design of such CPW MMICs it is important to keep the circuit layout compact.

Balanced amplifiers are attractive because of their excellent cascadability, high power and good stability. However, the standard balanced amplifier configuration with its two identical amplifiers placed between two quadrature 3 dB couplers has the disadvantage of requiring a large chip area due to the size of the coupler. In this Letter a new balanced amplifier topology is presented which employs reduced-size impedance transforming coplanar waveguide branchline couplers. Such couplers, employing short high impedance CPW transmission lines and shunt-lumped capacitors occupy less than 25% of the area of the standard branchline coupler [3]. Furthermore, the method presented here of applying impedance transforming couplers to balanced amplifiers significantly reduces the required input and output matching networks compared to 50 Ω input/output couplers, and overcomes the size disadvantage associated with conventional balanced amplifiers.

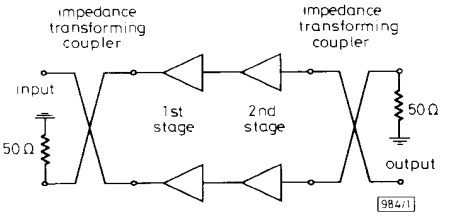

Fig. 1 *Schematic circuit diagram of MMIC two-stage balanced Ku-band amplifier*

Balanced amplifier design: The schematic circuit diagram of the MMIC two-stage balanced amplifier with its two impedance transforming reduced-sized branchline couplers is shown in Fig. 1. A simplified schematic diagram of each of the balanced amplifier arms is shown in Fig. 2. This circuit topology provides both the optimum matching networks, and DC blocking and DC biasing for a minimum layout size. Shorted stubs and series transmission lines are used for the distributed matching elements. For the actual choice of the optimum characteristic impedance of the CPW lines, it is necessary to keep Z_0 high to maintain a high inductance per unit length, while keeping the CPW gap and centre conductor small in order to keep the chip area small, and to minimise any junction discontinuities and coupling effects. The choice of Z_0 results from a tradeoff between low insertion loss and small chip size, and a value of $Z_0 = 55\,\Omega$ was chosen here. To achieve a compact layout it is necessary to bend the distributed matching elements. This is best achieved for CPW lines with small gap widths whose transversal field distribution is closely confined [4], thus reducing any coupling effects and therefore allowing the positioning of relatively close parallel CPW lines. At each right angled CPW bend a $4\,\mu m$ wide underpass strap connects both CPW ground planes.

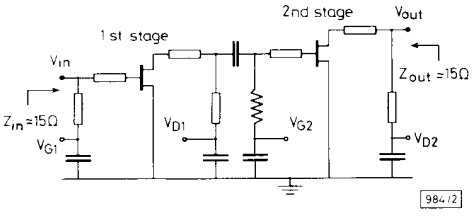

Fig. 2 *Simplified schematic diagram of two-stage balanced amplifier arm*

Throughout the design process the number of junction and bend discontinuities was minimised while attempting to maintain a compact MMIC layout. Although the monolithic coupler has been realised in a completely uniplanar configuration, the amplifier chip has via holes connecting the upper CPW ground planes to the back face metallisation. This conductor-backed CPW provides an improved mechanism for removing heat produced from the MESFET devices in such CPW MMICs. Four-finger ion-implanted MESFETs with a gate length of $0.5\,\mu m$ are used. Because the MESFET sources are connected directly to the upper metallisation ground plane the source inductance is minimised.

Matching network optimisation: All the matching networks were synthesised and optimised to produce maximum small-

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