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Ch. Hu-Guo, J. Baudot, G. Bertolone, A. Besson ...+21 more authors

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# CMOS pixel sensor development: a fast read-out architecture with integrated zero suppression

**Ch. Hu-Guo,**[a,1] **J. Baudot,**[a] **G. Bertolone,**[a] **A. Besson,**[a] **A.S. Brogna,**[a] **C. Colledani,**[a] **G. Claus,**[a] **R. De Masi,**[a] **Y. Degerli,**[b] **A. Dorokhov,**[a] **G. Doziere,**[a] **W. Dulinski,**[a] **X. Fang,**[a] **M. Gelin,**[b] **M. Goffe,**[a] **F. Guilloux,**[b] **A. Himmi,**[a] **K. Jaaskelainen,**[a] **M. Koziel,**[a] **F. Morel,**[a] **F. Orsini,**[b] **M. Specht,**[a] **Q. Sun,**[a] **I. Valin**[a] **and M. Winter**[a]

[a]*Institut Pluridisciplinaire Hubert Curien, University of Strasbourg, CNRS/IN2P3,*
  *23 rue du lœss, BP 28, 67037 Strasbourg, France*
[b]*IRFU/SEDI,*
  *CEA Saclay, 91191 Gif-sur-Yvette Cedex, France*

  *E-mail:* Christine.Hu@IReS.in2p3.fr

ABSTRACT: CMOS Monolithic Active Pixel Sensors (MAPS) have demonstrated their strong potential for tracking devices, particularly for flavour tagging. They are foreseen to equip several vertex detectors and beam telescopes. Most applications require high read-out speed, which imposes sensors to feature digital output with integrated zero suppression. The most recent development of MAPS at IPHC and IRFU addressing this issue will be reviewed. The design architecture, combining pixel array, column-level discriminators and zero suppression circuits, will be presented. Each pixel features a preamplifier and a correlated double sampling (CDS) micro-circuit reducing the temporal and fixed pattern noises. The sensor is fully programmable and can be monitored. It will equip experimental apparatus starting data taking in 2009/2010.

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[1]Corresponding author.

## Contents

## 1 Introduction

Subatomic physics experiments express a growing need for very high performance flavour tagging, with emphasis on short lived particles (e.g. charmed mesons) through their decay vertex. This calls for an excellent vertexing and tracking system in order to reconstruct displaced vertices and to measure precisely track momenta. As compared to the state of the art, the system accuracy is required to be improved by up to an order of magnitude.

Existing pixel technologies are not adequate for this new challenging requirement level. The next generation of pixel technologies needs to be simultaneously highly granular, ultra-light, radiation tolerant and fast to match the environment and physics constraints of future poly-layer vertex pixel detectors which will be installed very close to the beam interaction point. MAPS provide an attractive trade-off between granularity, material budget, read-out speed, radiation tolerance and power dissipation, which may suit these challenging requirements.

Their most original aspect is that the sensitive volume and the front-end read-out electronics are integrated on the same substrate. The charges generated by an impinging particle in the epitaxial layer (typically 5 to 15 $\mu$m thin) underneath the read-out electronics are collected through thermal diffusion by regularly implanted N-well/P-epi diodes. These charges are then converted, "in situ", into voltage signal at the capacitance of the sensing diode. The signal can then be processed by the integrated read-out electronics. Being fabricated in standard CMOS processes available through many commercial microelectronics foundries, MAPS are attractive for their cost effectiveness and for the fast multi-project run turn-around.

MAPS tracking performance are now well established [1]. Due to their particularly low equivalent noise charge (ENC), the most probable value (MPV) of the signal-to-noise ratio (S/N) ranges
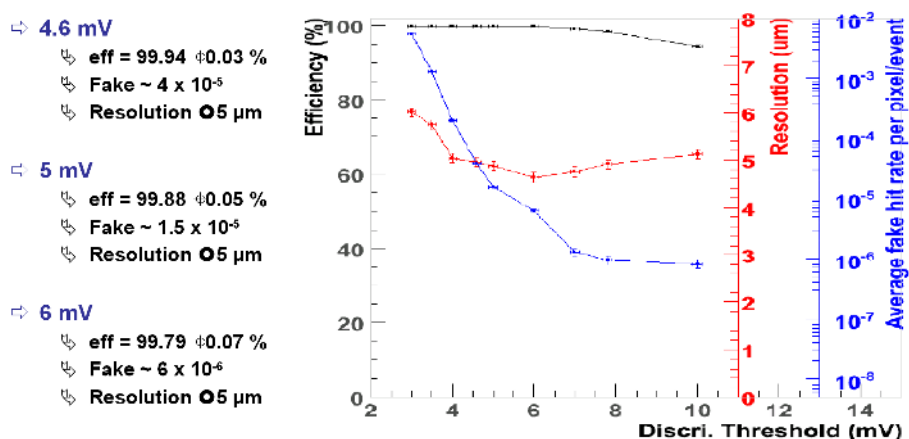
**Figure 1**. MIMOSA16: pixel digital read-out performance extracted from beam test data.

from 15 to 30, depending on the pixel size. A detection efficiency exceeding 99.5% was demonstrated [1], even in the case of a pitch as large as $40\,\mu$m, at an operating temperature of up to $40\,^{\circ}$C. The single point resolution was measured to range from $\sim 1\,\mu$m for a $10\,\mu$m pixel pitch, up to $\sim 3\,\mu$m for a $40\,\mu$m pitch, in case of sensors with analogue read-out.

Although analogue read-out MAPS show excellent performances, they suffer from moderate read-out speed in case of large pixel arrays. Numerous applications need simultaneously a high granularity and a fast read-out speed. In order to fulfil these conflicting requirements, sensors have to integrate signal processing functionalities: CDS, ADC (Analogue to Digital Converter) and zero suppression circuitry. These functionalities will translate into severe constraints on the pixel dimensions, clock frequency and power consumption. A prototype sensor, called MIMOSA16 [2], with 24 integrated column-level discriminators, had been realised to check detection performance for sensors featuring digital read-out. Figure 1 shows the detection efficiency, the single point resolution and the average fake rate as a function of the discriminator threshold, measured with $\sim 120\,$GeV pion beam at the CERN-SPS. The detection efficiency is close to 100% up to a threshold value of $6\,$mV, corresponding to $\sim 6$ times the noise standard deviation, with a fake rate below $10^{-5}$ and a spatial resolution better than $5\,\mu$m. The latter is substantially better than the pure digital resolution (pixel pitch of $25\,\mu$m) due to charge sharing among pixels in a cluster.

These results validate the proposed MAPS architecture allowing to extend it to a large area pixel array (reticle size) with column-level discriminators, a data sparsification circuitry and a serial data transmission on the same substrate.

MAPS are foreseen for several applications, ranging from subatomic physics experiments to bio-medical imaging devices. The vertex detector upgrade of the STAR (Solenoidal Tracker at RHIC) experiment at RHIC (Relativistic Heavy Ion Collider) and the construction of the EUDET beam telescope, an EU R&D program, offer the first opportunities for operating such devices in real experimental conditions.

In the first part of the paper, the applications to the experiments above will be described. In the second part, the MAPS architecture developed by the IPHC-Strasbourg and IRFU-Saclay collaboration, will be discussed in detail.
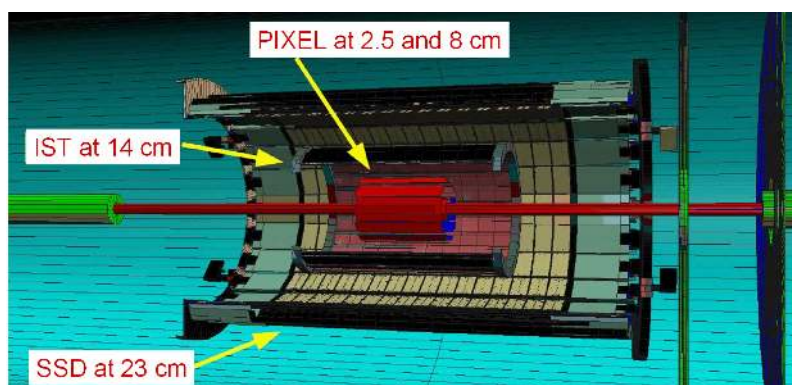
**Figure 2**. The Heavy Flavor Tracker (HFT).

## 2 Examples of MAPS applications

### 2.1 STAR Heavy Flavor Tracker (HFT) upgrade

The STAR HFT upgrade is intended to allow for direct topological reconstruction of D (and B) mesons through the identification of decay vertices displaced from the primary interaction vertex by 100–150 $\mu$m [3]. In order to achieve a vertex pointing resolution of about 30 $\mu$m or better, two nearly cylindrical MAPS layers with average radii of about 2.5 cm and 8 cm, will be inserted in the existing detector (figure 2). There will be no space available for a sophisticated cooling system, only air cooling will be used. This imposes MAPS to be operational at room temperature and to keep their power dissipation in the order of 100 mW/cm$^2$. Multiple Coulomb scattering imposes a material budget as low as $\sim 0.3\%$ of radiation length per layer, assuming 50 $\mu$m thin sensors. The final pixel sensors, expected to be operated with Au + Au collisions at a RHIC II luminosity of $\sim 8 \times 10^{27}$ cm$^{-2}$s$^{-1}$, will face a hit density in the order of $10^6$ hits/s/cm$^2$ in the inner layer. The total ionising dose was estimated to 150–300 kRad per year and the non-ionising radiation dose should mainly come from an annual flux of 3–12 $\times 10^{12}$ charged pions per cm$^2$ traversing the inner layer [4].

The pixel vertex detector upgrade relies on three main steps. The first step was achieved by operating successfully a MAPS telescope in the STAR environment during the 2007 Au + Au RHIC run [5]. The telescope consists of three planes made of MimoSTAR2 chips [6]. Each chip provides a $128 \times 128$ pixel array with 30 $\mu$m $\times$ 30 $\mu$m pixels. With its serial analogue outputs, MimoSTAR2 was a first generation sensor. The second step, foreseen in 2009, is to equip three sectors ($\sim 30\%$ of the surface) of the HFT with second generation MAPS, named "PHASE1". They feature a $640 \times 640$ pixel array with 30 $\mu$m pitch. These sensors, ready for test, contain in-pixel CDS and column-level discriminators. The read-out is done in rolling shutter mode with an integration time of 640 $\mu$s. Finally, in 2010, the whole HFT vertex detector will be equipped with faster and more granular sensors, named "ULTIMATE". They will contain all attributes of the PHASE1 sensors, but with a faster rolling shutter clock which allows compressing the read-out time to 200 $\mu$s. An integrated zero suppression circuitry will be implemented in the sensor. The chip will include a $1152 \times 1024$ pixel array with 18.4 $\mu$m $\times$ 18.4 $\mu$m pixels.

## 2.2 EUDET telescope

The purpose of EUDET [7] is to provide to the scientific community an infrastructure exploiting R&D on the different detectors for the future international linear collider (ILC). It includes a vertexing activity aiming to construct a CMOS pixel beam telescope with six planes of sensors, to be operated at the DESY electron test beam facility. The beam telescope, providing an extrapolated resolution better than $2\,\mu$m, is to be used for a wide range of R&D applications.

In order to minimise the risk, the construction of the telescope was organised in two stages. In the first stage, a demonstrator telescope, exploiting the existing MAPS with analogue read-out, has been realised. It has been successfully operating since 2007 [8]. In 2009, the final telescope will be equipped with sensors providing an active surface 4 times larger and a read-out speed ($\sim 100\,\mu$s) about an order magnitude faster than the previous one. The sensors will include a $1152 \times 576$ pixel array with $18.4\,\mu$m pitch, and will incorporate CDS, digital fast read-out and integrated data zero suppression circuitry. Their architecture will be extended to the ULTIMATE sensor for STAR.

## 3 Fast Read-out MAPS architecture

The development of the Fast Read-out MAPS is based on two separate prototyping lines: one addressing the upstream part of the signal detection and processing chain, and the other devoted to data sparsification and formatting. Two prototype circuits, MIMOSA22 and SUZE-01, were fabricated in the AMS CMOS $0.35\,\mu$m technology, addressing these two research lines.

The MIMOSA22 sensor explores analogue signal processing. It is composed of 128 columns of 576 pixels, each column ended with a discriminator. The pixel ($18.4\,\mu$m $\times 18.4\,\mu$m) contains a pre-amplifier and CDS circuitry. The matrix is read out in rolling shutter mode, the row being selected sequentially by a shift register. SUZE-01, which is the sparsification chip, incorporates the zero suppression logic, the memory buffers and the serial transmission.

The reticule size Fast Read-out MAPS will merge the 2 previous designs according to three main issues:

- Increasing the S/N at pixel-level

- Analogue to digital conversion (discriminator) at the column level

- Zero suppression at chip edge level

### 3.1 Pixel

Pixel-level amplification and CDS are necessary to increase the S/N in order to achieve column-level digitisation. CDS suppresses low frequency noise, reset noise and fixed pattern noise (FPN). The difficulty of in-pixel signal processing is that only NMOS transistors can be used, since any additional N-well used to host PMOS transistors would compete for charge collection with the sensing N-well diodes.

The pixel architecture is illustrated in figure 3(a). A preamplifier stage is implemented nearby the sensing diode. It is active only when the row is selected to be read, which reduces significantly the power consumption. The double sampling is achieved with a serially connected capacitor made by a NMOS and a clamping switch. A source follower and a row select switch are used to output
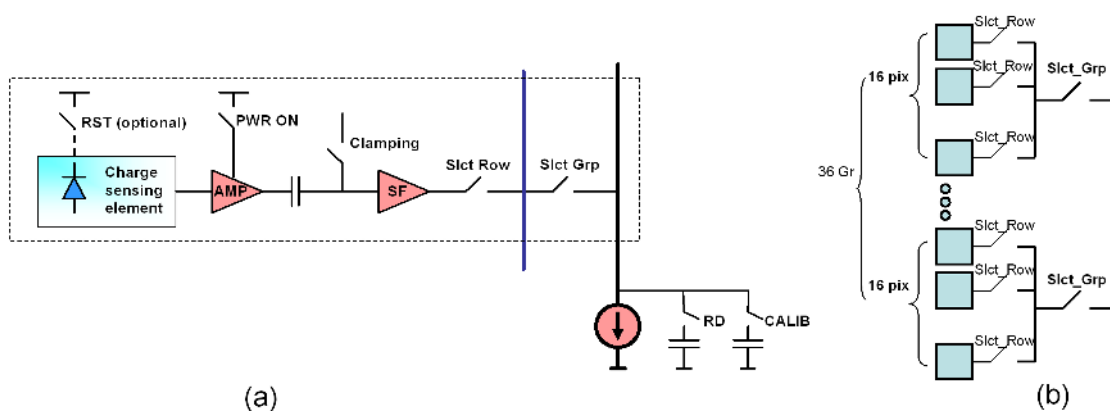
**Figure 3**. Pixel topology.

the signal. For such a large pixel array ($\sim 2 \times 2\,\text{cm}^2$), the column is split into 36 groups. Each of them has a dedicated switch to a column data bus, which allows replacing the parasitic capacitance of 16 pixel switches by the capacitance of a single switch (figure 3(b)).

"RD" and "CALIB" in figure 3 are column-level commands to store the pixel output signal and the reference levels, respectively. This second double sampling operation reduces the pixel to pixel dispersion (FPN). The row read-out operation requires 16 clock cycles at up to 160 MHz. The timing diagram and more details on the CDS can be found in [9].

Figure 4 displays in-pixel amplifier design variants, addressing the following goals:

- reaching maximal S/N for a given N-well sensing diode size;

- minimising the power consumption;

- reducing the pixel to pixel dispersion.

Figure 4(a) shows a standard common source (CS) amplifier [9]. The AC gain of the amplifier can be increased by implementing extra transistor M4 (figures 4(b) and (c)) as described in details in [10]. It works in saturated sub-threshold mode, and therefore, the gate of M3 has the DC potential close to Vdd. As a result the DC operating point and DC gain of M2 is almost unchanged. The AC output conductance of M4 working in saturated sub-threshold mode is very small, so the gate of M3 is strongly AC coupled to the source of M3 via parasitic capacitance. For the standard amplifier the gate of M3 is AC coupled to ground. Therefore, the output conductance of M3 for the improved schematic is smaller; hence, the AC gain of amplifier increases. An even more robust pixel is shown in figure 4(c), where a negative low frequency feedback was introduced to decrease the operating point variation due to process dispersion. In addition, the feedback ensures biasing of the sensing diodes [11].

The three pixel variants were implemented in the MIMOSA22 prototype, and tested with an $^{55}$Fe source (5.9 keV X-ray) at 20 °C. The power consumption per activated pixel, i.e. ready for read-out, is about 200 $\mu$W. Table 1 illustrates the measured performances. The chip was also irradiated with a 10 keV X-ray source. Figure 5 shows the measured temporal noise and FPN of the three pixels as a function of the ionising dose. The feedback self biased structure (figure 4(c))
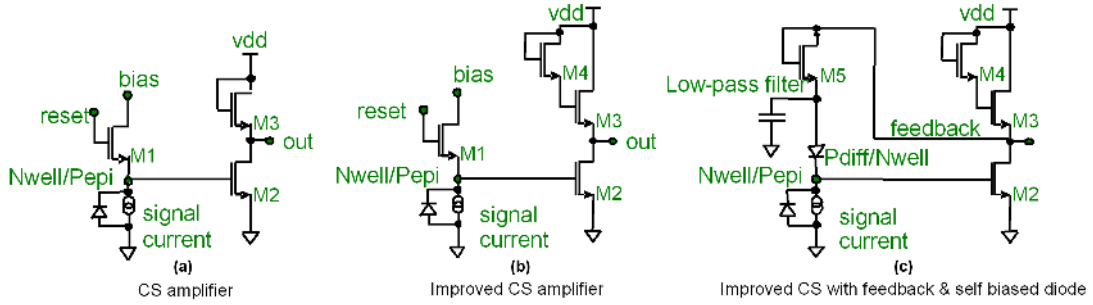
**Figure 4**. Pixel amplification.

**Table 1**. Measured performances of the MIMOSA22 sensor.

| Pixel types | Diode size ($\mu m^2$) | CVF* ($\mu V/e^-$) | ENC ($e^-$) |
|---|---|---|---|
| CS (a) | 15.21 | 57.3 | $13.3 \pm 0.1$ |
| Improved CS (b) | 15.21 | 57.3 | $13.0 \pm 0.1$ |
| Feedback & self biased (c) | 14.62 | 55.8 | $12.3 \pm 0.1$ |

*CVF: Charge-to-Voltage conversion Factor.

exhibits the best behaviour. It has the smallest increase of the temporal noise and the FPN remains unchanged. It will therefore be implemented in the Fast Read-out MAPS.

Enhancing of the tolerance to ionising radiation damage is among the main pixel design goals. In order to improve the pixel circuit, the feedback transistor (M5), serially connected to the sensing diode, should be an enclosed layout transistor (ELT) surrounded by a guard ring. This will minimise the drain-source leakage current. To increase the radiation tolerance of the sensing diode, the thick oxide surrounding it by default needs to be replaced by thin oxide (gate oxide ring). The improvement of the performance of this radiation tolerant diode design has already been reported in [12]. The results provided in table 1 and figure 5 correspond to pixels with radiation tolerant N-well diodes.

The effect of non ionising radiation damage can be alleviated by decreasing the pixel pitch and the integration time, and by enlarging the sensing diode area [13]. This is why the pixel pitch of MIMOSA22 was reduced to 18.4 $\mu$m in comparison with MIMOSA16.

### 3.2 Analogue to Digital Conversion

Like in MIMOSA22, ADCs will be implemented in the Fast Read-out MAPS below the pixel array. Pixel signals of the selected row are transmitted to the bottom of the matrix, where 1152 ADCs will convert them at the row read-out speed with low power consumption. The ADC layout has to fit in the pixel pitch (18.4 $\mu$m). Its number of bits will follow from the required spatial resolution. It is about 4 $\mu$m for the EUDET beam telescope, and somewhat below 10 $\mu$m for the STAR application. In these cases, the best solution is a 1 bit ADC, i.e. just a comparator, for its low power consumption and simplicity. The 1152 discriminators will use a common threshold value for comparisons. It will be adjustable and will be set to its optimal value in order to ensure $\sim 100\%$ of detection efficiency and low fake rate ($\sim 10^{-4}$–$10^{-5}$).
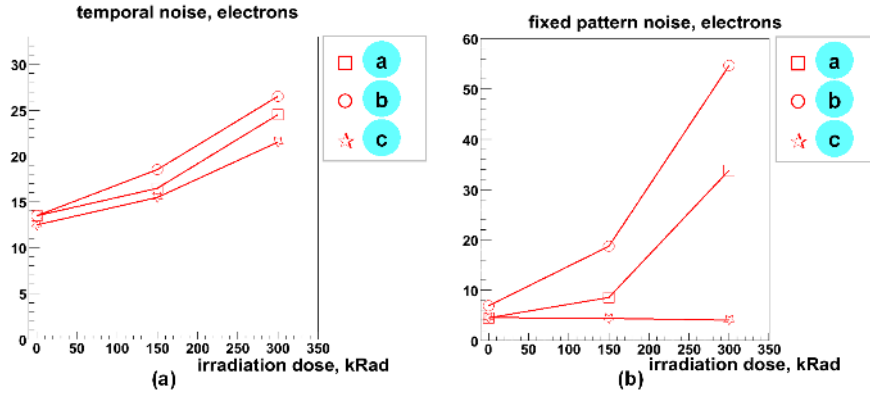
**Figure 5**. Temporal noise & FPN of amplifiers as a function of irradiation dose (10 keV X-Ray).
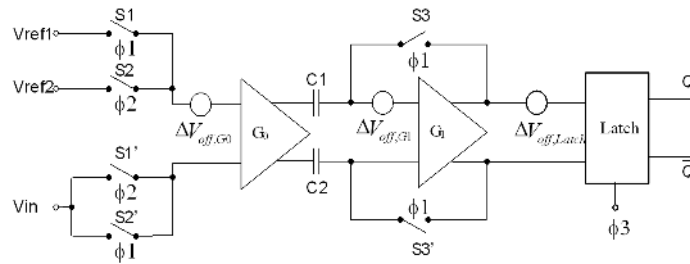


**Figure 6**. Architecture of the column-level discriminator.

The discriminator design has been detailed in [9]. Considering the small amplitude of the analogue signal, it is mandatory to use an offset compensated amplifying stage (figure 6) which corrects the residual offsets. Its power consumption is below 250 $\mu$W.

The 128 discriminators implemented in MIMOSA22 were evaluated by scanning the common threshold voltage. The "S-curves" were fit with an error function to extract the offset, temporal noise and FPN. The extracted temporal noise and the FPN values amount to 0.3 mV and 0.2 mV respectively.

The noise performance of the pixel array connected to the discriminator was also evaluated. The temporal noise is about 0.64 mV which comes mainly from the pixel noise ($\sim$ 0.69 mV, measured from pixel output), while the FPN (0.22 mV) comes from discriminators. MIMOSA22 was tested on a $\sim$ 120 GeV pion beam at CERN-SPS. Results show that the detection efficiency is better than 99.5% for a threshold value corresponding to about 6.5 times the noise standard deviation. The spatial resolution is better than 4 $\mu$m while the fake rate is below $10^{-4}$. In order to extend the architecture from 128 up to 1152 columns, thorough studies were conducted. In particular, in order to minimise the interference originated by closing thousands of switches (S1, S2 of figure 6), the reference voltage signals Vref1 and Vref2 were buffered and split into four groups.

### 3.3 Zero suppression

In order to reduce the raw data flow of MAPS for STAR and EUDET, which may reach up to several Gb/s per chip, the zero suppression circuitry will be located right after the discriminators.
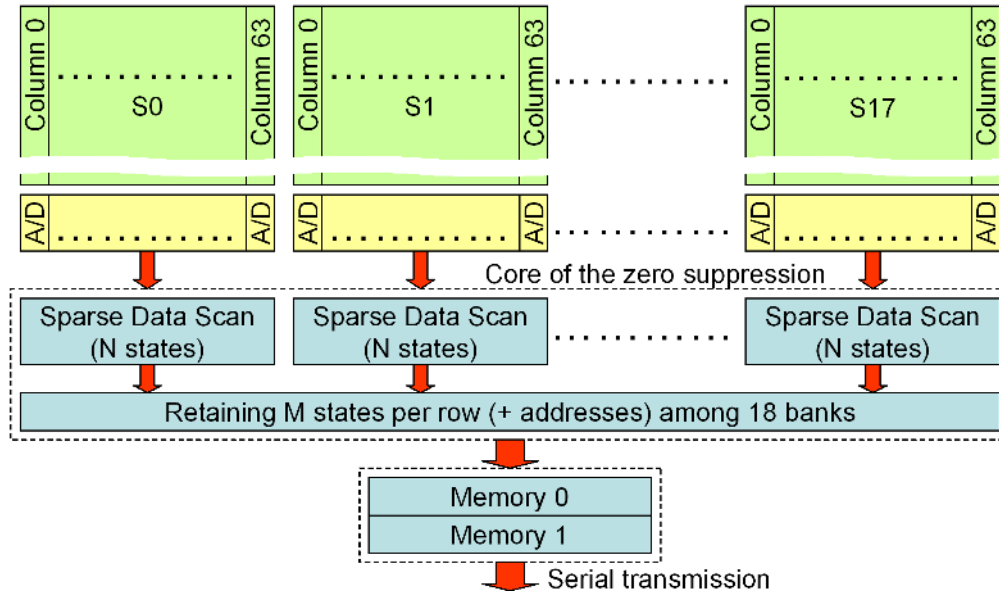
**Figure 7**. Block diagram of the sensor read-out architecture.

The circuitry will be organised in a 3 stage pipeline. The purpose is to skip non hit pixels in order to obtain a data compression factor ranging from 10 to 1000, depending on the hit density per frame. In the first stage, the 1152 discriminator outputs will be distributed over 18 banks (see figure 7), where a sparse data scan algorithm on hit pixels is performed [14]. Up to 4 contiguous pixel signals above threshold (string) will be encoded in a 2 bit state word. Up to N states per bank can be memorised with column addresses. The column address of a string shared by two neighbouring banks will be transferred only once. The second stage will combine the outcomes of the 18 banks of the first stage. Its multiplexing logic accepts up to M states per pixel row and adds bank address information. In the Fast Read-out MAPS, N and M will respectively be equal to 6 and 9, according to the hit density defined by the estimated (simulated) amount of events. The results of the second stage will be stored in the third stage, i.e. a 96 kbit memory split in 2 buffers, allowing a continuous read-out via a LVDS link at 160 MHz. The values of N and M, the memory capacity and the transfer frequency must be customized for each application.

A reduced scale prototype (2 banks) called SUZE-01, has been realised to verify the concept described above. All critical paths of the design were tested. The hits for a matrix were emulated and processed row by row by SUZE-01 at clock frequencies of up to 115 MHz. The result shows that the zero suppression circuit compresses the estimated EUDET and STAR data flows without any loss of information. The simulated power consumption for the full size logic is about 135 mW.

### 3.4 General considerations

For the reticule size chips, one needs focusing on design optimisation in order to improve the trade-off between power consumption and speed. For example, the Row Sequencer (RS) which drives about 2 cm metal lines to control the pixels, may consume a significant amount of power. The power consumption of the digital circuit has to be minimised while ensuring that it still provide correct timing. Since the AMS-035 process is limited to 4-metal levels and the digital processing

circuitry is located at the bottom of the pixel array, the RS was implemented at the side of the pixel array ($\sim 350\,\mu$m wide). This generates a small insensitive band in the sensitive area when the MAPS are abutted in order to encompass a larger detection area. The power consumption for the RS with its clock distribution is about 10 mW. The total power consumption estimated for the ULTIMATE sensor is around 170 mW/cm$^2$, which is 70% higher than the STAR final goal. Studies are in progress to improve this value.

The testability is another point to be considered. Several test points will be implemented in the design along the read-out path, i.e. pixels, discriminators, zero suppression circuit and data transmission. The biasing and test mode settings will be programmable, via a boundary scan controller, like in previous sensors [6].

For the MAPS used for the STAR vertex upgrade, some additional tests, like Single Event Upset (SEU) and Single Event Latch-up (SEL), have still to be performed. Some digital circuit layout may have to be redesigned consecutively, especially the memory block.

## 4   Conclusions

In this paper, a Fast Read-out architecture of MAPS which integrates on-chip data sparsification has been presented. Its feasibility was verified with two prototypes of intermediate size which share the upstream and the downstream parts of the signal collection and conditioning. The read-out speed reaches 10 kframe/s. This architecture seems to be an optimal choice for present CMOS technologies. The final MAPS for the EUDET telescope will be sent for fabrication before the end of 2008 and the ULTIMATE sensors for the STAR upgrade is scheduled for 2009.

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