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Article

CMOS Radio Frequency Energy Harvester (RFEH) with Fully On-Chip Tunable Voltage-Booster for Wideband Sensitivity Enhancement

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Abstract: Radio frequency energy harvesting (RFEH) is one form of renewable energy harvesting currently seeing widespread popularity because many wireless electronic devices can coordinate their communications via RFEH, especially in CMOS technology. For RFEH, the sensitivity of detecting low-power ambient RF signals is the utmost priority. The voltage boosting mechanisms at the input of the RFEH are typically applied to enhance its sensitivity. However, the bandwidth in which its sensitivity is maintained is very poor. This work implements a tunable voltage boosting (TVB) mechanism fully on-chip in a 3-stage cross-coupled differential drive rectifier (CCDD). The TVB is designed with an interleaved transformer architecture where the primary winding is implemented to the rectifier, while the secondary winding is connected to a MOSFET switch that tunes the inductance of the network. The TVB enables the sensitivity of the rectifier to be maintained at 1V DC output voltage with a minimum deviation of −2 dBm across a wide bandwidth of 3 to 6 GHz of 5G New Radio frequency (5GNR) bands. A DC output voltage of 1 V and a peak PCE of 83% at 3 GHz for −23 dBm input power are achieved. A PCE of more than 50% can be maintained at the sensitivity point of 1 V with the aid of TVB. The proposed CCDD-TVB mechanism enables the CMOS RFEH to be operated for wideband applications with optimum sensitivity, DC output voltage, and efficiency.

Keywords: radio frequency energy harvester; CMOS; voltage boosting; wideband; CCDD; 5GNR

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1. Introduction

Since the 3rd Generation Partnership Project (3GPP) standardized the first New Radio (NR) version (Release 15) in mid-2018, the evolution of the fifth-generation (5G) new radio (NR) has been rapid. 5GNR technology was designed to operate in two distinct bands: FR1 (410 to 7125 MHz) and FR2 (24,250 to 52,600 MHz). Despite operating into the 7 GHz band, FR1 is commonly referred to as the "Sub-6 GHz" band. The leading carriers compete to provide various commercial services over 5G networks. In the future, it is expected that over 6.5 million 5G base stations will be installed, allowing over 58% of the world's population to access services via over 100 billion 5G connections [1]. Following 5G's rapid development, many commercialization use cases will push the 5G network to improve performance and expand capabilities continuously.

It is no secret that the worldwide demand for electronic devices has been rising, which means that the global use of electrical energy has been growing alongside it. According to studies cited in [2], by 2030, communication technologies might account for as much as 51% of the world's total electricity consumption. The study also indicates that by 2030, the

power used by communication technologies might account for up to 23% of worldwide greenhouse gas emissions. As a result, reducing the energy needed to run all these gadgets connected to the internet is an absolute necessity. Furthermore, these connected devices are powered by batteries, contributing to increased waste and environmental pollution. Since the introduction of the first commercial lithium-ion (Li-Ion) batteries in 1991, the number of portable electronic device products that use Li-Ion batteries has grown dramatically [3].

Since the battery life of connected electronic devices can be vastly improved by reducing the frequency with which they need to be charged, it is crucial to lower their power consumption. Several energy harvesting works have been successfully implemented recently, including the triboelectric nano-generators (TENG) devices [4,5]. TENG devices are commonly utilized for biomechanical energy harvesting applications. In [4], a nanocomposite that acts as a positive triboelectric layer was successfully used in the fabrication of the TENG device, which converts waste mechanical energy into valuable electrical energy. The TENG device consumes an area of 4cm^2 while capable of delivering an output voltage of 35 V as well as 130 nA output current at 100 MΩ load. Moreover, in [5], a ZIF-8 HG-Kapton TENG device with dual-mode operation was proposed. A triple-unit TENG is constructed using additive manufacturing, producing an output voltage of 150 V and a current of 4.95 μA. The single-unit mode is implemented to detect a robotic system's right and left tilting motion. Meanwhile, the triple-unit mode is utilized as a sustainable power source to power up low-power electronics. However, the TENG devices mainly focus on harvesting the wasted mechanical motions, which is not present in on-chip microelectronics integrated circuits.

Radio frequency energy harvesting (RFEH) is a particularly prevalent type of renewable energy harvesting at the moment [6–11] because RFEH can be unified into a single wireless communication system used by all interconnected electronic devices. RFEH is widely studied and implemented in integrated circuits to improve the system's efficiency and charge the batteries. It aids in decreasing the need for large battery packs in electronic gadgets and the amount of time between charges. The RFEH system consists of an antenna, an input impedance matching network, a rectifier, a voltage multiplier, and an energy storage component or load.

The antenna in the RFEH system detects or receives the transmitted RF wave propagating through the transmission medium. Its impedance-matching network is designed to provide maximum power transfer for the RFEH system. The impedance matching network employs low-loss or high Q-factor inductors or transformers. The rectifier converts the received alternating current (AC) RF signal to direct current (DC) power. However, the rectifier's DC output voltage is too low to power a wireless device. As a result, a voltage multiplier is used to increase the DC voltage level to the level required by wireless devices. Finally, the harvested energy is stored in energy storage devices such as rechargeable batteries and super-capacitors or directly applied to the load. Figure 1 depicts the block diagram of an RFEH system [12].

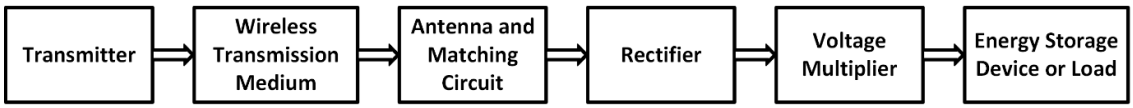

Figure 1. Block diagram of an RFEH system.

A reconfigurable RFEH with dual-path rectifiers and an adaptive control circuit (ACC) is presented in [13]. The dual-path rectifiers are configured with series and parallel paths for low-power and high-power operations. This method maintains a high-power PCE over a wide range of input power. The rectifiers use internal threshold voltage cancellation (IVC) to compensate the transistors' V_{th} effectively. The ACC includes a comparator, an inverter, and three switches that activate series or parallel paths based on the RF input power range. An off-chip impedance matching network is used to match the rectifier's input impedance to the source of the RF input power. For a 200 kΩ load at 0.902 GHz, the reconfigurable

RFEH achieved a peak power conversion efficiency (PCE) of 33% and a DC output voltage of 3.23 V with −8 dBm RF input power. It has a sensitivity of −20.2 dBm input power and outputs 1 V DC voltage for a 1 MΩ load.

Furthermore, a 3-stage Cross-Coupled Differential-Drive (CCDD) rectifier with a broad PCE dynamic range was proposed in [14]. The proposed RFEH uses a self-body biasing approach to lower the V_{th} and diode-tied transistors to lower the reverse leakage current. Both shared-capacitor-coupling (SCC) and individual-capacitor-coupling (ICC) input-capacitor topologies are designed independently for the CCDD rectifier. Two separate capacitors are used to separate the DC power supply from the RF signal route. When used in conjunction with one another, these capacitors bias the gate of the transistors while one store charge. The SCC configuration is achieved when the NMOS and PMOS transistor gates are linked to the same coupling capacitor at the input. In contrast, the gate biasing of each NMOS and PMOS transistor is kept independent by physically separating the coupling capacitor in the ICC arrangement. Input power of −18.4 dBm at 0.9 GHz resulted in a peak PCE of 83.7% for the SCC configuration. At the same frequency, the ICC configuration's peak PCE was 80.3% when fed with an input power of −17 dBm.

Moreover, an RFEH based on an improved Dickson charge pump with an output capacitor to reduce the load capacitance during the positive half cycle is proposed in [15]. The rectifiers addressed here are modified output capacitor Dickson and differential load Dickson. The Dickson charge pump scheme is used in both rectifiers, which consists of diode-connected transistors, charge storage coupling capacitors, load capacitors for output ripple reduction, and resistive load. The first design incorporates a 3-stage voltage multiplier with a modified output capacitor loop. In the meantime, the second design employs a 2-stage voltage multiplier with a differential load. The output capacitor helps increase the DC output voltage, allowing for appropriate load resistors. The differential load, on the other hand, helps to improve the rectifier's sensitivity to operate for low RF input signals at 0.953 GHz. Under −12.5 dBm input RF power, the rectifier with a modified output capacitor achieved a peak PCE of 84.4% and 1 V DC output voltage. Meanwhile, under −15 dBm input power, the rectifier with differential capacitor load achieved a peak PCE of 56.2%.

As observed from recent on-chip RFEH works, it is evident that most of them are operating in narrowband applications, and a wideband energy harvesting solution is still a challenge, unlike in other RF circuits, such as power amplifiers or voltage-controlled oscillators, which achieve wideband [16,17]. Thus, in this study, a 3-stage CCDD rectifier is equipped with an on-chip tunable voltage boosting mechanism that is entirely adjustable for wideband sensitivity tuning. The tunable voltage booster is constructed with an interleaved transformer architecture, with the primary winding connected to the rectifier while the secondary winding is connected to a MOSFET switch that tunes the network's inductance. Adjusting the voltage booster enables the CMOS RFEH's sensitivity to be maintained at 1V DC output voltage throughout a bandwidth of 3 to 6 GHz of 5GNR frequency bands. The suggested technique allows the CMOS RFEH to operate with optimal sensitivity, DC output voltage, and PCE for wideband applications.

2. Rectifier Design and Operation

The rectifier designed adopts the cross-coupled differential-drive (CCDD) architecture, as depicted in Figure 2. Referring to Figure 2, the CCDD rectifier comprises two NMOS transistors (M_{N1} and M_{N2}) and two PMOS transistors (M_{P1} and M_{P2}) connected in a cross-coupled configuration. The transistors in the rectifier are operating in the subthreshold region, and the drain-current I_D is given as [18]:

$$I_D = I_S \cdot e^{\frac{V_{GS}-V_{TH}}{nV_T}} \left(1 - e^{-\frac{V_{DS}}{V_T}}\right) \quad (1)$$

where I_S is the zero-bias current of the device, V_{GS} is the gate-source voltage of the transistor, V_{DS} is the drain-source voltage of the transistor, V_{TH} is the threshold voltage of the transistor, n is the subthreshold slope, and V_T is the thermal voltage.

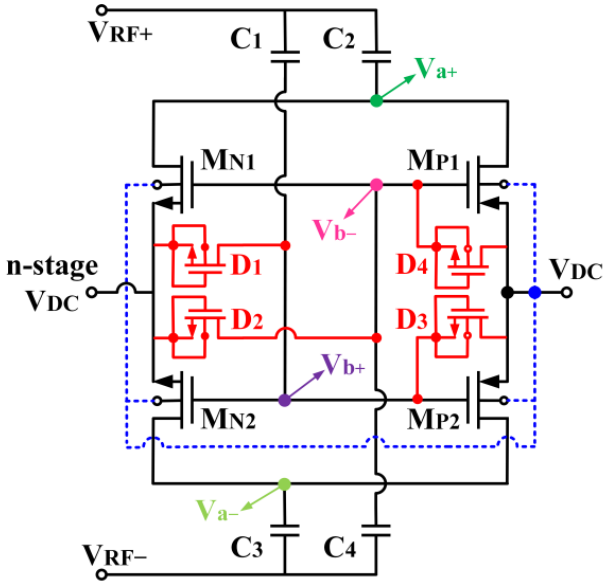

Figure 2. Schematic of the designed CCDD rectifier.

M_{N1} and M_{N2} adopt a self-body-biasing mechanism in which their bulk terminals are connected to the DC output voltage (V_{DC}). The self-body-biasing mechanism reduces the threshold gate voltage (V_{TH}) of M_{N1} and M_{N2}. Figure 3 compares drain current (I_D) with and without bulk biasing. It can be observed that the V_{TH} of the transistor can be mitigated to 440 mV from 540 mV after applying the bias to the bulk. The transistor's V_{TH} contributes to voltage drop, limiting the maximum V_{DC} and the PCE that can be achieved. Therefore, it is essential to lower the transistor's V_{TH} for the rectifier. Furthermore, to mitigate the reverse-leakage current, diode-connected MOS transistors (D_1–D_4) are integrated between the gate and the source of each transistor, as depicted in Figure 2. The diodes also aid in raising the forward conduction of the rectifier.

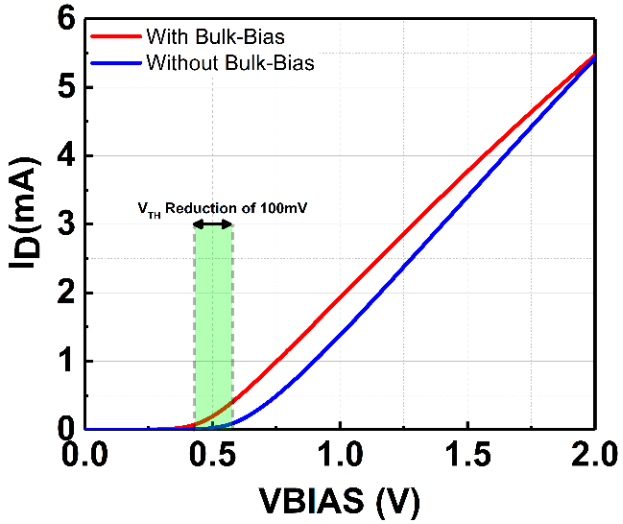

Figure 3. Drain current (I_D) comparison without and with bulk-biasing. 100 mV V_{TH} reduction is achieved with a bulk-biasing mechanism.

Assuming a steady-state operation, when the RF input power of the rectifier is low and for the first half-period of the input RF signal ($V_{RF+} > V_{RF-}$), M_{P1} and M_{N2} are turned

on to perform rectification while M_{P2} and M_{N1} are turned off. For the second half-period of the input RF signal, M_{P2} and M_{N1} perform the rectification function while M_{P1} and M_{N2} are turned off. During the first and second half-periods, the bulk of M_{N2} and M_{N1} are, respectively, biased by the V_{DC} from the rectifier in which it realizes the self-body-biasing mechanism. The self-body-biasing is not implemented on M_{P1} and M_{P2} since only the positive DC voltage is produced in the rectifier circuitry. At the low RF input signal, the reverse leakage current is minimal as the resistive loss mainly contributes to the energy loss during forward conduction. This is due to the low DC biasing voltage applied at the transistor's bulk, which is not significant for V_{TH} reduction. A voltage of more than 500 mV is necessary to overcome the forward voltage of the diode-configured transistors utilized in the rectifier circuit. This is shown in Figure 3, where the I-V curve of the diode configured MOS with W/L of 12.0 µm/0.13 µm begins to conduct current beyond 540 mV. Thus, D_1–D_4 is turned off when the RF input signal is low.

On the other hand, when the RF input signal is large enough to overcome the forward voltage of D_1–D_4, it starts to operate. At M_{N1} and M_{N2}, D_1 and D_2 are in reverse biased condition when n-stage $V_{DC} > V_{RF\pm}$. n-stage V_{DC} is the DC output voltage from the previous stage of the rectifier. The potential difference between the source and gate creates an extra current path for the forward current to flow to the system's drain, increasing the PCE. Suppose the voltage $V_{DC} > V_{RF\pm}$, the D_1, and D_2 are in forward biased condition. The diodes act as a large resistor that blocks the reverse-leakage current flowing from n-stage V_{DC} into $V_{RF\pm}$. Moreover, when $V_{DC} < V_{RF\pm}$, D_3, and D_4, which are connected at the M_{P2} and M_{P1}, respectively, are in reverse bias. D_3 and D_4 emulate a huge resistor with a potential of $-V_D$ between the gate and source of the transistors to block the reverse leakage current from flowing back to the source. Suppose the voltage $V_{DC} > V_{RF\pm}$, D_3, and D_4 are in forward bias, where it increases the forward current by pushing further charge to the output, increasing the total output charge and thus enhancing V_{DC}, sensitivity, and PCE of the rectifier.

As depicted in Figure 2, the proposed CCDD rectifier is implemented with a mutual capacitor coupling configuration as the gates of the NMOS and PMOS are connected to the same coupling capacitor at the input. The capacitors pair (C_2 and C_3) decouple from the gates of the transistors to isolate the RF signal path from the power line with the addition of C_1 and C_4. C_2 and C_3 serve as charge-storing capacitors only, while C_1 and C_4 focus solely on biasing the gate of the transistors without being impacted by the DC offset contributed by C_2 and C_3. Figure 4 depicts the input RF voltage waveforms for the proposed CCDD rectifier.

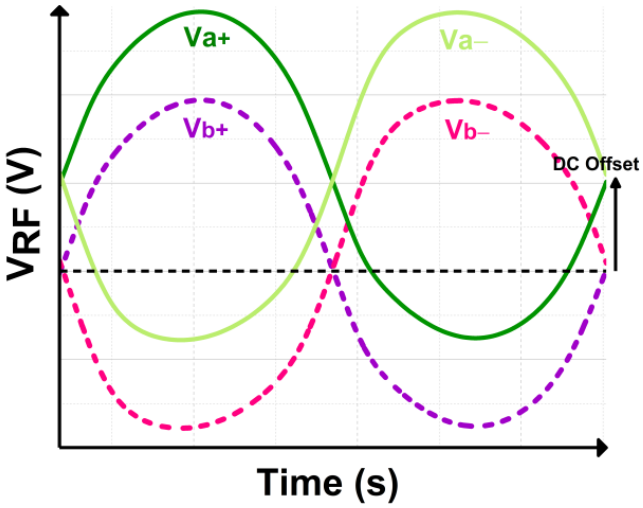

Figure 4. Terminal RF voltage waveform of the designed CCDD rectifier.

When implemented in ambient RFEH systems, cascading more stages typically allows for a higher V_{DC} output. Albeit, as a result of its proportionality to RF input power (P_{RFIN}) and PCE for a fixed output load (R_L), the power equation in (2) imposes a theoretical limit on the possible value of V_{DC}. The PCE of the rectifier is defined as in (3). As demonstrated in Figure 5, extending the rectifier stages beyond necessary would be superfluous because V_{DC} would not increase considerably. By referring to Figure 5, it can be deduced that the V_{DC} is not rising significantly beyond 3 stages and begins to drop as the stages increase. Therefore, a 3-stage rectifier is considered essential, and its configuration is depicted in Figure 6. Meanwhile, Figure 7 shows the rectification response of the 3-stage CCDD rectifier at 3 GHz.

$$V_{DC} = \sqrt{\eta \cdot P_{RFIN} \cdot R_L} \tag{2}$$

$$\eta = \frac{P_{DC}}{P_{RFIN}} = \frac{V_{DC}^2}{R_L \cdot P_{RFIN}} \times 100\% \tag{3}$$

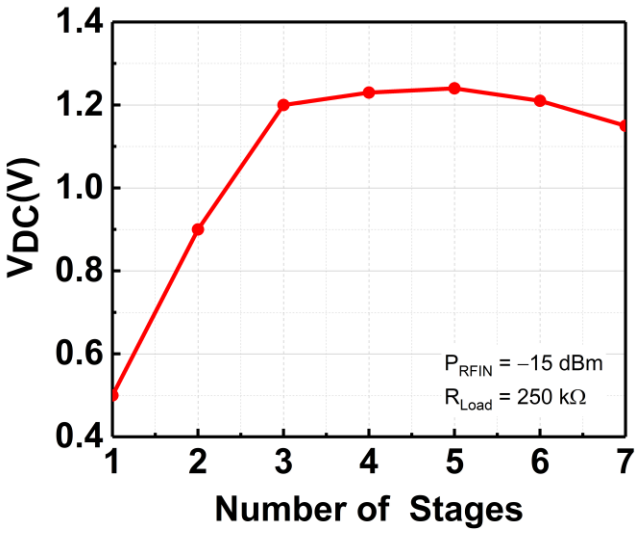

Figure 5. V_{DC} versus rectifier stages.

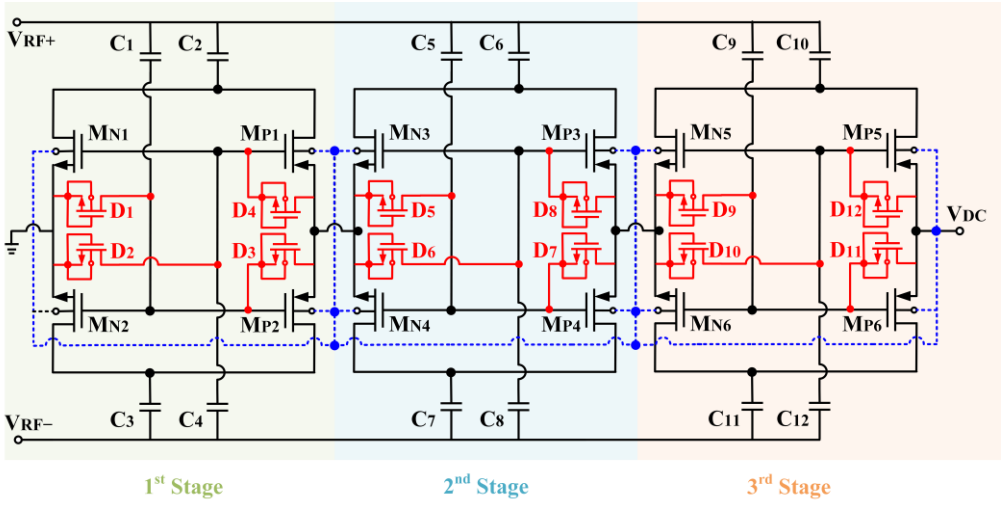

Figure 6. Schematic of the 3-stage CCDD rectifier.

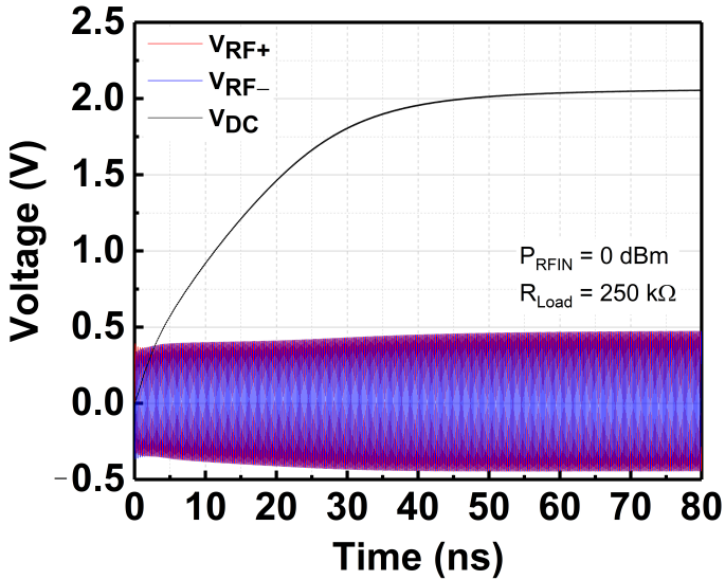

Figure 7. Rectification response of the 3-stage CCDD rectifier at 3 GHz.

3. Tunable Voltage Booster (TVB) Design and Operation

The tunable voltage booster (TVB) consists of a primary conductor and a secondary conductor interleaved between each other, as illustrated in Figure 8. The primary conductor is the main inductor connected to the input of the rectifier. In contrast, the secondary conductor is the auxiliary conductor used to tune the inductance of the primary conductor through magnetic coupling. A transistor switch is connected in parallel to the secondary conductor, which opens and shorts the conductor when the gate voltage is applied. A coupling coefficient, k, magnetically couples the primary conductor and secondary conductor. When the ambient RF input signal is applied to the primary conductor, the changing magnetic field in the primary conductor induces an opposite current flow which translates to an opposing magnetic field on the secondary conductor.

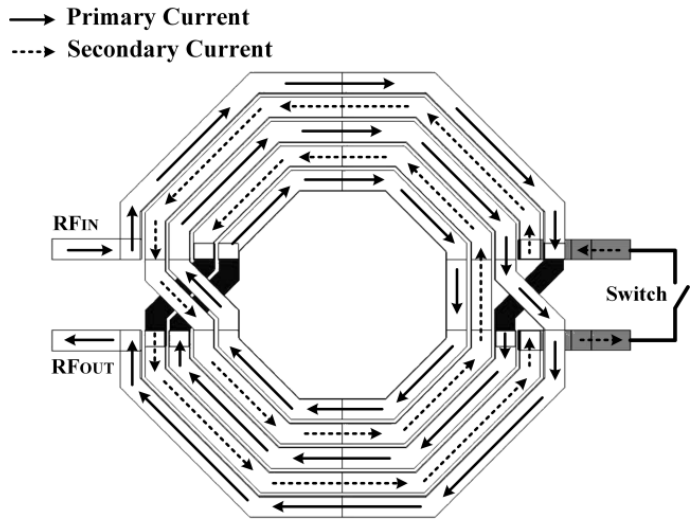

Figure 8. Tunable voltage booster (TVB) architecture.

The current flow in the secondary conductor is gradually shorted by varying the gate voltage of the transistor switch. When the transistor switch is entirely off, the secondary coil is open. Thus, no current flow occurs, and the inductance value in the primary conductor remains the default. When the transistor switch is gradually turned on via the applied gate voltage, the secondary conductor becomes shorted in, where the current flow opposes a

change of the flux. The opposing magnetic field in the secondary conductor cancels out the magnetic field created in the primary conductor. As a result, the decreasing magnetic field reduces the inductance of the primary conductor, which realizes the variability of the inductance value.

Figure 9 shows the schematic of the TVB configuration applied in the CCDD rectifier. The ambient RF input signal is applied at the primary conductor, L_p. The secondary conductor, L_s, is connected to the drain and source of an NMOS transistor, acting as a switch. A DC voltage (V_T) is applied at the gate of the NMOS transistor, where a resistor, R_1, is connected in series to provide isolation between the AC signal path and the DC signal path. The secondary conductor is open when the transistor is turned off (V_T = 0 V). When the gate voltage is gradually increased (V_T > 0 V), the secondary conductor is shorted, which induces an opposite current flow that opposes the magnetic field in the primary conductor, as aforementioned. The current flow paths on each conductor are illustrated in Figure 8. The opposite current flow in the secondary reduces the inductance value in the primary conductor due to their magnetic coupling. The following brief analysis, with the aid of Figure 10, shows the relation of primary inductance when the secondary coil is shorted. Referring to Figure 10:

$$V_1 = j\omega L_P I_1 + j\omega M I_2 \tag{4}$$

$$V_2 = j\omega M I_1 + j\omega L_s I_2 \tag{5}$$

when L_s is shorted,

$$V_2 = 0 \tag{6}$$

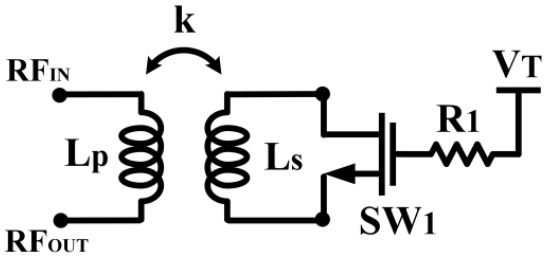

Figure 9. Schematic of the TVB.

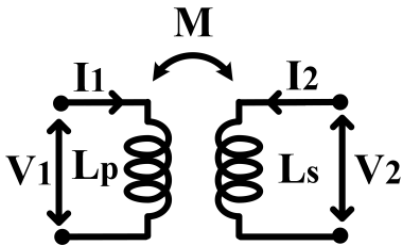

Figure 10. Simple analysis schematic for the TVB operation.

Thus,

$$I_2 = -\frac{M}{L_s} I_1 \tag{7}$$

Substituting (7) into (4),

$$V_1 = j\omega L_P I_1 + j\omega M\left(-\frac{M}{L_s} I_1\right) \tag{8}$$

$$V_1 = j\omega L_P I_1 + j\omega M\left(-\frac{M}{L_s} I_1\right) \tag{9}$$

Since $M = k\sqrt{L_p L_s}$:

$$M^2 = k^2 L_p L_s \tag{10}$$

Substituting (10) into (9),

$$V_1 = j\omega L_P\left(1 - k^2\right) I_1 \tag{11}$$

Thus, the inductance of L_P when the switch is turned on is:

$$L_{P,SW=ON} = L_P\left(1 - k^2\right) \tag{12}$$

It can be deduced from (12) that the inductance of L_P is reduced when the switch is turned on at the secondary coil.

The TVB is designed and characterized according to the impedance values needed for the rectifier to achieve wideband sensitivity from 3 to 6 GHz. Figure 11a delineates the simulated inductance value variations of the TVB when VT is tuned from 0 to 2.25 V. Referring to Figure 11a, it can be observed that the inductance (L) can be varied from 5 nH to 1.6 nH at 3 GHz. It is also observed that the inductor's self-resonance frequency (SRF) is increased to a higher frequency when V_T is tuned. On the other hand, Figure 11b shows the respective simulated Q-factor of the inductor. This tuning property of the voltage booster is integrated with the rectifier to achieve the wideband functionality of the CCDD rectifier.

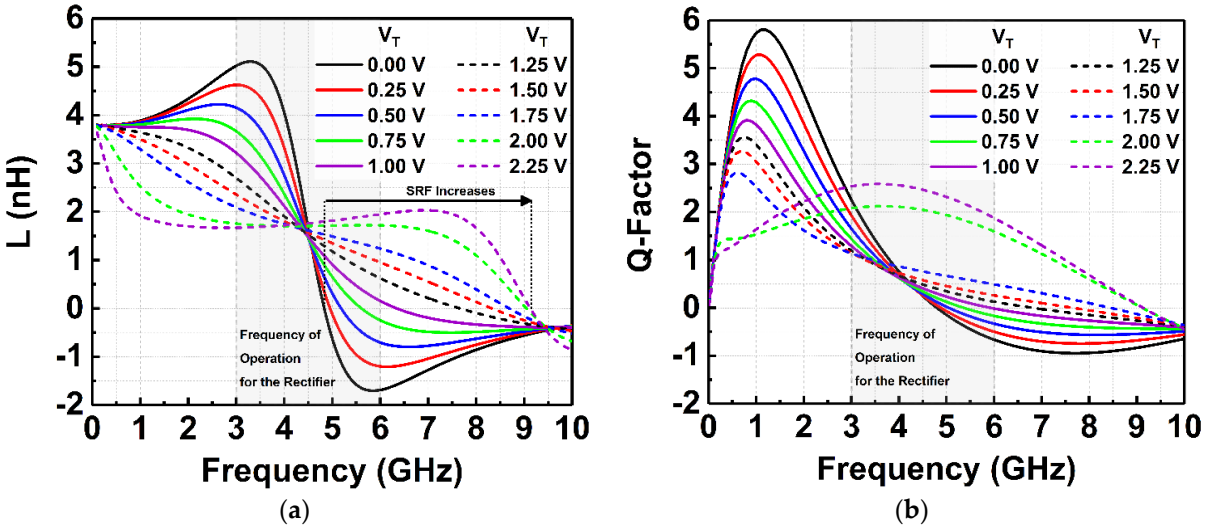

Figure 11. (**a**) Simulated inductance values of the TVB when V_T is tuned. (**b**) Simulated Q-factor values of the TVB when V_T is tuned.

4. CCDD-TVB Rectifier Design and Operation

The fully integrated architecture of the CCDD-TVB rectifier is illustrated in Figure 12. The rectifier is constructed in 3 stages to achieve the optimum DC output voltage and PCE. The TVB is employed at both differential inputs of the rectifier to provide the tuning property at the rectifier's input symmetrically. M_{N1} to M_{N6} and M_{P1} to M_{P6} are the NMOS and PMOS transistors utilized in the 3-stage CCDD rectifier. D_1 to D_{12} are the diode-connected transistors employed to suppress the reverse-leakage current throughout the stages. C_2, C_3, C_6, C_7, C_{10}, and C_{11} are the charge storing capacitors, while C_1, C_4, C_5, C_8, C_9, and C_{12} are the gate biasing capacitors. The tunable voltage boosters are L_1 (L_{1P} and L_{1S}), and L_2 (L_{2P} and L_{2S}) applied at the positive (V_{RF+}) and negative (V_{RF-}) inputs of the rectifier, respectively. L_{1P} and L_{1S} are the primary and secondary coil of L_1, respectively, while L_{2P} and L_{2S} are the primary and secondary coil of L_2, respectively. SW_1 and SW_2 are the NMOS switches employed at L_{1S} and L_{2S}, respectively, to tune the inductance of L_{1P} and L_{2P}. R_1 and R_2 are the isolation resistors for both TVBs. The gate voltages for SW_1

and SW_2 are applied via V_{T1} and $V_{T2,}$ respectively, to conduct the tuning mechanism of the TVBs. C_L is the capacitor load of the rectifier, and it is tested with a resistor load (R_L) of 250 kΩ.

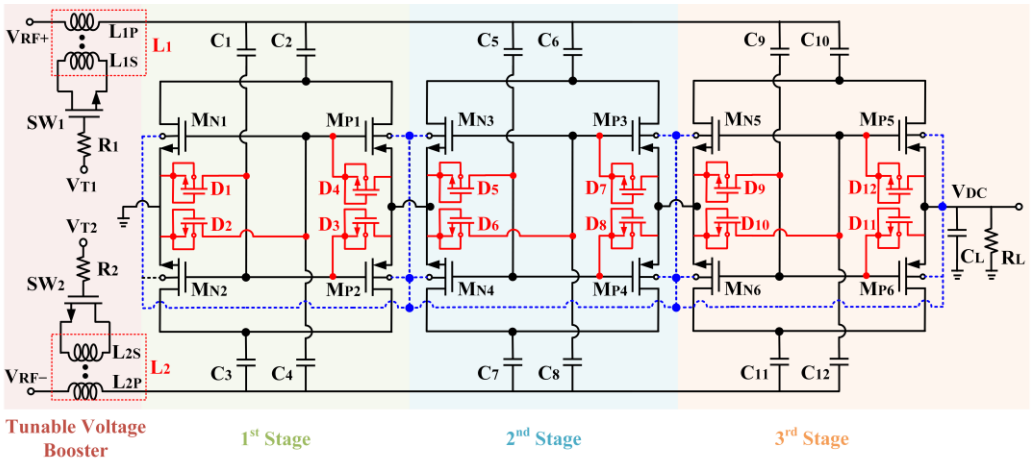

Figure 12. Detailed schematic of the CCDD-TVB rectifier.

Conventionally, a series inductor at the rectifier's input is utilized as the voltage booster (VB). The conventional implementation of the VB has significantly enhanced the V_{DC} of the rectifier. Figure 13 shows the simulated V_{DC} achieved by the rectifier with conventional VB and without VB across the targeted frequency of 3 to 6 GHz. At 3 GHz, the sensitivity of the CCDD rectifier at 1 V V_{DC} is significantly enhanced by −7 dBm (from −17 to −24 dBm). However, when the frequency changes, the sensitivity drastically degrades, reflecting the drawback of the conventional VB. This is due to the change in input impedance after implementing the conventional VB. Observe in Figure 13 that the sensitivity of the rectifier did not vary much without the VB. This is because the input impedance did not change significantly as compared to after VB implementation. It is clearly illustrated in the Smith chart provided in Figure 14. Referring to Figure 14, it can be deduced that the input impedance's location on the Smith chart changes drastically with the conventional VB compared to without the VB. Since the conventional VB does not have a tuning characteristic, it is a limitation for wideband implementation in rectifiers.

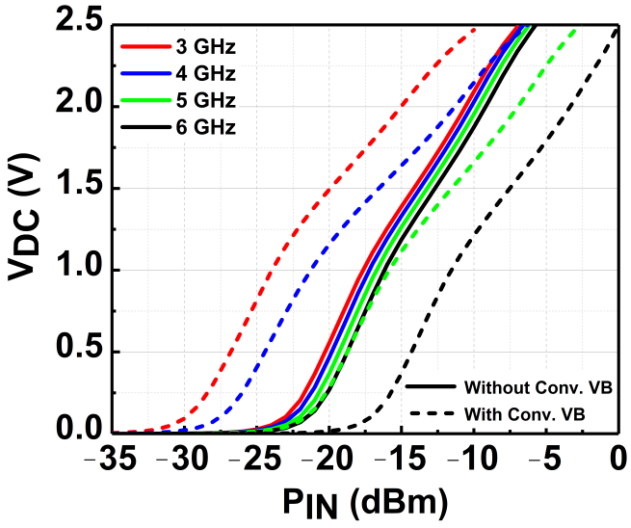

Figure 13. Simulated V_{DC} of the CCDD rectifier with and without the conventional VB.

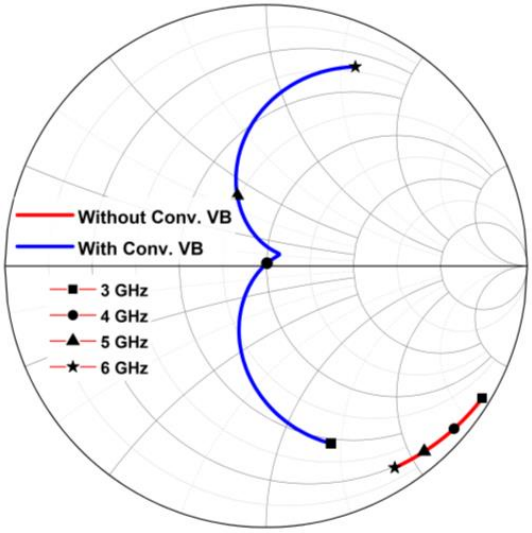

Figure 14. Input impedance's location across frequency with and without conventional VB.

Furthermore, the optimum impedance points for specific parameters can be determined via the load or source pull analysis [19]. Thus, the input impedance for sensitivity across the wideband frequency for the rectifier is identified using the source-pull evaluation. The input impedance for sensitivity at 1 V of less than −20 dBm across frequency is targeted to be achieved. The TVB is designed to fulfill the input impedance needed across the frequency for the targeted sensitivity at 1 V, thus resolving the limitation of the conventional VB, which is narrowband. Figure 15 shows the Smith chart illustrating the input impedance location after tuning the voltage booster. It can be observed that the input impedance's locations for wideband sensitivity can be attained by tuning the TVB. The TVB provides different values of inductances when tuned as compared to conventional VB, in which it can shift the input impedance locations for sensitivity optimization across wideband frequencies.

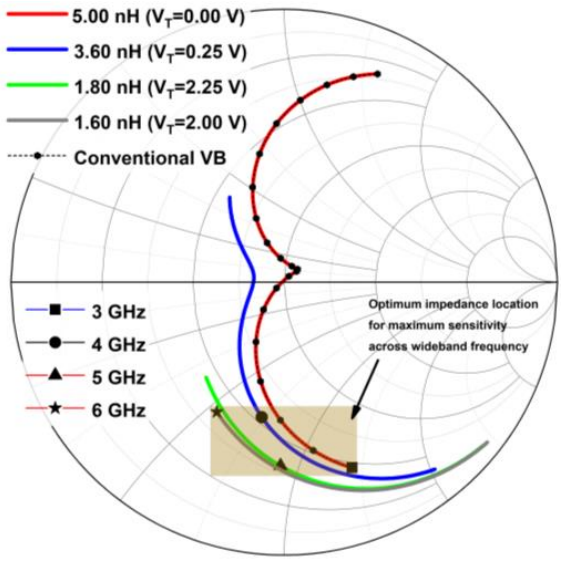

Figure 15. Input impedance's location across frequency after tuning the TVB as compared to conventional VB.

After tuning the TVB, the sensitivity of the rectifier at 1 V can be enhanced across the frequency. Figure 16 depicts the V_{DC} achieved by the rectifier before and after tuning. It can be observed that the sensitivity varies drastically by −13 dBm across frequency

before tuning. The sensitivity is enhanced to only −2 dBm variation across frequency after tuning the TVB. It proves the functionality of the tunable voltage in realizing the wideband sensitivity rectifier. At 3 GHz, the best V_T setting is by default 0 V. At 4 GHz; the V_T needed for the optimum performance is 0.25 V. Meanwhile, at 5 and 6 GHz, the V_T settings required are 2.25 V and 2 V, respectively.

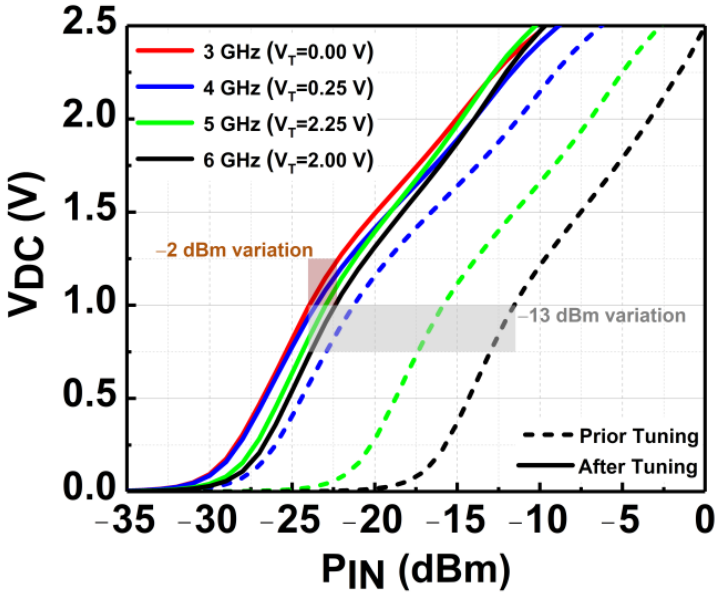

Figure 16. Simulated V_{DC} of the CCDD-TVB rectifier across frequency before and after tuning.

5. Measurement Results

The proposed CCDD-TVB rectifier is fabricated using the technology of CMOS 130 nm and six metal layers. It consumes an area of 1.43 mm^2 on-chip, including the bond pads for measurement. Figure 17 depicts the fabricated chip of the CCDD-TVB rectifier. In addition, Figure 18 illustrates the measurement setup utilized for validating and characterizing the CCDD-TVB rectifier. The parametric analyzer supplies and monitors the DC voltages (V_{T1} and V_{T2}) to the chip. The RF and DC probes are used to probe the connection pads on-chip. Additionally, the multimeter is used to measure the DC output voltage (V_{DC}) of the CCDD-TVB rectifier from the PCB variable load. A 250 kΩ load is used as the optimum load for the system. The signal generator is utilized to supply the RF input power (P_{IN}) to the rectifier and the RF balun to split the signal into a differential signal.

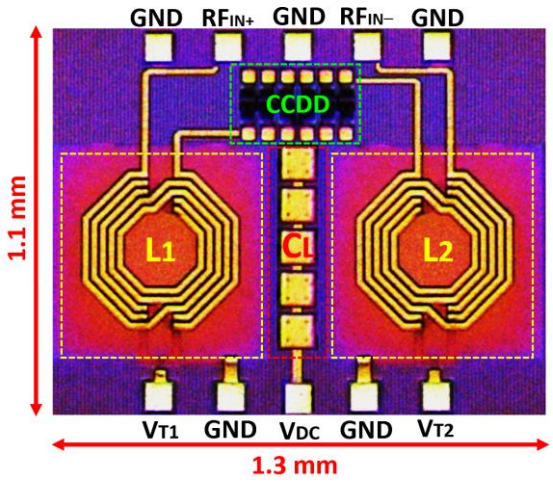

Figure 17. The micro-photograph of the fabricated CMOS 130 nm CCDD-TVB rectifier.

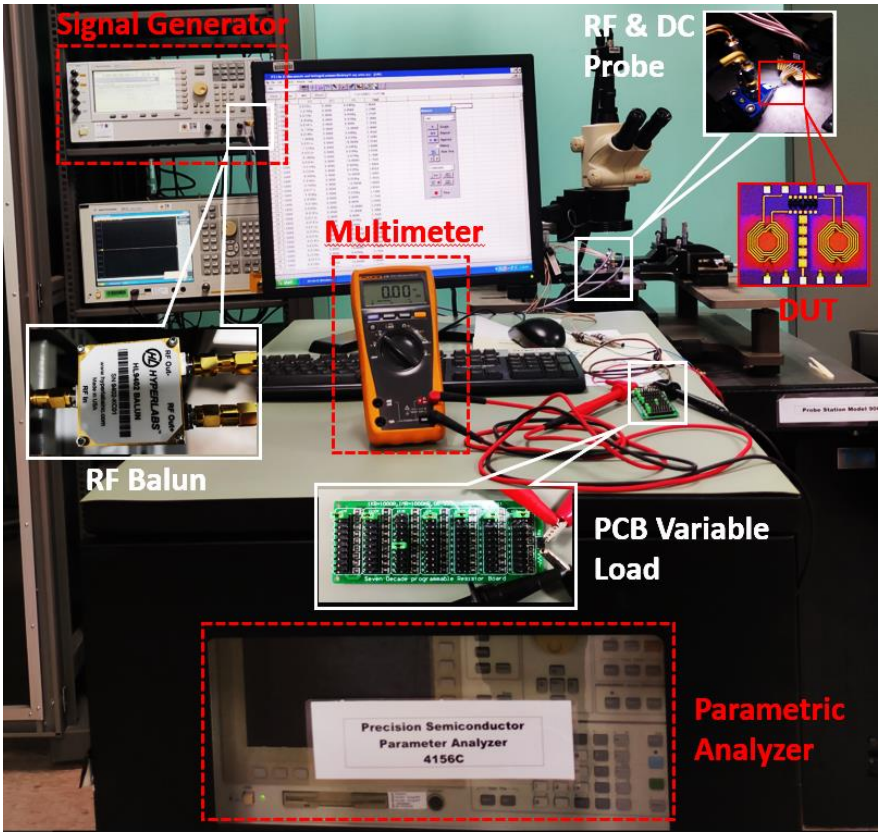

Figure 18. Measurement setup for the validation of CCDD-TVB rectifier.

Figure 19 depicts the measured V_{DC} of the CCDD-TVB rectifier for different load conditions across the P_{IN} at 3 GHz. It can be observed that as the load is increased from 50 kΩ to 250 kΩ, the sensitivity of the rectifier rises as well. The open-load condition is close to the 250 kΩ load, which is required to achieve the highest sensitivity for the rectifier. Thus, 250 kΩ is selected as the optimum load condition required, and the measurement across frequency is conducted. The CCDD-TVB rectifier can deliver a maximum V_{DC} of 2.5 V for P_{IN} of −7 to −8 dBm across the frequency when measured with R_L = 250 kΩ. The measured results do not deviate much from simulated results which reflect the reliability of the design, as illustrated in Figure 20. The measured sensitivity at 1 V obtained is from −21.5 dBm at 6 GHz to −23.5 dBm at 3 GHz, where the variation is −2 dBm across the frequency. Figure 21 delineates the sensitivity of the CCDD-TVB rectifier across the frequency of 3 to 6 GHz. The slight deviation of performance between the simulation and measured results is due to the parasitic effect on-chip and process variations during the fabrication of the rectifier.

Figure 22 shows the respective measured PCE achieved by the CCDD-TVB rectifier across the frequency. A peak PCE of 83% is achieved at 3 GHz for −23 dBm P_{IN}. At 4 GHz, the peak PCE achieved is 73% for −22.5 dBm P_{IN}. At 5 GHz and 6 GHz, the peak PCE is 67% and 57% for −22 dBm and −21.5 dBm, respectively. Referring to Figure 21, the peak PCE is achieved at the lowest sensitivity points across the frequency. It can be observed that the PCE can be maintained at more than 50% across the frequency at its sensitivity point of 1V DC output voltage by tuning the proposed TVB mechanism. Table 1 summarizes the performances of the CCDD-TVB rectifier and compares it to the recent state-of-art rectifiers. It can be observed from the summary that the proposed CCDD-TVB achieves an operating bandwidth of 3 GHz (3 to 6 GHz) as compared to other recent works. This work also realizes the RFEH application for 5GNR bands.

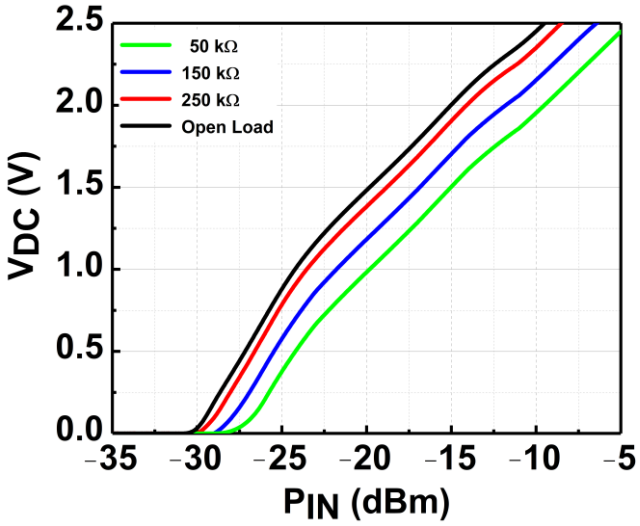

Figure 19. Measured V_{DC} of the CCDD-TVB rectifier at 3 GHz for different load conditions.

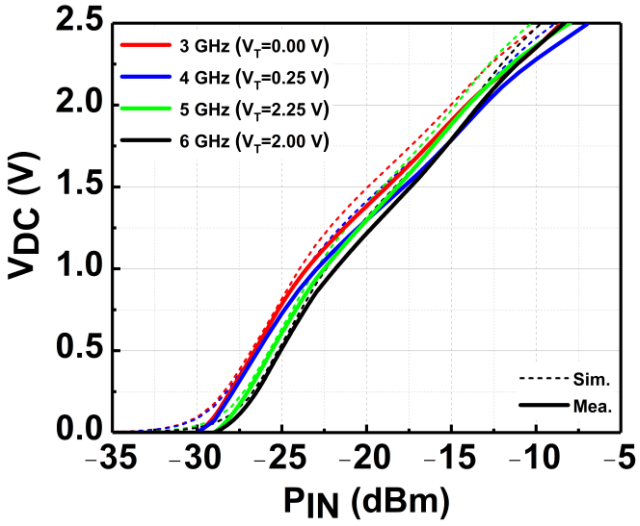

Figure 20. Measured tuned V_{DC} of the CCDD-TVB rectifier across frequency.

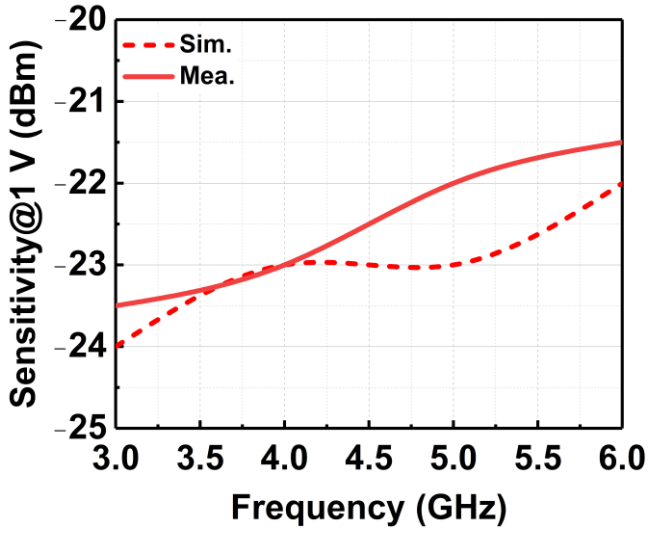

Figure 21. Sensitivity of the CCDD-TVB rectifier across wideband frequency.

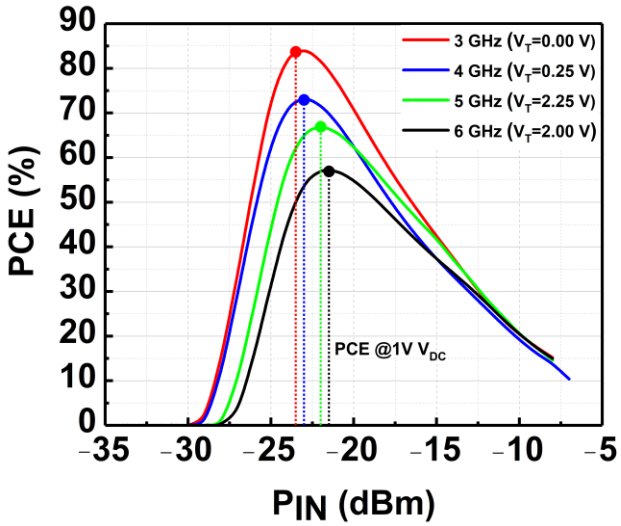

Figure 22. PCE of the CCDD-TVB rectifier across wideband frequency.

Table 1. Comparison of CCDD-TVB rectifier with recent works.

Ref.	Tech.	Rectifier Topology	Freq. (GHz)	Peak PCE (% for Load at Input Level)	VDC_{out} (V)	Sensitivity@VDC (dBm@V)
[13]	180 nm CMOS	1-stage voltage doubler	0.902	33% for 200 kΩ@ −8 dBm	3.23	−20.2@1
[14]	130 nm CMOS	3-stage CCDD	0.9	83.7% for 100 kΩ@ −18.4 dBm	1.1	−19.2@1
[15]	65 nm CMOS	3-stage Dickson	0.953	84.4% for 21.5 kΩ@ −12.5 dBm	1	−12.5@1
[20]	130 nm CMOS	12-stage Dickson	0.915	32% for 1 MΩ@ −15 dBm	3.2	−20.5@1
[21]	180 nm CMOS	Dickson	0.433	30% for 10 kΩ@ −5 dBm	0.5	−9@0.1
[22]	180 nm CMOS	1-stage CCDD	0.1	65% for 100 kΩ@ −18 dBm	1	−18@1
[23]	180 nm CMOS	1-stage CCDD	0.433	65.3% for 50 kΩ@ −15.2 dBm	1	−17@1
[24]	180 nm CMOS	2-stage differential	0.433	74% for 5 kΩ@ −2 dBm	0.8	0@0.8
[25]	180 nm CMOS	5-stage Dickson	0.93/2.63	25.2%/22.5% for 500 kΩ@ −1 dBm	9.5	−16/−15.4@1
[26]	130 nm CMOS	3-stage CCDD Bridge	0.953	72.2% for 10 kΩ@ −1.3 dBm	4.2	−6.3@1
This Work	130 nm CMOS	CCDD + TVB	3–6	83% at 3 GHz for 250 kΩ@ −23 dBm	2.5	−23.5 to −21.5 @1

6. Conclusions

A wideband sensitivity rectifier is designed and validated in this work. The proposed TVB can tune the input impedance of the designed CCDD rectifier, which realizes the wideband property. The CCDD-TVB rectifier can maintain its sensitivity of 1 V V_{DC} with a minimum deviation of −2 dBm input power across a frequency bandwidth of 3 GHz to 6 GHz. The PCE at the sensitivity point is also maintained by more than 40% across the

frequency. A peak PCE of 83% is achieved at 3 GHz for P_{IN} of −20 dBm. All the measured results are validated with a 250 kΩ resistor output load for the rectifier. The maximum DC output voltage of 2.5 V is achieved across the bandwidth. The CCDD-TVB architecture realizes the wideband operating rectifier, which is suitable for 5GNR bands that operate from 3 GHz to 6 GHz.

Author Contributions: Conceptualization, Y.L. and J.R.; methodology, Y.L., J.R. and S.M.; software, Y.L. and S.S.H.; formal analysis, Y.L., J.R., S.M., A.S.R. and S.S.H.; validation, Y.L., J.R., S.M., N.K. and M.O.; resources, J.R. and S.M.; data curation, Y.L., J.R., S.M. and A.S.R.; writing—original draft preparation, Y.L., J.R., S.M. and A.S.R.; writing—review and editing, J.R., S.M., N.K., M.O. and A.N.; visualization, Y.L., S.M. and S.S.H.; supervision, J.R., M.O. and A.N.; project administration, J.R.; funding acquisition, J.R. and S.M. All authors have read and agreed to the published version of the manuscript.

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