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CMOS reliability issues for emerging cryogenic Lunar electronics applications

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Abstract

We investigate the reliability issues associated with the application of CMOS devices contained within an advanced SiGe HBT BiCMOS technology to emerging cryogenic space electronics (e.g., down to 43 K, for Lunar missions). Reduced temperature operation improves CMOS device performance (e.g., transconductance, carrier mobility, subthreshold swing, and output current drive), as expected. However, operation at cryogenic temperatures also causes serious device reliability concerns, since it aggravates hot-carrier effects, effectively decreasing the inferred device lifetime significantly, especially at short gate lengths. In the paper, hot-carrier effects are demonstrated to be a stronger function of the device gate length than the temperature, suggesting that significant trade-offs between the gate length and the operational temperature must be made in order to ensure safe and reliable operation over typical projected mission lifetimes in these hostile environments.
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Keywords: CMOS; Cryogenic temperatures; Low-temperature operation; Reliability; Space electronics

1. Introduction

Recently, emerging cryogenic electronics applications using silicon (Si) CMOS technology have generated renewed interest due to NASA's recently mandated refocus on Lunar and Martian robotics and human exploration [1]. Since the required cooling system overhead dramatically increases system cost and complexity [2], cryogenic CMOS devices have yet to make significant in-roads into conventional electronics applications, although it is well-established that cryogenic operation of Si CMOS technology can provide significant device performance improvements beyond geometrical scaling [3]. In NASA's envisioned Lunar missions, the surprisingly extreme low temperature conditions (e.g., −230 °C in the shadowed polar craters, −180 °C during the Lunar night) make the operation of the electronic sub-systems on the surface of the moon exceptionally difficult, but is required for the envisioned complex suite of electronics systems used in sensing, actuation, and control of robotic systems. Such applications typically do not need the most aggressively scaled CMOS technology, because they are fairly low frequency in nature (e.g., <100 MHz). The most important concern becomes how reliable a full suite of mixed-signal circuit building blocks can be within operating over such extremely wide temperature ranges (e.g., +120 °C to −230 °C = 350 °C swings!). Therefore, adequate Si CMOS

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device reliability must clearly be achieved first. CMOS device degradation due to hot carrier effects (HCE) is known to generally be considerably worse at low temperatures [4]. Device lifetime data at cryogenic temperatures, and a solid understanding of the corresponding degradation mechanisms, are thus critical in this context, and are addressed in this paper.

2. Device technology

The Si CMOS devices investigated here are from a commercially-available, 3.3 V, 0.5 μm SiGe HBT BiCMOS technology (the targeted integrated circuit platform for Lunar electronics), with a fixed channel width of 10.0 μm, and effective gate lengths ranging from 0.35 μm (minimum geometry), to 5.0 μm. The gate oxide thickness is 8 nm. The devices were characterized on a custom cryogenic probe system from 300 K (+27 °C) down to 43 K (−230 °C).

3. Electrical results

To gain deeper physical insight into the temperature dependence, we measured and analyzed the important CMOS device parameters: output current, carrier mobility, transconductance, and threshold voltage, at different temperatures. Figs. 1 and 2 show the typical I–V characteristics of the CMOS devices from 43 K to 300 K, with V_{DS} at 50 mV and V_{GS} at 3.3 V, respectively. As expected,

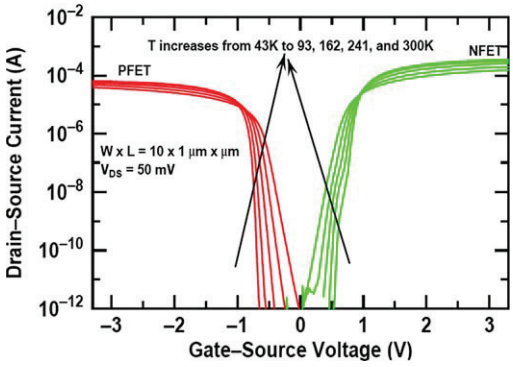

Fig. 1. I_D vs. V_G for nFET and pFET devices at different temperatures.

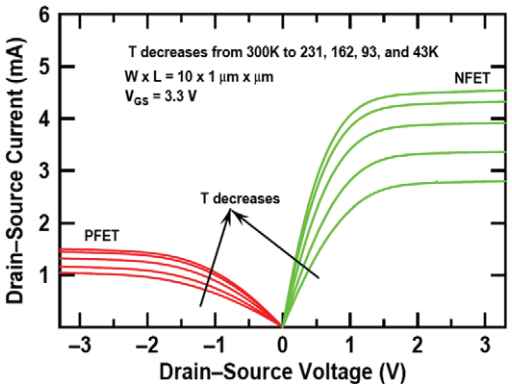

Fig. 2. I_D versus V_D for nFET and pFET devices at different temperatures.

the current drive capability increases significantly for the same bias conditions as the temperature decreases, indicating a significant performance improvement at low temperatures. It can also be seen from the slope in the subthreshold region in Fig. 1 that the CMOS devices can be switched on and off in a relatively small gate bias range, a decided design advantage for low-temperature operation since it can enable reduced power supply voltage operation [5].

Table 1 summarizes the key device parameters, such as normalized low-field mobility, normalized linear transconductance, threshold voltage, and sub-threshold swing, at different temperatures. The low-field mobility was extracted using the method described in [6]. The transconductance increases by a factor of three as the temperature decreases from 300 K to 43 K. The low field mobility increases with decreasing temperature from 300 K to 43 K, by a factor of 2.0 and 5.5 for holes and electrons, respectively, because of the reduced carrier scattering at low temperatures. The threshold voltage increases from 0.6 to 0.8 V with cooling. The substrate voltage can be approximated as the sum of the flatband voltage and the gate bias needed to create a channel surface potential of $2\Phi_F$, where Φ_F is the Fermi potential. The increased Φ_F at lower temperatures leads to an increase in the threshold voltage, as expected [7]. The subthreshold swing decreases from 90 mV/decade to about 20 mV/decade with cooling to 43 K.

Table 1
The key parameters of nFET and pFET devices at different temperatures

Temperature (K)	Normalized transconductance		Normalized mobility		Absolute threshold voltage (V)		Subthreshold swing (mV/decade)	
	nFET	pFET	nFET	pFET	nFET	pFET	nFET	pFET
43	3.25	2.72	5.40	2.06	0.83	0.82	27.2	20.7
93	2.72	2.47	3.82	1.84	0.78	0.77	28.1	32.0
162	2.00	1.90	2.16	1.50	0.72	0.72	43.8	44.4
231	1.37	1.39	1.46	1.23	0.67	0.66	64.3	64.2
300	1.00	1.00	1.00	1.00	0.60	0.60	90.2	89.4

4. Device reliability

It is well known that nFET generally have worse reliability behavior than the pFETs at the same geometry, and for brevity we will focus here only on the nFET data. The nFET reliability lifetime was inferred using electrical stress-induced changes to the I_D–V_G characteristics. The lifetime τ is defined as the inferred stress time for which a certain parameter of the I_D–V_G characteristics has shifted by a predefined amount (e.g., 10% degradation in gm). A typical lifetime assessment analysis using the I_D–V_G characteristics for a 1.0 μm nFET is shown in Figs. 3 and 4. Fig. 3 demonstrates the change of I_D–V_G with increasing stress time; while Fig. 4 shows the relative change of the extracted transconductance as a function of stress time, for two different stress bias conditions. The slope of 0.6 for the linear fitting in Fig. 4 suggests that interface state generation is responsible for the observed device degradation at the maximum substrate current ($V_D \approx 2\ V_G$); while the slope of 0.3 for the maximum gate current bias condition ($V_D = V_G$) suggests that oxide trapped charges dominate [8]. For the nFETs operating at 300 K, the worst case bias condition for hot carrier degradation is known to be under maximum substrate current bias for long channel devices. The worst case bias conditions for hot carrier degradation can be a function of temperature, however, and must be revisited here [9,10]. Fig. 4 verifies that for the present technology, maximum substrate current is indeed the worst bias condition for long-channel devices ($L \geqslant 1$ μm), at least down to 82 K.

The substrate current is comprised of the generated hot carriers, and is thus a good monitoring parameter for HCE in practical reliability measurements. For an nFET under a certain V_{DS}, channel electrons enter the high-field region of the device, acquiring enough energy to break a Si–Si bond (normally larger than the Si bandgap). Many of these energetic carriers will break bonds, generating free electron–hole pairs. The holes are swept into the body of the device, where they are measured as substrate current. Furthermore, correlation between device degradation and substrate current can be extended to include different temperatures without the use of additional parameters [11].

Figs. 5 and 6 show the effects of temperature and gate length on the substrate current, respectively. It can be seen from Fig. 5 that the maximum substrate current under the same bias condition increases by 3× as temperature decreases from 300 K to 43 K. The number of hot carriers that have energies significantly above the Si bandgap is limited by the equilibrium between carrier kinetic energy and lattice phonons [12]. With the decrease in temperature, the channel carriers see less phonon scattering and their mean free path lengths increase. Thus, the ratio of hot carriers to the number of total channel carriers increases at reduced temperatures, and the measured substrate current

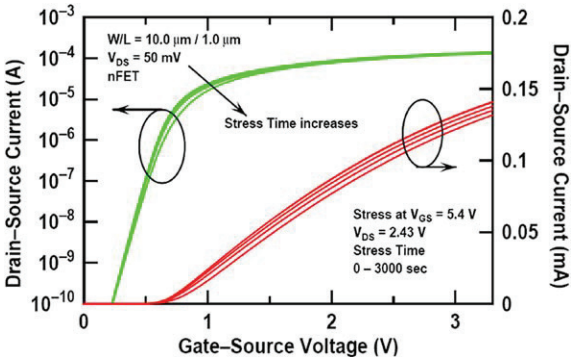

Fig. 3. I_D versus V_G for an nFET with increasing stress time.

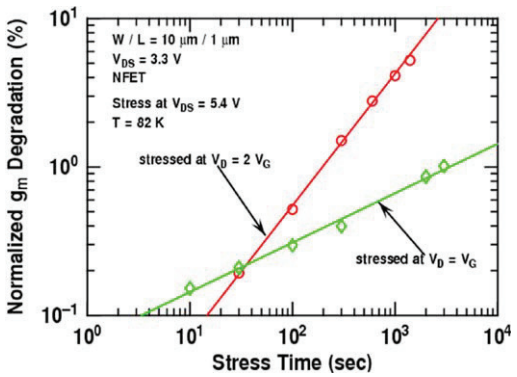

Fig. 4. Time-dependent transconductance degradations used to extract device lifetime.

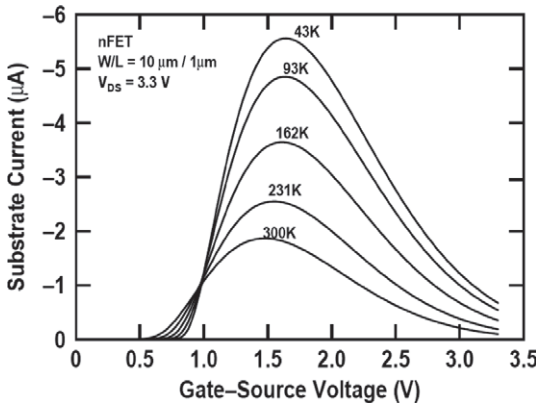

Fig. 5. The substrate current as a function of gate bias for an nFET at different temperatures.

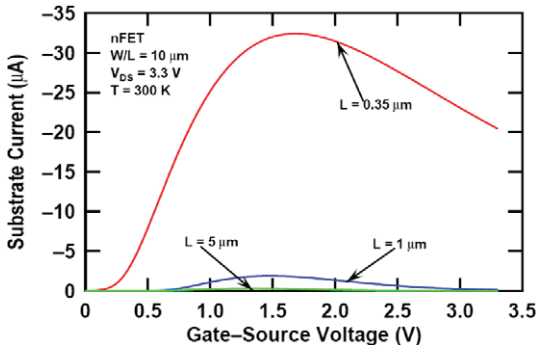

Fig. 6. The substrate current as a function of gate bias for nFETs with different gate lengths.

due to impact ionization increases significantly. Fig. 6 shows that the maximum substrate current increases by more than 10× as L decreases from 1.0 μm to 0.35 μm, and becomes negligible as L increases to 5.0 μm. The peak value of the longitudinal electric field along the channel depends on V_{DS} and gate length. When V_{DS} is kept at a fixed value, the shorter the gate length, the higher the field, hence the larger proportion of hot carriers in the overall population [13]. The increased proportion of hot carriers leads to the increase of substrate current for the short-channel device.

The similar substrate current trends are observed for long and short channel (0.35 μm) devices from 300 K down to 82 K. The magnitude of gate currents is negligible compared with that of substrate currents over the investigated temperature range. Thus, HCE are influenced more by device geometry than by the temperature for the present technology, as can be seen by comparing Figs. 5 and 6.

It has long been the standard industry practice to project hot carrier lifetime by performing a set of stresses for a particular channel length using different V_{DS} values and a single V_{GS} condition for nFETs, typically at the peak substrate current. By plotting the inferred lifetime at different drain biases, one obtains reasonable estimates of V_{DS} for a ten-year lifetime of the given CMOS device. Fig. 7 shows the inferred lifetime for the nFETs in the present technology with fixed gate length when stressed at different drain biases, for different stress temperatures. Fig. 8 shows the inferred lifetime for devices with different gate lengths, when stressed at a different drain bias at room temperature. As seen in Fig. 7, τ decreases by ~10× as the temperature is reduced from 300 K to 82 K, and V_{DS} for a ten-year lifetime decreases from 3.50 to 3.19 V. Fig. 8 suggests that τ differs by more than 100× and V_{DS} for a ten-year lifetime differs by more than 0.6 V among the 0.35 μm, the 1.0 μm, and the 5.0 μm transistors. Hence, the long-channel devices ($L \geqslant 1.0$ μm) are the preferred choice for cryogenic Lunar applications using this SiGe BiCMOS technology. Given the relatively slow speeds of the requisite Lunar mixed-signal circuits envisioned, this relaxation of gate length to improve cryogenic reliability is a favorable

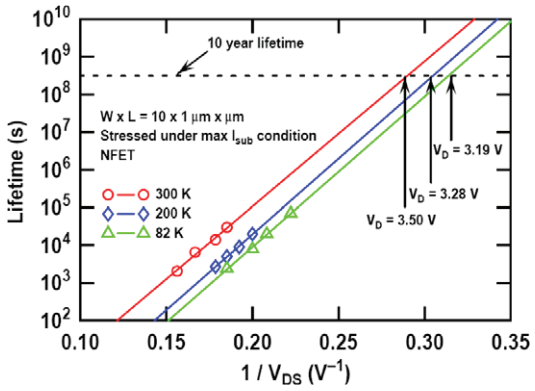

Fig. 7. The inferred lifetime as a function of bias condition for an nFET at 82, 200, and 300 K.

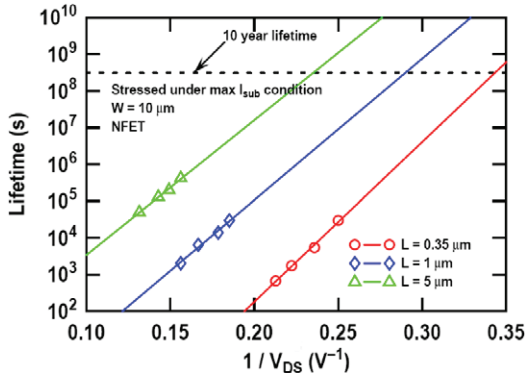

Fig. 8. The inferred lifetime as a function of bias condition for nFETs with various gate lengths.

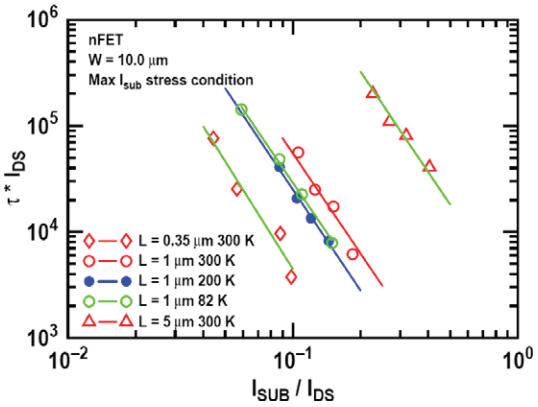

Fig. 9. The nFET extrapolated lifetime plots used to evaluate activation energy.

trade-off. All of the lifetime data used in Figs. 7 and 8 were extracted from stress measurements under maximum substrate current bias conditions. However, it is not necessarily true that this is the worst bias condition for shorter channel devices.

Figs. 7 and 8 suggest that the device lifetime is a stronger function of gate length than operating temperature, and correlates well with the HCE data in Figs. 5 and 6. Assuming fast interface trap generation dominates the HCE degradation process, plotting $(\tau \cdot I_D)$ versus (I_{SUB}/I_D) on a log–log scale should yield a straight line behavior [14]. The critical electron energy for generating an interface trap is calculated to be 3.9 eV from the slope of this line. Both the slope and the critical energy from Fig. 9 correlate well with published literature data (e.g., 2.9 and 3.7 eV in [15]), suggesting that interface state generation is the dominant limiting reliability factor in the present CMOS devices, when the devices are stressed under maximum substrate current condition.

5. Discussion

Cryogenic temperature operation provides CMOS device performance enhancement, albeit at the expense of shorter device reliability lifetime. Part of this reliability

degradation can be offset by using CMOS with longer channel transistors, since the hot carrier inducing device degradation is more strongly dependent on channel length than on operating temperature. The use of longer channel devices leads to smaller output current drive capability (hence circuit speed) because of the smaller W/L ratio. Trade-offs must thus be negotiated between speed and device reliability. The choice of the right device geometry will often depend on the practical application of the transistors in the circuit. For example, in digital applications, the output current driving capability will be critical for a source-follower transistor in a buffered FET logic circuit, so a short-channel CMOS will be preferred; while long-channel devices will be preferred for CMOS in an inverter that requires a large logic swing. In addition, analog circuit primitives such as op-amps and comparators can typically tolerate larger (more reliable at cryogenic temperatures) geometry transistors since transistor-to-transistor matching and noise often dominate circuit performance. One of the advantages of low-temperature operation is the reduced power consumption resulting from the potential scaling of the power supply voltage with temperature. The threshold voltage of an unoptimized CMOS device will increase, however, as the temperature decreases. One solution to this problem is to reduce the threshold voltage through careful channel profile design. For example, V_T can be reduced by decreasing the channel doping. Another solution is to modulate the threshold voltage by forward biasing the source-body junction. An interesting threshold voltage engineering scheme at room temperature has been reported based on the active well CMOS strategy [15]. By forward-biasing the body at about 0.6 V, CMOS gains significant performance enhancement, yielding faster device switching speed and lower power consumption. This technique requires, however, the use of a dual trench isolation process to limit the junction leakage and prevent latch up, and has not to date been attempted for cryogenic circuits. When the temperature is reduced, both the source-body junction leakage and latch up can be tolerated with ever higher forward substrate bias. With the elimination of an additional isolation process, CMOS can be used "as is" for better performance, thus dramatically reducing design cost.

6. Summary

Measurements of CMOS devices in a commercially available SiGe HBT BiCMOS technology platform are used to assess their efficacy for emerging cryogenic Lunar applications, and reliability data of the nFETs with multiple gate lengths at low temperatures are reported. CMOS device performance improves at reduced temperatures, as expected, with higher carrier mobility, lower subthreshold swing, and higher current drive. However, CMOS device reliability becomes worse at decreased temperatures due to aggravated hot-carrier effects. The device lifetime is found to be a strong function of the gate length, suggesting that design trade-offs are inevitable for such space electronics applications.

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