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Topics: Switched capacitor, Sample and hold, Feedthrough, Operational amplifier and CMOS

CMOS Switched-Op-Amp-Based Sample-and-Hold Circuit

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***Abstract*—This paper presents a sample-and-hold design that is based on a switched-op-amp topology. Charge injection errors are greatly reduced by turning off transistors in the saturation region instead of the triode region as is the case for traditional MOS switches. The remaining clock feedthrough error is mostly signal-independent and is cancelled out by a pseudodifferential topology. Switched-op-amps are designed and fabricated in a 2-μ CMOS technology. The measurement results show that the harmonics are at least 78 dB below the signal level. Both the measurement results from fabricated IC's and simulation results suggest the potential benefits of this approach in comparison to traditional switched-capacitor circuits.**

***Index Terms*—Analog–digital conversion, charge injection, sample-and-hold circuits, switched opamp.**

I. Introduction

SAMPLE-AND-HOLD (S/H) circuits are important building blocks in data-converter systems. Traditional switched-capacitor (SC) techniques take advantage of the excellent properties of on-chip capacitors and MOS switches and permit the realization of numerous analog sampled-data circuits. Unfortunately, channel charge injection and clock feedthrough are the major sources of errors when the switch is turned off. Though many switching techniques [1]–[3] and circuit topologies [4]–[7] have been proposed and developed, the nonlinearity caused by charge injection and clock feedthrough still limits circuit performance, particularly in high-resolution data converters.

A MOS transistor holds mobile charges in its channel when it is on. When the transistor is turned off, a certain portion of this charge is released from the channel to the hold capacitor C_h, and the rest is transferred back to the voltage source [8], [9]. The charge transferred onto the hold capacitor while the transistor is turned off determines the total error as a result of charge injection. Clock feedthrough via the gate-to-source and gate-to-drain parasitic capacitances also contribute to this error. However, this error is largely voltage independent and less problematic. Charge injection and clock feedthrough are the primary errors that set the maximum usable resolution of an S/H. In the next few sections, we provide more detailed analysis about charge injection and clock feedthrough and propose a new technique based on switched op-amps (SOP's) to dramatically reduce this error.

The rest of this paper is organized as follows: We introduce channel charge injection and clock feedthrough errors in Section II. In Section III, we show our design for the SOP-based S/H topology with some preliminary simulations and discussions. In Section IV, measurement results are provided for our example design. These are followed by some conclusions in Section V.

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II. Charge Injection/Clock Feedthrough

In this section, we analyze channel charge injection and clock feedthrough errors and show that by turning off MOS devices while they are in the saturation region, all the channel charge flows into the source, leaving the drain terminal unaffected. As a result, signal-dependent channel charge injection error no longer exists.

The mechanism for charge injection and clock feedthrough can be illustrated with the help of Fig. 1. When a MOS switch is on, it operates in the triode region and has approximately zero voltage drop across the drain and source. There is a finite amount of channel charge in the inversion layer underneath the gate, which is given by [10]

$$Q_{\rm ch} = -WLC_{\rm ox}(V_{\rm GS} - V_T) \tag{1}$$

where

W, L	width and length of the MOS transistor, respectively;
$C_{\rm ox}$	gate capacitance per unit area;
$V_{\rm GS}$	gate-to-source voltage;
V_T	device threshold voltage.

Since the charge injected into the input source has no effect on the sampled-and-held value, we will concentrate only on the charge injected onto C_h. Given that the fraction of the channel charge that flows into C_h is k, the voltage change $\Delta V'$ due to the injected channel charge is given by (2). The fraction k depends on both the source and drain voltages as well as the impedances seen by them. So the parameters k, $V_{\rm GS}$, and V_T in (2) all depend on the input signal voltage and lead to nonlinear signal distortion

$$\Delta V' = \frac{k \cdot Q_{\rm ch}}{C_h} = -\frac{kWLC_{\rm ox}(V_{\rm GS} - V_T)}{C_h}. \tag{2}$$

Similarly the clock feedthrough error $\Delta V''$ due to the overlap and fringe capacitance is given by (3) where $C_{\rm para}$ stands for the parasitic capacitance and $V_{\rm DD}$ and $V_{\rm SS}$ are the high- and low-voltage values of the clock [10]. Contrary to channel charge injection error given by (2), clock feedthrough error is largely independent of the input signal

$$\Delta V'' = -\frac{(V_{\rm DD} - V_{\rm SS})C_{\rm para}}{C_{\rm para} + C_h}. \tag{3}$$

If, on the other hand, we are able to operate the MOSFET in the saturation region, then the channel will be pinched off and disconnected from the drain. In Fig. 2 a comparison is shown between the channel sheet model for a MOSFET operated in the triode region (top) and in the saturation region (bottom). If

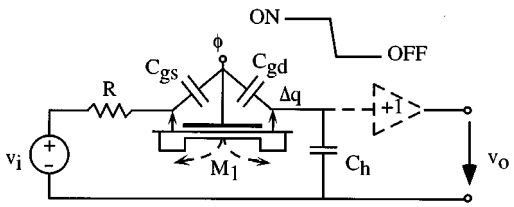

Fig. 1. Charge injection and clock feedthrough mechanism.

the hold capacitor is connected to the drain side, then when the transistor is turned off, all the channel charge will be injected into the source region while the drain side remains unaffected.

Using this basic concept, in the following sections, we propose a SOP [11] based S/H, in which the MOS transistors at the output node are turned off while they are operated in the saturation region. Hence no channel charge will flow into the output node. Clock feedthrough error, due to the parasitic gate-to-drain capacitance, still exists, but it is largely signal-independent and can be cancelled out by using a differential topology.

III. Switched-Op-Amp-Based Sample-and-Hold Circuits

In this section, we introduce our SOP-based S/H design, where our idea of turning off devices in the saturation region is implemented. First, we build a simplified model for our design and discuss the impact of circuit nonidealities. We then show our S/H circuit design and discuss its advantages over traditional SC S/H circuits.

A. Model and Simulation Results

Fig. 3 shows the block diagram of an SOP-based S/H. During the sample mode, the SOP behaves just like a regular op-amp. If the op-amp is assumed to be ideal, then during the sample mode, the S/H output follows the input. In the hold mode, the SOP is shut off and node A is held at high impedance. So the charge on C_h is preserved throughout the hold mode. The output buffer is operational during both the hold and sample modes and provides the voltage sampled on the capacitor C_h at the output.

To further reduce the signal-independent error caused by clock feedthrough, we use a pseudodifferential topology by duplicating the circuit shown in Fig. 3. If the two circuit halves are matched, then even this offset is cancelled out.

To verify this idea, we developed a simplified model for our SOP-based S/H design as shown in Fig. 4. It has two independent signal paths, which make the circuit pseudodifferential. Each signal path is an SOP-based signal-ended S/H. The differential pair in the operational transconductance amplifier (OTA) input stage is modeled by G_m blocks. R_1 and R_2 convert the output currents from the G_m blocks into voltages, which control the gates of M_1 and M_2 of the output stage. Both the current source I_b and the switches S_1 and S_2 are controlled by the clock ϕ. When ϕ is high, the switches are on, I_b supplies bias current, and the circuit is in sample mode. As ϕ goes low, the switches turn on and pull the gate voltages of M_1 and M_2 down to ground, turning them off. The bias current I_b is also turned off, leaving the drains of M_1 and M_2 at high impedance. Now the S/H is in the hold mode. The hold capacitors retain the sampled value and transfer it to the output via the unity gain buffers.

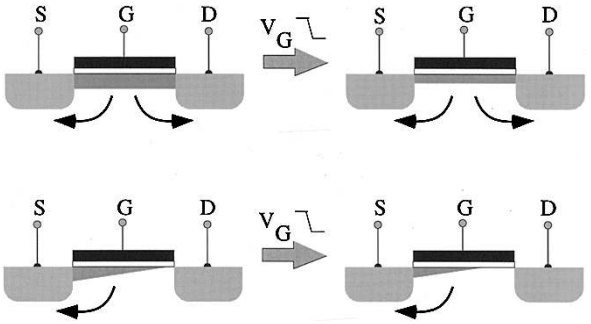

Fig. 2. Channel charge in (top) triode and (bottom) saturation.

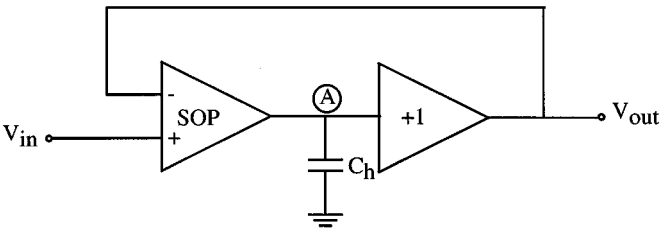

Fig. 3. Switched-op-amp-based S/H circuit.

We performed a transient analysis of the circuit using HSPICE with a sinusoidal input signal using Level 3 models for the MOS devices. The charge conservation algorithm was invoked by setting the option CAPOP $= 4$. Fig. 5 shows the differential sampled-and-held waveform where no nonideality can be observed.

To further evaluate the nonlinearity, we generated the power spectral density (PSD) of the input and the simulated (via HSPICE) differential output signals using Matlab. A total of 2^{16} data samples with 1000 samples per signal cycle were used. The data were windowed using the Blackman windowing function. The result is shown in Fig. 6.

As shown in Fig. 6, the even-order harmonics have been completely eliminated by the differential topology. The third harmonic of the differential output is below −102 dB, which corresponds to a 17-bit resolution. However, in reality, the resolution is likely to be even better than this, since we are limited by the numerical error of our simulator. Since the signal is a highly self-correlated sinusoidal waveform, some of the simulator's numerical error appears as harmonics instead of white noise. To validate this claim, we also computed the PSD of the input sinusoidal waveform, and the harmonics of output waveform is only slightly higher than that of the input waveform. This shows the superior linearity of our S/H circuit. This comparison is not shown here due to space limitation. As device noise is not modeled in this transient simulation, in practice, a higher noise floor in expected.

Though not conclusive, these simulation results are indicative of the performance that is provided with our new SOP-based S/H. We provide further evidence with measurement results from fabricated IC's in Section IV.

B. Circuit Implementation

We introduce the folded cascode SOP shown in Fig. 7. M_1 through M_{13} compose the regular slew-rate enhanced folded cascode OTA [10], and M_{14} and M_{15} form the unity-gain output

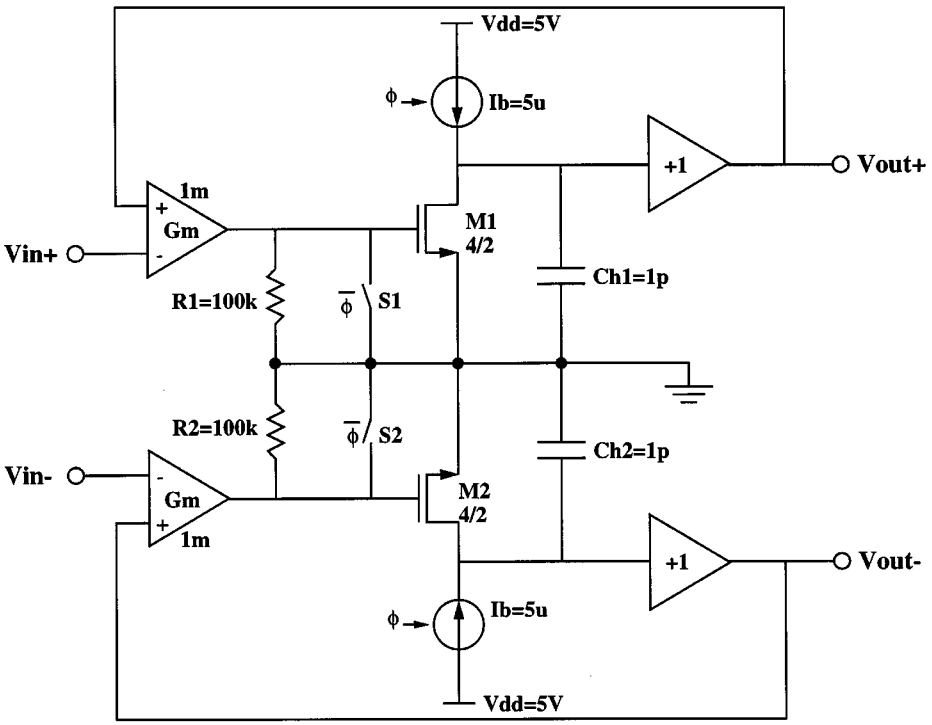

Fig. 4. Simplified model of the pseudodifferential SOP-based S/H.

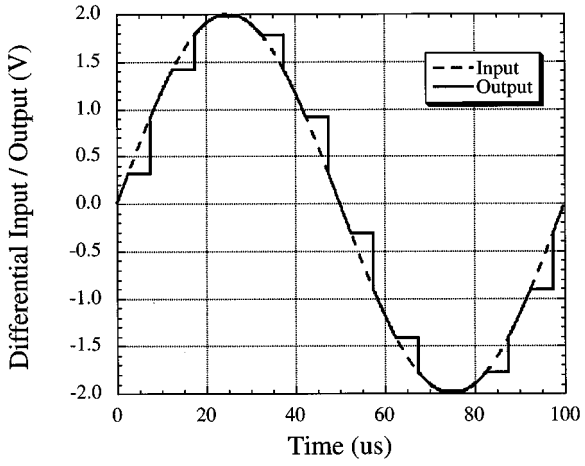

Fig. 5. Simulation results for a complete cycle of sampled-and-held waveform.

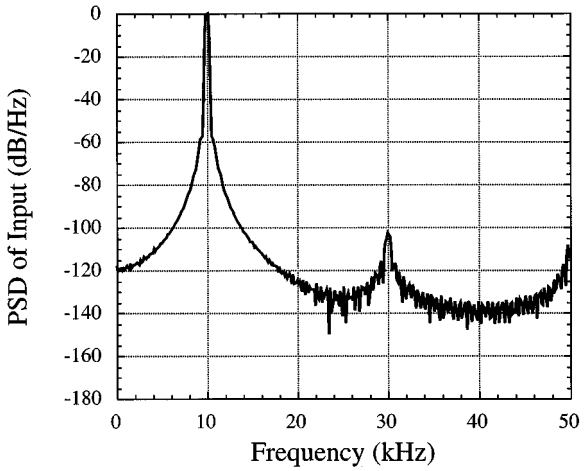

Fig. 6. Simulation results of the spectrum of the sampled-and-held waveform.

buffer. Four switches, M_{16}–M_{19}, have been added to turn the op-amp off at the end of the sample mode. In order to solve the charge sharing problem that occurs when the op-amp turns off, the clocks controlling nodes 3 and $pbias$ are slightly delayed with respect to the clocks controlling $ncas$ are $pcas$. Otherwise, nodes 1 and 2 have the potential to share charge with capacitor C_h, when the op-amp turns off.

Since channel charge injection no longer exists, clock feedthrough becomes the only source of error. The is due to the overlap and fringe capacitance of the transistors M_9 and M_{11}. To minimize this error as well as the impact of the leakage current when the devices are off, device widths for M_8 through M_{11} are minimized. The clock feedthrough errors due to M_{11} and M_9 are given by (4) and (5), where $C_{\rm Npara}$ and $C_{\rm Ppara}$ are the parasitic gate-to-drain capacitances of the NMOS and PMOS devices

$$V_{\rm Nerr} = -\frac{C_{\rm Npara}}{C_h + C_{\rm Npara}} V_{N_{\rm GS}} \tag{4}$$

and

$$V_{\rm Perr} = \frac{C_{\rm Ppara}}{C_h + C_{\rm Ppara}} |V_{P_{\rm GS}}| \tag{5}$$

All the values in (4) and (5) are either signal-independent or only a weak function of the input signal. The diffusion capacitances of the drains of M_9 and M_{11}, which make up part of the hold capacitance, are voltage-dependent. However, if designed with sufficient care, the variation of the parasitic capacitance due to the change of the input voltage will only be a small

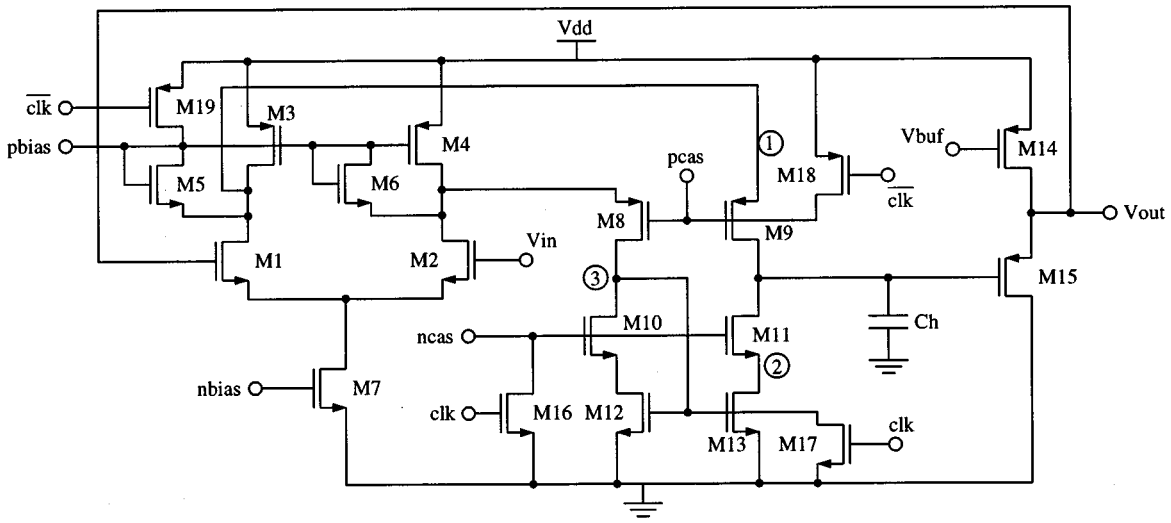

Fig. 7. Folded cascode switched op-amp in the unity-gain feedback configuration.

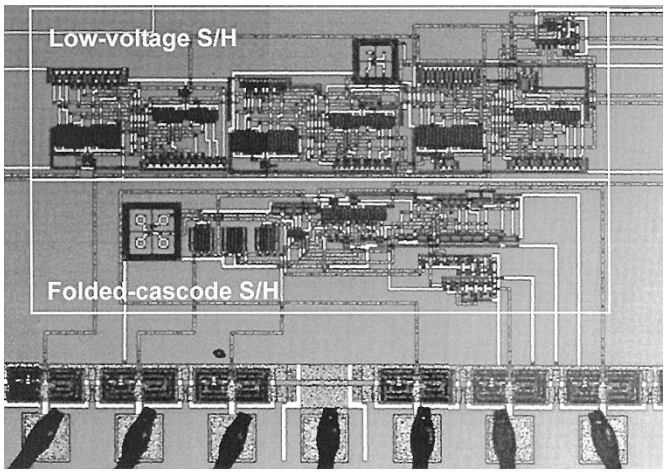

Fig. 8. Fabricated chip die photograph.

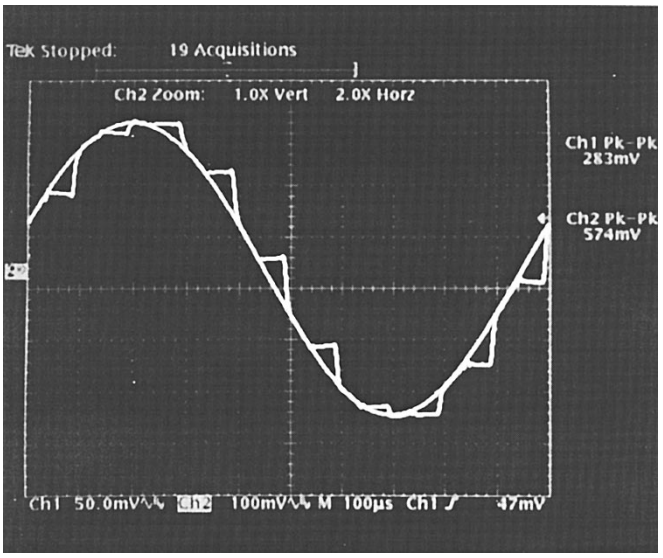

Fig. 9. A complete cycle of the differential sampled-and-held waveform.

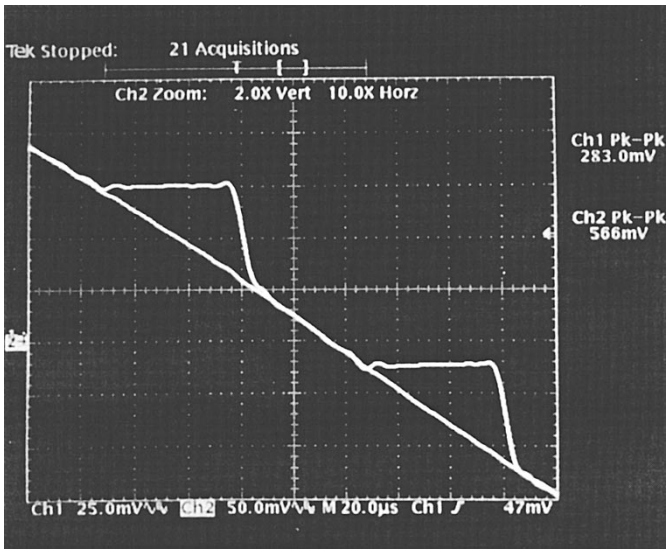

Fig. 10. A close-up view of the differential sampled-and-held waveform.

fraction of the total load capacitance. Moreover, since the clock feedthrough errors from M_9 and M_{11} have the opposite polarities, they tend to cancel each other to some extent. Furthermore, if we create a pseudodifferential version of the circuit and match the devices at the output, this remaining error is further reduced.

IV. Measurement Results

Two of our example designs were fabricated in a 2-µCMOS process. Circuit designs with transistors in both strong inversion and weak inversion were generated. The die photograph is shown in Fig. 8. The top circuit is an S/H capable of operating at 2 V of power supply, and its devices are operated in the weak inversion. The bottom one is an S/H using folded-cascode op-amps, as shown in Fig. 7. In this section, we provide measurement results that were used to verify our design. As will be seen, the measurement results are in good agreement with our theoretical analysis and computer simulations.

Time-domain measurement results for the differential output of the S/H with the folded cascode OTA's for a sinusoidal input signal is shown in Figs. 9 and 10. From this figure, it is clear that the input continuous-time signal and the sampled-and-held

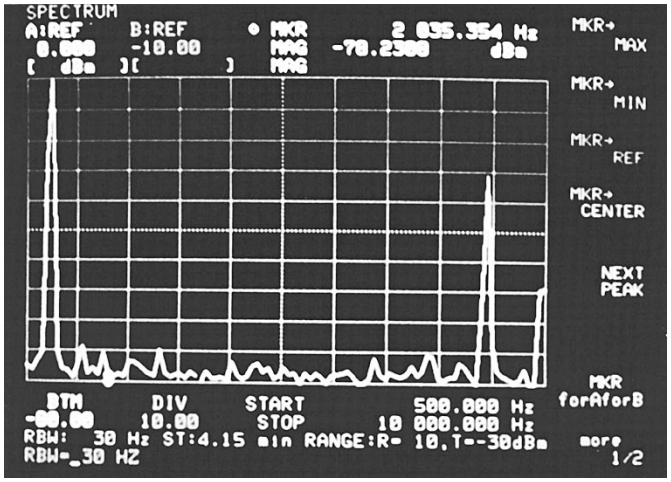

Fig. 11. Spectrum of the differential output waveform for the folded cascode S/H.

signal are perfectly aligned without noticeable offset or nonlinear errors. To further verify the operation of the S/H circuit, we performed a spectrum analysis of the differential output waveform. The result of this analysis is shown in Fig. 11. Each op-amp was biased at 0.8-μA current. For this test, a 1-kHz sinusoidal input signal was sampled at a frequency of 10 kHz. In Fig. 11, we see that the harmonics are buried in the noise floor, which is 78 dB below the signal. Hand calculations for the thermal noise of the op-amps for our capacitor size and bias conditions agree with these measurement results. A better design with less thermal noise could have been achieved by increasing the transconductance of the input differential pairs.

The S/H designed with devices in weak inversion was also tested, and similar performance was observed except for a higher noise floor due to the lower transconductance of the input differential pairs. Measurement results are not provided here due to space limitations, but it turns out that our design concepts are also valid for devices operated in the weak inversion region.

V. Conclusions

In this paper, a novel S/H design was introduced. The switches are turned off in the saturation region rather than in the triode region as in traditional MOS switches. Hence, the channel charge injection error is completely removed. The remaining signal-dependent clock feedthrough error is cancelled out by a pseudodifferential structure. In applications where the signal-independent offset is not important, a single-ended version of the S/H can be used. Simulation and measurement results show good agreement with our analysis.

Since our research motivation was for extremely low-power medical applications, our designs concentrated on signals at low frequencies. However, the basic idea can be extended to high-frequency applications. Since our design does not suffer from charge injection error, which is input signal-dependent, we expect to achieve the same linearity even with a smaller load capacitance. Thus high-speed operation can be achieved.

References

[1] U. L. McCreary and P. R. Gray, "All-MOS charge redistribution analog-to-digital conversion techniques," *IEEE J. Solid-State Circuits*, vol. SC-10, pp. 371–379, Dec. 1975.

[2] P. Van Peteghem and W. Sanaen, "Single versus complementary switches: A discussion of clock feedthrough in SC circuits," in *Proc. 12th Eur. Solid-State Circuits Conf. (ESSCIRC '86)*, Delft, the Netherlands, Sept. 1986, pp. 16–18.

[3] C. Eichenberger and W. Guggenbühl, "Dummy transistor compensation of analog MOS switches," *IEEE J. Solid-State Circuits*, vol. 24, pp. 1143–1146, Aug. 1989.

[4] M. Nayebi and B. A. Wooley, "A 10-bit video BiCMOS track-and-hold amplifier," *IEEE J. Solid-State Circuits*, vol. 24, pp. 1507–1516, Dec. 1989.

[5] P. J. Lim and B. A. Wooley, "A high-speed sample-and-hold technique using a miller hold capacitance," *IEEE J. Solid-State Circuits*, vol. 26, pp. 643–651, Apr. 1991.

[6] G. C. Temes, Y. Huang, and P. F. Ferguson Jr., "A high-frequency track-and-hold stage with offset and gain compensation," *IEEE Trans. Circuits Syst. II*, vol. 42, pp. 559–560, Aug. 1995.

[7] S. Brigati, F. Maloberti, and G. Torelli, "A CMOS sample and hold for high-speed ADC's," in *Proc. IEEE Int. Symp. Circuits and Systems Circuits and Systems Connecting the World*, vol. 1, May 1996, pp. 163–166.

[8] J. H. Shieh, M. Patil, and B. J. Sheu, "Measurement and analysis of charge injection in MOS switches," *IEEE J. Solid-State Circuits*, vol. SC-22, pp. 277–281, Apr. 1986.

[9] G. Wegmann, E. A. Vittoz, and F. Rahali, "Charge injection in analog MOS switches," *IEEE J. Solid-State Circuits*, vol. SC-22, pp. 1091–1097, Dec. 1987.

[10] D. Johns and K. Martin, *Analog Integrated Circuit Design*. New York: Wiley, 1997.

[11] J. Crols and M. Steyaert, "Switched-opamp: An approach to realize full CMOS switched-capacitor circuits at very low power supply voltages," *IEEE J. Solid-State Circuits*, vol. 29, no. 8, Aug. 1994.