CMOS T/R switch design : towards ultra-wideband and higher frequency

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CMOS T/R Switch Design: Towards Ultra-Wideband and Higher Frequency

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Abstract—This paper presents the comprehensive considerations of CMOS transmit/receive (T/R) switch design towards ultra-wideband and over 15-GHz frequencies. Techniques for minimizing parasitics and increasing linearity are discussed. A customized transistor layout is proposed for T/R switch design and its effects on insertion loss and isolation are studied. The analysis shows that a series-only architecture using the customized transistor layout achieves better insertion loss and reasonable isolation. A double-well body-floating technique is proposed and its effects are discussed. A differential switch architecture without shunt arms is designed and verified by experimental results. Fabricated in 0.13-μm triple-well CMOS, the T/R switch exhibits less than 2 dB insertion loss and higher than 21 dB isolation up to 20 GHz. With resistive body floating and differential architecture, the high linearity is of ultra-wideband characteristic, more than 30-dBm power 1-dB compression point $(\mathrm{P_{1dB}})$ is obtained up to 20 GHz in only 0.03 mm^2 active die area.

Index Terms—CMOS integrated circuits, cutoff, differential, floating body, MOSFET switches, RF switches, transmit/receive (T/R) switches, triple-well, ultra-wideband (UWB).

I. INTRODUCTION

WITH THE DEVELOPMENT of modern silicon technology, more and more high-frequency circuits can be implemented in standard CMOS process. Radio-frequency (RF) integrated circuits (ICs) in standard CMOS technology have proven feasible [1], and the trend of system-on-chip (SoC) requires further integration of transmit-receive (T/R) antenna switch in CMOS.

For years RF switch has been dominated by discrete components using PIN diodes and III-V MESFETs. Recently, CMOS T/R switch design has been explored to a certain extent. Regarding the performance of insertion loss and isolation, the effect of substrate resistance is studied in [2], [3], where low insertion loss was obtained by minimizing the substrate resistance and DC biasing the T/R nodes. A high isolation was achieved using CMOS-SOI technology [4]. In both cases, however, the linearity was limited due to the parasitic capacitance and source/drain junction diodes. Thus, techniques of body floating are developed for higher linearity. A LC-tuned substrate bias technique is firstly reported in [5], where the bulk is not separated from substrate. Using on-chip inductor can tune the bulk of switching transistor to be floating at certain frequencies. At 5.2 GHz, 28-dBm power 1-dB compression

point $(\mathrm{P_{1dB}})$ in the transmit mode was obtained. The disadvantages of this approach are the design complexity and large silicon area consumed. Taking advantage of modern triple-well CMOS process, the idea of body floating can be simply realized by using a large resistor to bias the bulk [6]. As resistors are intrinsically wideband, the linearity improvement of this approach is also wideband. 20-dBm $\mathrm{P_{1dB}}$ was achieved at 5.8 GHz. Another approach to linearity improvement is using stacked transistors [7], however, insertion loss will be degraded and has to be compensated, e.g., by the special DET process in [7]. A 15-GHz T/R switch is reported in [8], the impedance matching network was employed to improve the linearity, while the isolation performance is degraded. The linearity can also be improved by using differential architectures [9], 3-dB linearity improvement can be obtained.

Comparing with other RF IC circuits that have been pushed up to 60 GHz [10], CMOS T/R switches for higher frequency operations are explored only to a limited extent. Most of reported RF switches use a series/shunt architecture. At higher frequencies, the loss due to shunt-arm severely degrades the insertion loss. While the lack of shunt arm results in a low isolation. This paper presents a comprehensive consideration on the CMOS T/R switch design, with focus on the ultra-wideband (UWB) and over 10-GHz operations.

Section II discusses high-frequency considerations of the switch transistor in the cutoff region. A customized MOS layout technique for minimizing interconnect coupling is explored. Section III presents an improved double-well resistive body-floating technique for linearity enhancement. In Section IV, the advantage of differential architecture and its considerations on the T/R switch design are discussed, and the final circuits are presented. Section V shows the experimental results and discussions. The paper is concluded in Section VI.

II. SWITCH TRANSISTOR IN CUTOFF REGION

Conventionally, the T/R switch design follows a series/shunt architecture [2]–[4], [6], [8], [11], as shown in Fig. 1. The series transistors, $M1$ and $M2$, perform switch functions for TX and RX paths. The shunt transistors, $M3$ and $M4$, turn on when $M1$ and $M2$ are *off*, respectively, so that the undesired signal in each mode can be grounded by the shunt transistor. Previous analysis has proved that a shunt transistor improves the isolation effectively [11]. As the tradeoff, degradation on the insertion loss is observed, which is resulted from the parasitic capacitances of shunt transistors in the cutoff region. The impedances of these parasitic capacitances are large at relatively low frequencies, and the design effort is always put into the analysis of transistors in the triode region, acting as a voltage-controlled
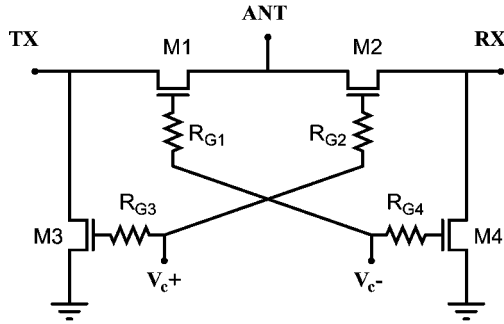
Fig. 1.   Schematic of series/shunt type single-ended T/R switch.
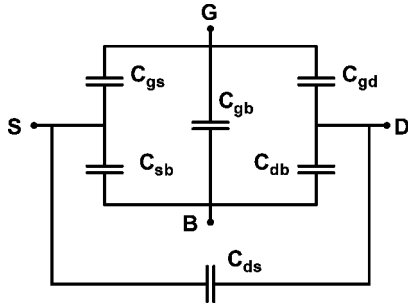
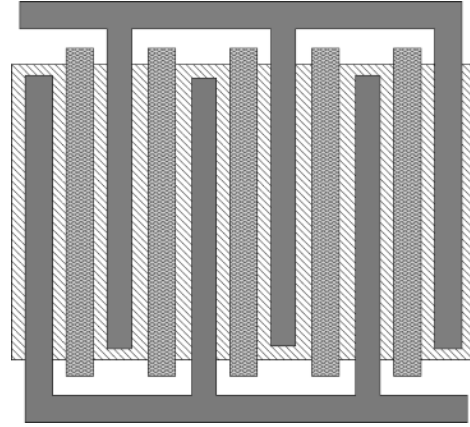Fig. 2.   Parasitic capacitances of a MOS transistor that is used as switch and turned off.

Fig. 3.   Layout sketch of an interdigitized MOS transistor used as a switch.

TABLE I
PARASITIC CAPACITANCES OF nMOS TRANSISTOR IN CUTOFF REGION, WHERE $W = 108\ \mu$m, $L = 0.13\ \mu$m, fingers $= 6$

Parasitic Capacitances	Foundry Layout (Fig. 4(a))	Customized Layout (Fig. 4(b))
C_{gs} (fF)	19	19
C_{gd} (fF)	19	19
C_{gb} (fF)	3.7	7.1
C_{sb} (fF)	9.3	37
C_{db} (fF)	8.3	33
C_{ds} (fF)	36	0

resistance. However, at high frequencies, the impedances of parasitic capacitances due to *off* transistors become small and more comparable to impedances of *on* transistors, leading to a severe impact of transistors in the cutoff region. Furthermore, observation of the series/shunt configuration shows that there is not only the shunt transistor but also another series transistor that is in the *off* state, each *on* transistor is connected by two *off* transistors, e.g., both $M2$ and $M3$ are *off* when $M1$ is *on*. Therefore, it is essential to investigate the high-frequency behavior of a switch transistor in the cutoff region.

Fig. 2 shows a model of high-frequency parasitic capacitances for a MOS that is used as a switch and turned off. The *off* resistance between drain and source is very large and not considered here. The parasitic capacitances, couple part of the signal to ground and lead to insertion loss degradation. As the channel is not formed, C_{gs} and C_{gd} are due to only overlap and fringing capacitances [12]

$$C_{gs} = C_{gd} = WL_{ov}C_{ox} \qquad (1)$$

where L_{ov} denotes the overlap distance between gate and source/drain, C_{ox} denotes the gate capacitance per unit area, and W is the width of transistor. Obviously, they are very small comparing to that of a MOS in saturation or triode region. C_{sb} and C_{db} become small as well when the channel is not present. They depend mainly on the area of source and drain, respectively.

Comparing with the small-signal model presented in [12], an extra capacitance C_{ds} is added in Fig. 2. For a standalone MOS transistor, C_{ds} is very small and normally not considered. However, when the transistor is used as a switch, the metal connection style exhibits severe coupling between drain and source,

and thus C_{ds} cannot be ignored. This can be explained by Fig. 3, where an interdigitized transistor layout sketch is shown. The metal connections of drain and source are in parallel and next to each other. When these metals are connected as a switch, they actually form a lateral metal capacitor, which is of high capacity [13]. This effect becomes more significant with the scale down of technologies, as the metal distance between drain and source decreases with smaller channel length.

The accurate values of these parasitic capacitances can be extracted from post layout simulations. Table I shows the extracted value of a nMOS transistor with $W = 108\ \mu$m, $L = 0.13\ \mu$m, fingers $= 6$. Note that some of capacitances are voltage dependent, the results shown in Table I are obtained with $V_{GS} = V_{GD} = V_{DS} = V_{SB} = V_{DB} = 0$. The values in the column *Foundry Layout* show the capacitances extracted from foundry provided layout (p-cell). A 36-fF C_{ds} is exhibited, which is much larger than any other capacitances and dominates the drain-source coupling effect in the cutoff region.

Therefore, a straightforward technique to improve isolation is reducing C_{ds}, which can be realized by increasing the distance between drain and source fingers. As shown in Fig. 4, the drain-source distance of a customized nMOS layout [Fig. 4(b)] is 4 times the p-cell default [Fig. 4(a)]. Table I gives also the parasitic capacitances extracted from the customized layout under exactly the same condition. It is shown that C_{ds} has been reduced to a value that can be omitted by the simulation tools. The
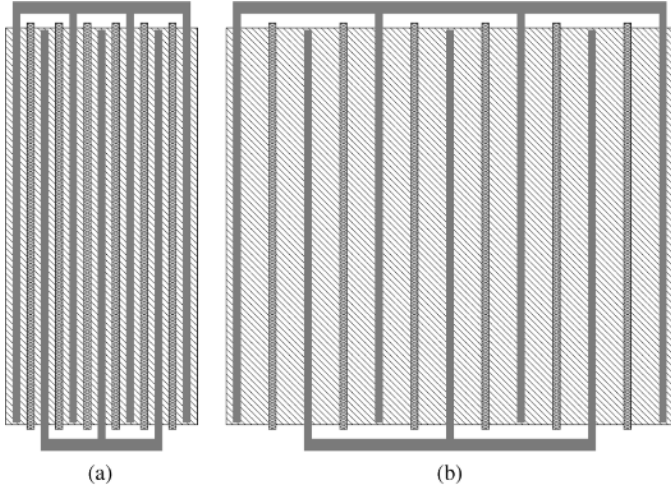
Fig. 4. (a) Foundry provided p-cell and (b) customized layout of a nMOS transistor operating as a switch. $W = 108\ \mu$m, $L = 0.13\ \mu$m, fingers $= 6$. The drain-source distance in the customized layout is 4 times that in the standard p-cell.
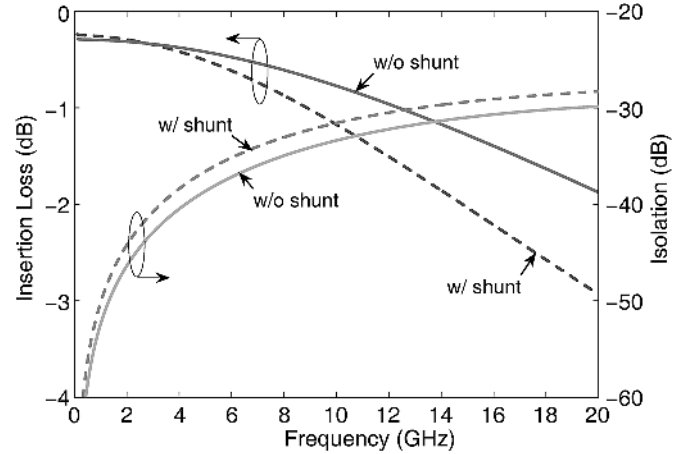

Fig. 5. Simulated insertion loss and isolation of T/R switch with and without shunt arm. The switch without shunt arm employs customized layout of Fig. 4(b).

drawback of this decoupling technique is due to the increased drain and source area, where C_{sb} and C_{db} also increase by a factor around 4. For the gate parasitics, C_{gs} and C_{gd}, there is no difference according to (1). C_{gb} is nearly doubled.

The impacts of customized layout on the T/R switch performances are discussed as follows. Based on the configuration of Fig. 1, the bulk is connected to ground, and the gate is biased through a large resistor to create a floating node at RF. When the transistor is used as the series transistor and is *on*, the increased drain and source area increases C_{sb} and C_{db}, insertion loss will be certainly degraded. It is a typical case of operation and agrees to the well-known principle that drain and source area should be minimized in high-frequency designs. However, when the transistor is *off*, the customized layout provides better isolation. The overall drain-source coupling capacitance can be written as

$$C_{\text{OFF}} = C_{ds} + \frac{C_{gs} \cdot C_{gd}}{C_{gs} + C_{gd}}. \qquad (2)$$

It is shown that C_{OFF} is reduced significantly from 45.5 fF for the standard layout to 9.5 fF for the customized layout, which provides directly better isolation when the switch is used as the series transistor and is *off*. Furthermore, when this transistor is used as the shunt transistor, the smaller C_{OFF} leads to smaller loss, which poses positive effect on the overall insertion loss. Again, the increase of C_{sb} and C_{db} increases the loss due to shunt transistor and degrades the overall insertion loss.

Briefly, the overall performance depends severely on the transistors operating in the *off* state, especially for switch targeting on high-frequency applications. The customized layout provides better isolation due to the drain-source decoupling, and degrades the insertion loss due to the increase of parasitics regarding the bulk (C_{sb} and C_{db}).

The increase of C_{gb} slightly affects the *on/off* transition speed and is not considered to affect steady-state performances. Note that the increased drain/source area also increases the ohmic loss. However, the overall resistance of drain/source region is still very small comparing to that of the *on* resistance of switch transistors. It is expected that a slight degradation of insertion loss can be observed at DC and low frequencies.

Further observing the series/shunt configuration in Fig. 1, the shunt arm has to provide sufficient large impedance when it is turned off, so that insertion loss can be prevented from severe degradation. At high frequencies, the capacitive coupling effect becomes significant, leading to a shunt path with lower impedance and thus higher loss. At the same time, the presence of shunt arm degrades the power handling capability as the unintentional turn on of the shunt transistor increases loss significantly [5], [6]. Thus, when the isolation can be maintained with other method, the shunt arm becomes not necessary and can be removed to improve the insertion loss and linearity performances.

Fig. 5 shows the simulated performances of T/R switches with and without shunt arms. Both results are obtained from post-layout simulations. For the switch with shunt arms, the sizes of series transistors and shunt transistors are 108 μm/0.13 μm/6 fingers and 21 μm/0.13 μm/3 fingers, respectively. The layout employs standard p-cells. For the switch without shunt arm, the sizes of series transistors are 108 μm/0.13 μm/6 fingers, and customized layout of Fig. 4(b) is employed. In the simulations, the signal is biased at 0.5 V and the high and low control voltages are 2 V and 0 V, respectively. It is shown that the customized switch layout achieves 2 dB better isolation comparing with standard transistor layout, and this result is obtained without shunt arms. Thus, the insertion loss and isolation tradeoffs due to shunt transistors are relaxed. Benefiting from the absence of shunt arms, significant improvement of insertion loss at high frequencies can be observed. Note that at frequencies below 3 GHz, the insertion loss of customized layout is slightly higher than that of the standard layout, which is due to the increased drain/source ohmic loss and has been predicted previously. The linearity performance is also improved without shunt arms. At 10 GHz, 19 dBm $P_{1\text{dB}}$ is obtained for the switch without shunt arms, while only 15 dBm $P_{1\text{dB}}$ is obtained for the switch with shunt arms.
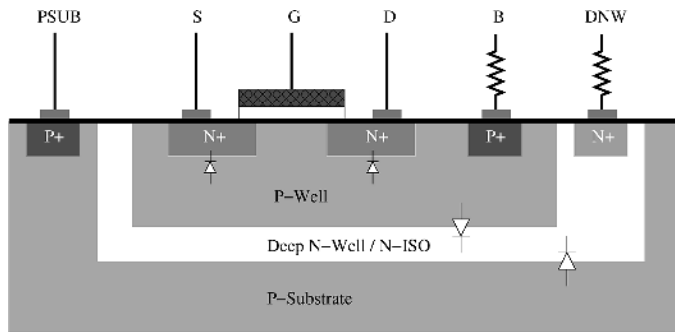
Fig. 6. Simplified cross-sectional view of a nMOS transistor in triple-well technology.

Fig. 7. Simulated linearity performance for T/R switch with and without shunt arms, and with different types of body-floating.

III. DOUBLE-WELL BODY FLOATING

The linearity of a T/R switch determines its power handling capability. The problems of linearity can be considered by different points of view. One is from the point of unintentional turn-on of junction diodes [2], [5]. Normally, the gate-source and gate-drain can be kept around the proper value as the gate is RF floating and its voltage is bootstrapped. But a strong signal still turns on the source-bulk and/or drain-bulk diodes, which clips the signal itself. Note that this happens in both series transistor and shunt transistor, and it is the reason that a shunt arm degrades the power handling capability. Based on this point of view, the linearity performance can be improved by either giving a large voltage headroom for these diodes or bootstrapping the bulk voltages. The former can be realized by large DC bias at sensitive nodes, at the price of reliability. While the latter can be done by floating the bulk at RF. LC-tuned substrate bias has to be employed when the bulk is not separated from the substrate. Another view of linearity problem is from the DC I-V characteristics [6]. The similar body-floating approach to linearity improvement can be reached. The use of impedance transformation networks can also improve the power handling capability [8].

Nowadays, the triple-well process is becoming commonly available for analog and mixed-signal designs, which offers better performance in terms of noise, isolation, bulk control, etc. Fig. 6 shows the simplified cross-sectional view of a nMOS transistor in triple-well CMOS technology. The buried deep N-well separates the body of nMOS from the common substrate. Thus, the body can be easily biased through a large resistor. In a similar manner with gate bias, the bulk becomes RF floating and its voltage is bootstrapped to the source and drain voltages.

The resistive body-floating technique has been realized in 2.4 and 5.8 GHz and reported in [6], the result shows that 20–21 dBm P_{1dB} can be obtained by floating the P-well through resistors. Although the area is saved comparing with LC-tuned approach, the linearity improvement is not comparable to that with LC-tuned body-floating [5] technique, where more than 28 dBm P_{1dB} was achieved.

The comparison result leads to a further study of the diode models in triple-well process. As can be seen in Fig. 6, the adding of the deep N-well layer creates two more diodes: the diode between P-well and deep N-well, and the diode between
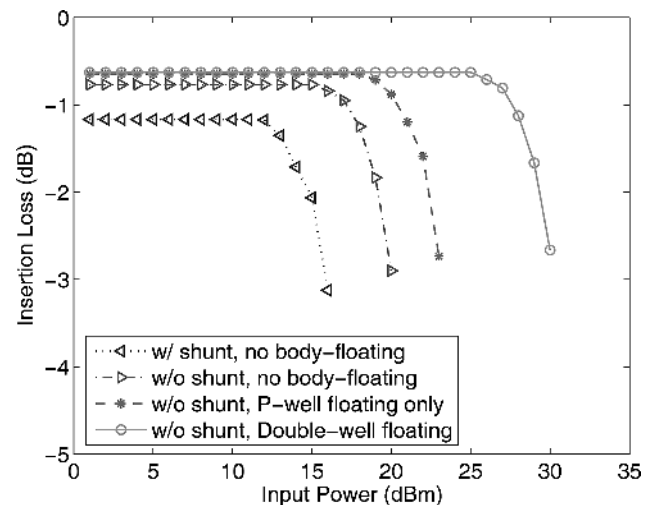
deep N-well and P-substrate. When the body is floated by a large resistor, the transient voltage of P-well is actually bootstrapped to the signal voltage. This prevents the source-bulk and drain-bulk diodes from being turned on by large signals and improves the linearity. However, the diode between P-well and deep N-well becomes unprotected and can be turned on by large P-well voltages. This would not happen if the P-well is biased directly by a DC voltage (RF grounded), but the bootstrapped P-well voltage depends on the signal voltage and thus may turn on the diode between P-well and deep N-well. Once the turn-on happens, the RF-floating state of the body (P-well) is broken and the linearity will get degraded immediately.

To overcome the body-floating limitation presented above, the deep N-well should also be floated. With both terminals floated, the diode between P-well and deep N-well is then made safe. In a similar manner, the diode between deep N-well and P-substrate is then unprotected and may be turned on by large signals. However, as the bootstrapped effect of these voltages is degressive, the signals that can turn on the outer diode need to be very large.

Fig. 7 gives the linearity simulation results with different switch configurations at 10 GHz. As discussed previously, the presence of shunt arms decreases the linearity, only 15 dBm P_{1dB} is obtained for a switch with shunt arms and 19 dBm is obtained for that without shunt arms. Both results are simulated without body floating. With a P-well-only floating resistor of 5 kΩ, the P_{1dB} is improved to 22 dBm. Dramatic improvement of linearity is observed when a second 5-kΩ resistor is used to further float the deep N-well. With resistive body-floating for both P-well and deep N-well, 29 dBm P_{1dB} is obtained. These results exhibit clearly the influence of junction diodes on the linearity performance and the efficiency of double-well body-floating.

Furthermore, the body-floating will certainly affect the insertion loss and isolation performances, especially when it is combined with the proposed custom layout scheme. For a switch transistor that is turned on, the parasitic capacitances regarding body, C_{sb} and C_{db}, will no longer affect the insertion less as
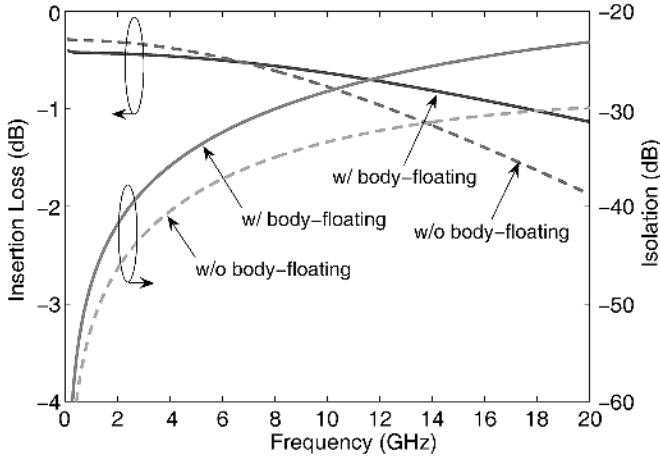
Fig. 8. Simulated insertion loss and isolation with and without body-floating. Both switches use the proposed custom layout and have no shunt transistors. Double-well body-floating is used.

Fig. 9. Final schematic and circuit parameters of the differential T/R switch.

they are now floated. Thus, the negative effect of increased drain and source areas for *on*-transistor is eliminated. On the other hand, when the transistor is turned off and the body is floating, from Fig. 2, C_{sb} and C_{db} become in series between drain and source. The increased drain-source coupling occurs, which will degrade the isolation. For the transistor parameters of Table I, the coupling capacitance, C_{OFF}, increases again from 9.5 fF to 27 fF. Although it is still smaller than that from a standard p-cell, the increased coupling degrades the efficiency of the custom layout on the isolation performance. Fig. 8 shows the simulated insertion loss and isolation for a switch with and without body-floating. Double-well body-floating is used in the comparison. Both circuits employ the proposed custom layout and have no shunt transistors. It is clear that the insertion loss is improved and isolation is degraded with body-floating technique. Note that at frequencies below 7 GHz, the insertion loss of the switch with body-floating is slightly higher than that of the switch without body-floating. This is interesting and may result from the body effect due to the large body-floating resistances.

IV. DIFFERENTIAL T/R SWITCH

The differential configuration of circuits results in an improved power handling capability comparing with single-ended configurations. From the power point of view, differential output scheme is able to handle twice over the single-ended output power, that is, 3 dB higher P_{1dB} could be achieved [9]. As the power handling capability is the bottleneck of CMOS T/R switches, differential architecture is of great advantage in current silicon technology. Furthermore, comparing with single-ended architecture, the differential nature permits higher linearity, lower offset, makes it immune to power supply variations and substrate noise. Therefore, differential architecture is normally preferred in applications requiring higher signal quality. Nowadays most of transceivers are designed with differential architecture, exploring the design of integrated differential T/R switch is essential for these transceivers.

The differential architecture poses extra considerations on the two matched signal paths. For single-ended T/R switches, practical problems include substrate resistance, source/drain para-
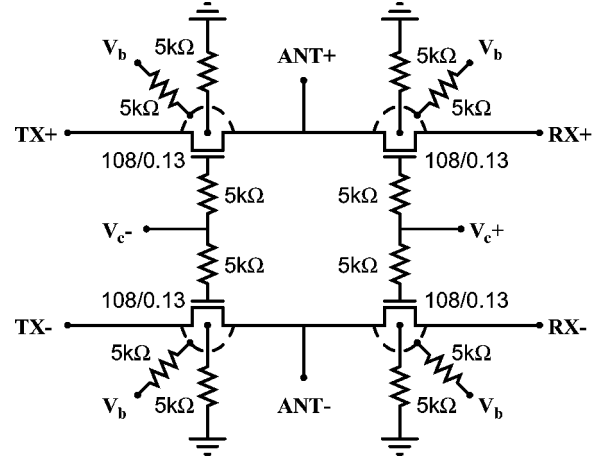
sitics, DC biasing, and transistor sizing [2], [4], [5]. For differential T/R switches, however, issues on crosscoupling and layout matching between the two signal paths should also be considered. Tradeoffs exist among these issues. Briefly, good matching of transistors (and resistors) requires a close placement, whereas crosstalk increases when transistors are placed near to others.

It depends on the application and system requirement to determine the layout strategy. In general, unintentional crosstalk and coupling increase the nonlinearity, resulting in degradation on the insertion loss performance and power handling capability. On the other hand, mismatch is a signal independent process, which does not cause signal dependent problems as crosscoupling does, e.g., crosscoupling may distort signal waveform, while mismatch only results in a DC offset in most cases. Therefore, considerations in this paper are placed on reducing the effect of crosscoupling, at the price of mismatch degradation. For instance, the transistors in different operating status (*on* and *off*) are placed far away to avoid crosscoupling. The layout matching techniques, e.g., common centroid, are intentionally not used.

The final circuit is shown in Fig. 9. The dashed line denotes the deep-N-well isolation. Only four switch transistors are employed. The transistor count of the proposed differential T/R switch is exactly equal to that of a single-ended switch with shunt arms. The customized layout is employed for all switch transistors.

V. MEASUREMENT RESULTS AND DISCUSSIONS

The final differential T/R switch circuit was fabricated in a 1.2-V two-poly eight-metal 0.13-μm triple-well CMOS technology. The cut-off frequency f_T of nMOS transistor is over 90 GHz. Fig. 10 shows the die microphotograph of the fabricated differential T/R switch. The active area of the switch is only 180 μm $\times$ 150 μm. With test pads, the whole T/R switch chip occupies 415 μm $\times$ 415 μm die area.

The measurements are carried out on wafer, using Cascade Microtech's differential G-S-S-G probes. A four-port network analyzer was employed in the experiment, which avoids the complicated on-chip balun design for testability. The control voltage is 2/0 V and the TX/RX nodes are biased at 0.5 V. The body (P-well) and P-substrate are biased at 0.5 V and
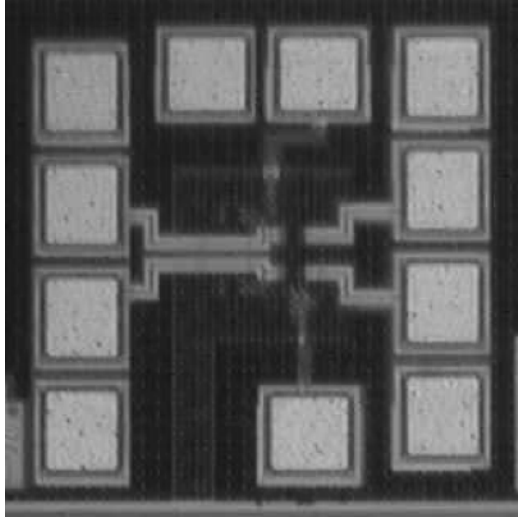
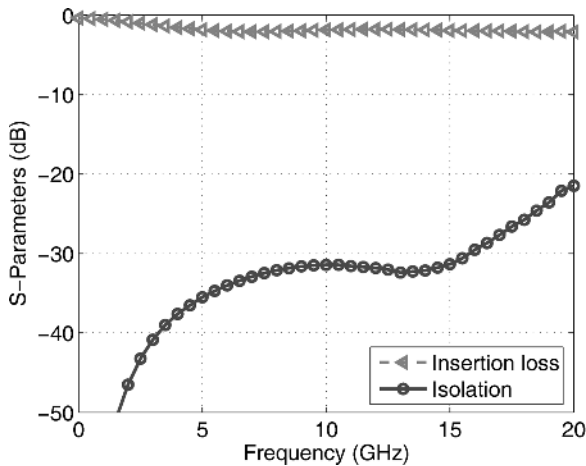Fig. 10. Die microphotograph of the fabricated differential T/R switch.

Fig. 12. Measured insertion loss and isolation parameters for the common-mode small-signals.

Fig. 11. Measured insertion loss and isolation parameters for the differential-mode small-signals.

trends up to 6 GHz. Review of previous publications shows this may result from the parasitic inductances. In [8], the switch designed with LC network shows a rather improved insertion loss at frequencies above 7 GHz, while the switch without LC network does not show that. The LC network changes the input impedance and may offer higher available input power at certain frequencies, therefore, the insertion loss may be improved at that frequency. In this design, the parasitic inductances of the input metal lines are relatively small, the LC resonance occurs at much higher frequency, and the effect is not large enough to exhibit an improved insertion loss characteristic.

B. Common-Mode Performance

The common-mode performance is of little importance, it is presented here mainly for comparisons with differential-mode performance. Fig. 12 shows the common-mode insertion loss and isolation performances. The insertion loss is within 7.9 dB over DC to 20 GHz. At 0.9, 5.8, 10, 15, and 20 GHz, the insertion loss is 1.1, 1.7, 3.2, 6.5, and 7.9 dB, respectively. The isolation is below 22 dB at frequencies up to 20 GHz.

It is shown the common-mode insertion loss is severely degraded comparing to the differential-mode signals. Similar observation can also be found in [9], which is caused by the severe coupling and loss of common-mode signals. The parasitic inductances have little impact on the common-mode insertion loss due to the large value of the loss.

Observing Fig. 11 and Fig. 12 shows that the LC resonance probably occurs at around 12 GHz. It is interesting to note the effects of such resonance: for insertion loss, the effect is positive for differential-mode signals and negative for common-mode signals; while for isolation, the effect is negative for differential-mode signals and positive for common-mode signals.

C. Common-Mode Rejection

The common-mode rejection ratio (CMRR) is measured by the forward transmission coefficient from the transmitted common-mode signal to the received differential-mode signal. Obviously, the CMRR is related to the *on-off* conditions of differential switch. In the *on* and *off* state, the common-mode rejection performances are shown in Fig. 13. In the *on* mode,

the deep-N-well is biased at 2 V. Note that the differential impedance at each port is 100 Ω, and the common-mode impedance is 25 Ω.

For a differential circuit, performances need to be considered include not only the differential-mode parameters, but also common-mode parameters and common-mode rejection performance. For a T/R switch that working in two status (*on* and *off*), these performances should be evaluated in both cases.

A. Differential-Mode Performance

Fig. 11 shows the differential-mode insertion loss and isolation performance. The insertion loss is within 2.0 dB over DC to 20 GHz. At 0.9, 5.8, 10, 15, and 20 GHz, the insertion loss is 0.7, 1.5, 1.7, 1.7, and 2.0 dB, respectively. The isolation is below 21 dB at frequencies up to 20 GHz.

The results are close to the simulation results in Fig. 8, however, the trends in Fig. 11 are different from that in Fig. 8. It is shown that the degradation effect of insertion loss at higher frequencies becomes slower at frequencies above 8 GHz. The differential T/R switch reported in [9] does not exhibit such
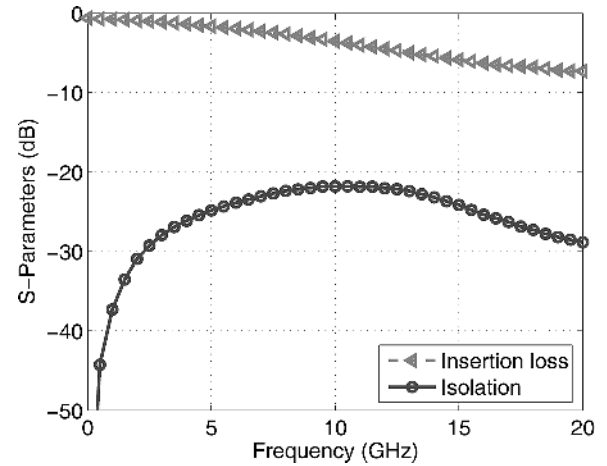
TABLE II
SUMMARY OF DIFFERENTIAL SWITCH PERFORMANCE AND COMPARISON WITH REPORTED STATE-OF-THE-ART DESIGNS

	Insertion Loss (dB)					Isolation (dB)					P_{1dB} (dBm)	CMOS Technology
	2.4-GHz	5.8-GHz	10-GHz	15-GHz	20-GHz	2.4-GHz	5.8-GHz	10-GHz	15-GHz	20-GHz		
This Work [*]	**0.9**	**1.5**	**1.7**	**1.7**	**2.0**	**43**	**34**	**32**	**32**	**21**	**30**	**0.13-μm TW[○]**
[8] [†]	—	—	1.1	1.8	—	35	29	24	18	—	21.5	0.13-μm
[6] [†]	0.7	1.1	—	—	—	35	27	—	—	—	21.3	0.18-μm TW[○]
[5] [†]	1.5	1.4 [‡]	—	—	—	32	30 [‡]	—	—	—	28.5	0.18-μm
[3] [†]	—	0.8	—	—	—	—	29	—	—	—	18	0.18-μm
[11]	1.5	—	—	—	—	24	—	—	—	—	11 [◁]	0.18-μm
[9] [*]	0.79	1.7 [‡]	—	—	—	20	16 [‡]	—	—	—	20	0.18-μm

[*] Performances in differential-mode.
[†] Best available insertion loss and isolation in case of multiple designs, or highest P_{1dB} among different frequencies.
[‡] Performances at 5.2-GHz.
[◁] 0.2-dB gain compression point ($P_{-0.2}$ dB).
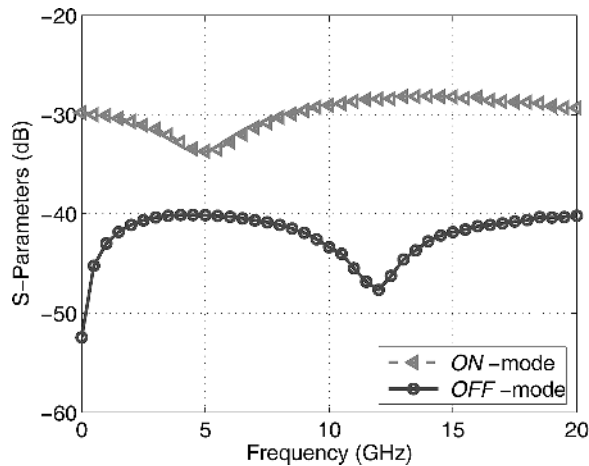[○] triple-well process (with a deep n-well isolation).

Fig. 13. Measured common-mode rejection ratio in the *on* and *off* state of the differential T/R switch.

Fig. 14. Power handling capability in terms of P_{1dB} at different frequencies.

the common-mode rejection is better than 28.7 dB. In the *off* mode, it is better than 40 dB.

From Fig. 13, it is more clear that the LC resonance occurs at about 12 GHz. Its effects are also opposite in *on* and *off* state of the switches.

D. Power Handling Capability

Fig. 14 shows the 1-dB compression point of the differential T/R switch. The P_{1dB} increases from 24.6 dBm at 1 GHz up to 30.2 dBm at 8 GHz, and it remains at the level around 30 dBm at frequencies above 8 GHz. This is reasonable considering the insertion loss degradation is reduced above 7 GHz due to the parasitic LC network. Similar improvement on linearity performance can be found in [8], where LC network is designed intentionally for higher power handling capability.

Note that 3 dB improvement in P_{1dB} is benefited from the differential architecture, without which the P_{1dB} is around 27 dBm. It is slightly lower than the simulated value of 29 dBm. Comparing with the 21.3 dBm and 20 dBm P_{1dB} obtained
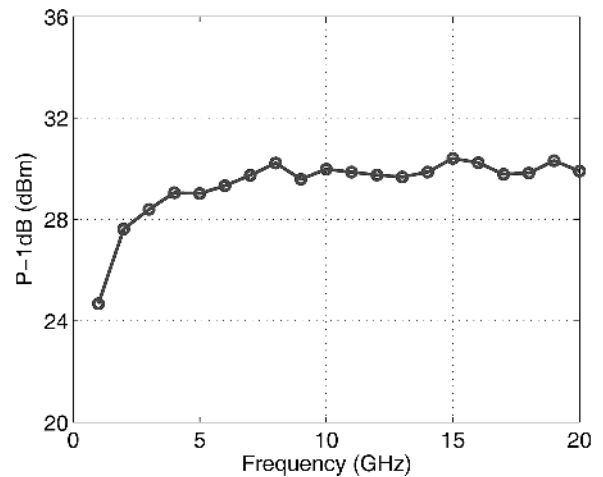
by single-well resistive body-floating [6], the power handling capability is improved significantly using double-well body floating technique.

Table II shows a summary of the measured performance of the differential T/R switch. The comparison with other reported state-of-the-art CMOS T/R switch designs is also presented. The T/R switch presented in this work achieves 20-GHz operating frequency, which is the highest among reported CMOS T/R switch designs. The bandwidth and linearity is suitable for UWB wireless transceiver front-ends. It can also be used in other potential wireless applications with up to 30-dBm transmit power level and 20-GHz bandwidth.

VI. CONCLUSION

This paper demonstrates a CMOS T/R switch designed for ultra-wideband and higher frequency applications. At frequencies above 6 GHz, the widely used series-shunt architecture of CMOS T/R switch encounters difficulties in achieving good insertion loss with reasonable isolation and linearity performances. The bottleneck lies in the operations of switch

transistors in the cutoff region. This issue was investigated and a customized transistor layout was proposed to minimize the parasitic capacitances due to drain-source interconnections, which permits a series-only architecture with better insertion loss and reasonable isolation. Benefitting from the triple-well process, the resistive body-floating technique can be used to improve the wideband power handling capability. A double-well resistive body floating was explored and the body-floating effects on the insertion loss and isolation performances were studied. The switch employs also the differential architectures for better linearity and other performances. The design analysis and approaches were verified by experimental results. Fabricated in 0.13-μm triple-well CMOS, the T/R switch exhibits less than 2 dB insertion loss and higher than 21 dB isolation up to 20 GHz. 30-dBm input P_{1dB} is obtained. The results shows that the CMOS T/R switch is capable of ultra-wideband and even higher frequency operations.

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