Coat Circuits for DC-DC Converters to Improve Voltage Conversion Ratio

Binxin Zhu[1]*, *Member, IEEE*, Feng Ding[1] and D. Mahinda Vilathgamuwa[2], *Senior Member, IEEE*

***Abstract*—The voltage conversion ratio of basic DC/DC converters is limited due to the influence of parasitic elements of circuits and components. In this paper, a family of passive circuits termed as "coat circuits" are proposed for conventional DC/DC converters. Not only voltage step-up capacity can be improved but also the voltage stress of components can be decreased by adding coat circuits to basic DC/DC converters. Moreover, no additional active switches are needed in the coat circuits, that means the control and driver circuits of the converters are not changed. Cuk converter with the coat circuit has been analyzed as an example, and a 200W experimental prototype has been built to verify the validity of the theoretical analysis.**

***Index Terms*: coat circuit, basic DC/DC converter, voltage conversion ratio**

I. Introduction

Conventional basic DC/DC converters such as buck, boost, buck-boost, Cuk, SEPIC and Zeta circuits are widely used in various industrial and consumer applications. In ideal conditions, by adjusting the duty cycle of the switch, any voltage conversion ratio can be achieved using these converters. However, in actual working conditions, the boost capacity of these converters is greatly limited by parasitic elements of the circuit and the voltage drop across the switch and diode [1-3]. And this also makes the application of basic DC/DC converters difficult in situations where a wider input and output voltage range or a larger voltage conversion ratio is required [4-7].

To achieve a high voltage conversion ratio, many solutions such as the use of transformers, coupled inductors, cascade structures, switch-capacitors, voltage multipliers (VMs) or combination of aforementioned techniques have been proposed. However, the use of transformer would increase the overall size and cost of the system in situation where isolation is not required [8-9]. The leakage inductive energy of the coupled inductor needs to be considered as it not only increases voltage stress across the switching devices but also necessitates the deployment of complex snubber circuits [10-12]. When cascaded converters are used several stages are required and that apparently increases the cost and reduces the efficiency of the system. Furthermore, it requires high voltage components at the output stage [13-14]. Switched capacitor converters have some fundamental problems such as the requirement of large switches, pulsating input current and complex driving circuit [15-16]. High voltage conversion gain can also be achieved by combining voltage multipliers (VMs) with the conventional boost converters [17-23] where some common advantages like adjustable voltage conversion ratio, lower voltage stresses on semiconductor components are evident. However, there are also some common disadvantages, firstly, at least two-phase interleaved boost converters have to be used together with the VMs, secondly, the combined duty cycle of the two switches has to be greater than 1 and there are limitations/boundaries of the selectable duty ratios. Based on buck-boost and SEPIC converters, two high step-up DC/DC converters capable of low voltage stress on the switch are proposed in [24] and [25] respectively. These two converters do not need additional switches, the control and drive circuit is as simple as basic DC/DC converters. However, as the topological structure of these two converters is fixed, the high step-up voltage conversion capacity of such converters cannot be changed.

This paper presents a family of generalized passive circuits termed as "coat circuits" for DC/DC converters to acquire a variable high voltage step-up capacity. These circuits are termed as coat circuits because such circuits surround the DC/DC converters like a coat and they only need additional passive elements to fit the voltage conversion ratio requirement akin to tailoring coats for peoples' body frame requirements. The proposed coat circuits do not need any additional active switches, and they do not affect the control or driver circuit design. Topology, working principles and performance characteristics of the DC/DC converters with the proposed coats are discussed in sections II and III respectively. The accuracy of the theoretical analysis and the converter characteristics are verified by experiments in section IV.

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B. Zhu and F. Ding are with the College of Electrical Engineering and New Energy, China Three Gorges University, Yichang, Hubei, CN (e-mail: zhubinxin40@163.com, dingfeng321@163.com). D. M. Vilathgamuwa is with the School of Electrical Engineering and Computer Science, Queensland University of Technology, Brisbane, Queensland, AUS (e-mail: mahinda.vilathgamuwa@qut.edu.au).

II Topologies And Working Principle

Fig. 1 shows the topologies of the basic DC/DC converters with the proposed coat circuits. The structure of coat circuit for boost and SEPIC converters is identical and there are also two other common characteristics among these coat circuits.

1) All coat circuits are composed of several basic units, and the number of basic units can be adjusted according to the application requirements.

2) Each basic unit of the proposed coat circuits contains two capacitors, one inductor and one diode.

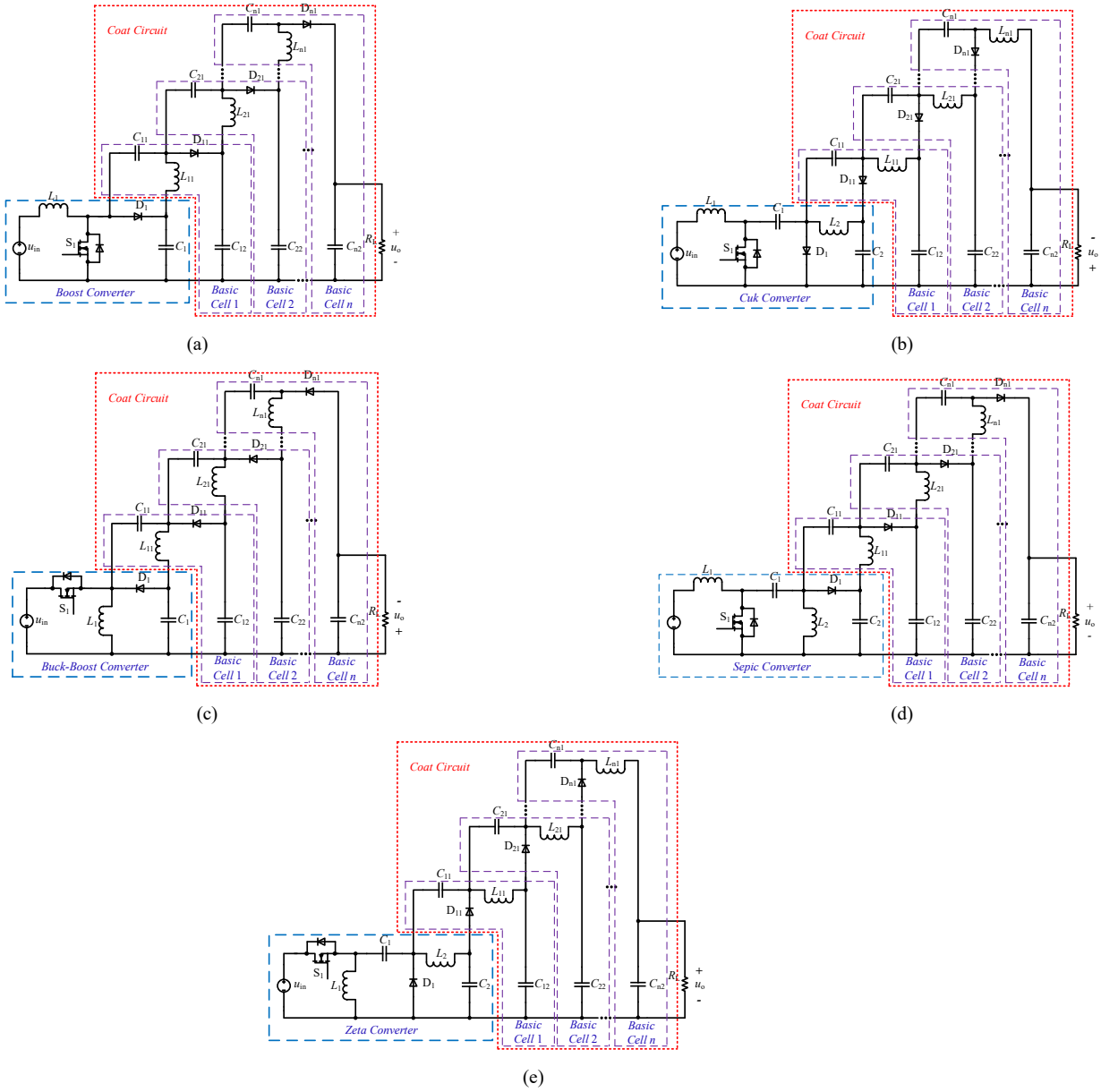


Fig. 1. Topologies of the DC/DC converters with the proposed coat circuits: (a) boost converter, (b) Cuk converter, (c) buck-boost converter, (d) SEPIC converter, (e) Zeta converter.

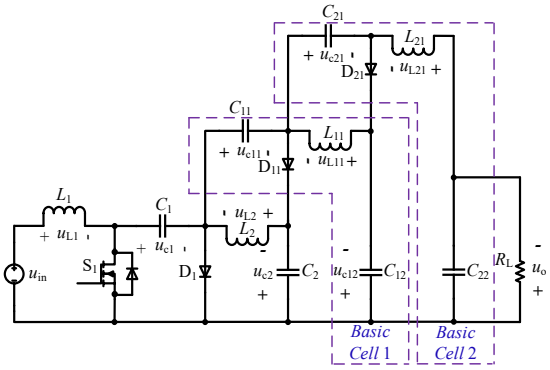


Fig. 2. Topology of the Cuk converter with the coat circuit of two basic cells.

Fig. 2 shows the topology of the Cuk converter with the coat circuit of two basic cells (Cuk-TBC). To simplify, Cuk-TBC has been analyzed in sections II, III and IV as an example. The assumptions for the analysis are given as follows:

1) All components are considered ideal and all effects of parasitic parameters are neglected.

2) The capacitance of all capacitors are larger enough and the influence of capacitor voltage ripple is negligible.

Similar to Cuk converter, there are two modes when Cuk-TBC operates in continuous conduction mode (CCM) as shown in Fig. 3 and Fig. 4 shows the key waveforms of the Cuk-TBC during one switching period. Detailed working process of the converter is presented as follows:

Mode 1[t_0-t_1], Fig. 3(a): Switch S_1 is turned on and all diodes work in the off-state. During this stage, the input voltage source charges the inductor L_1, the capacitor C_1 charges the inductor L_2 and the capacitor C_2, the capacitor C_{11} and C_1 charge the inductor L_{11} and the capacitor C_{12}, the capacitor C_{21}, C_{11} and C_1 charge the inductor L_{21} and the output stage (C_{22}//R_L), and all inductor currents are increased linearly. In this interval, C_2, C_{12} and C_{22} are charged while C_1, C_{11} and C_{21} are discharged.

$$\begin{cases} u_{L1} = u_{in} \\ u_{L2} = u_{C1} - u_{C2} \\ u_{L11} = u_{C1} + u_{C11} - u_{C12} \\ u_{L21} = u_{C1} + u_{C11} + u_{C21} - u_{C22} \end{cases} \tag{1}$$

Mode 2[t_1-t_2], Fig. 3(b): Switch S_1 is turned off. During this stage, all diodes work in the on-state. The inductor current of L_1 branches off through three paths; firstly through C_1, D_1 and u_{in}, secondly through C_1, C_{11}, D_{11}, C_2 and u_{in}, and thirdly through C_1, C_{11}, C_{21}, D_{21}, C_{12} and u_{in}. The inductor current of L_2 flows through D_1 and C_2, the inductor current of L_{11} flows through D_{11}, C_2 and C_{12}, the inductor current of L_{21} flows through D_{21}, C_{12} and the output stage (C_{22}//R_L). In this interval, C_1, C_{11} and C_{21} are charged while C_2, C_{12} and C_{22} are discharged, and all inductor currents are decreased.

$$\begin{cases} u_{L1} = u_{in} - u_{C1} = u_{in} + u_{C2} - u_{C1} - u_{C11} \\ \qquad = u_{in} + u_{C12} - u_{C1} - u_{C11} - u_{C21} \\ u_{L2} = -u_{C2} = -u_{C11} \\ u_{L11} = u_{C2} - u_{C12} = -u_{C21} \\ u_{L21} = u_{C12} - u_o \end{cases} \tag{2}$$

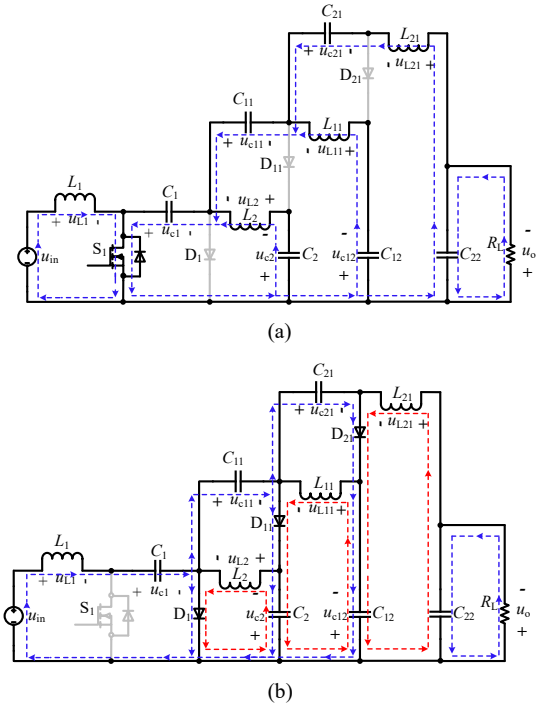


Fig. 3. Equivalent circuits of the two working states.

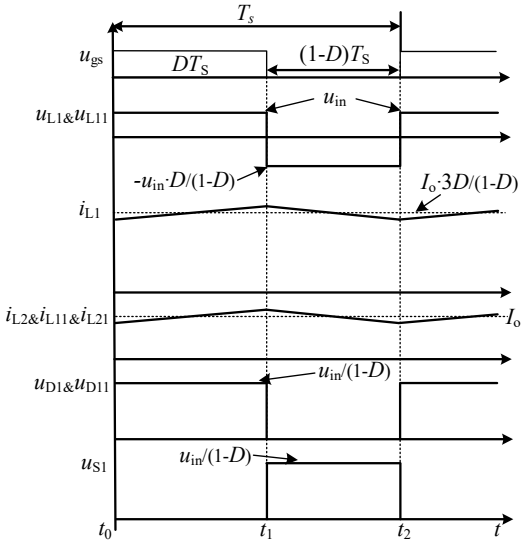


Fig. 4. Key waveforms of the converter during one switching period.

The working principle and analysis process of other converters are similar to the above analysis of Cuk-TBC and as such they are not discussed here.

III. Performance Characteristics

The performance characteristics of Cuk-TBC are illustrated as an example in this section and the characteristics of other converters of Fig. 1 have been summarized in Table I.

A. Voltage conversion ratio

By volt-second balance of the inductor L_1, L_2, L_{11} and L_{21} as given in (1) and (2), the following formulae can be obtained:

$$\begin{cases} u_{C1} = \dfrac{u_{in}}{1-D} \\ u_{C2} = \dfrac{D \cdot u_{in}}{1-D} \\ u_{C11} = u_{C21} = \dfrac{D \cdot u_{in}}{1-D} \\ u_{C12} = \dfrac{2D \cdot u_{in}}{1-D} \\ u_{o} = u_{C22} = \dfrac{3D \cdot u_{in}}{1-D} \end{cases} \tag{3}$$

Based on (3), the voltage conversion ratio (M) can be obtained as follows:

$$M = \frac{u_o}{u_{in}} = \frac{3D}{1-D} \tag{4}$$

Extending the above analysis to a converter with n basic cells:

$$\begin{cases} u_{C1} = \dfrac{u_{in}}{1-D} \\ u_{C2} = u_{C11} = u_{C21} = ... = u_{Cn1} = \dfrac{D \cdot u_{in}}{1-D} \\ u_{Ci2} = \dfrac{(i+1) \cdot D}{1-D} \\ u_{o} = u_{Cn2} = \dfrac{(n+1)D \cdot u_{in}}{1-D} \end{cases} \tag{5}$$

$$M = \frac{u_o}{u_{in}} = \frac{(n+1) \cdot D}{1-D} \tag{6}$$

where $i \in [1, n]$.

B. Voltage and Current Stress of Components

As shown in Fig 2, the voltage stress on switch S_1, diodes D_1, D_{11} and D_{21} can be expressed as u_{S1}, u_{D1}, u_{D11} and u_{D21} respectively. Based on (3), they can be obtained as (7).

Based on (5), extending the voltage stress of diodes of the converter with n basic cells is (8).

$$\begin{cases} u_{S1} = u_{D1} = u_{C1} = \dfrac{u_{in}}{1-D} \\ u_{D11} = u_{C1} + u_{C11} - u_{C2} = \dfrac{u_{in}}{1-D} \\ u_{D21} = u_{C1} + u_{C11} + u_{C21} - u_{C12} = \dfrac{u_{in}}{1-D} \end{cases} \tag{7}$$

$$u_{D11} = u_{D21} = ... = u_{Dn1} = \frac{u_{in}}{1-D} \tag{8}$$

The total voltage stress on diodes of the converter with n basic cells can be calculated as (8), which is the same as the conventional Cuk converter. And the voltage stress on switch of the converter with n basic cells is lower than that of the conventional Cuk converter as given in (7). Therefore, the total voltage stress on semiconductor components with the coat circuit will be lower. However, when all the capacitors and inductors are taken into consideration, the total voltage stress on all components with the coat circuit will be higher.

In order to simplify the current stress analysis, the current ripple of i_{L1}, i_{L2}, i_{L11}, i_{L21} and i_o can be ignored, and their DC values are represented as I_{L1}, I_{L2}, I_{L11}, I_{L21} and I_o respectively. Based on capacitor charge balance requirement of C_{22}, C_{21}, C_{12}, C_{11} and C_2, the average current of diodes D_1, D_{11}, D_{21} and inductors L_2, L_{11} and $L_{21}$are found to be equal to the output average current I_o, which can be expressed as in (9).

$$I_{D1} = I_{D11} = I_{D21} = I_{L2} = I_{L11} = I_{L21} = I_o \tag{9}$$

To simplify the analysis, the efficiency of the converter is assumed to be 100%. Thus, the input average current I_{L1} is

$$I_{L1} = I_o \cdot \frac{3D}{1-D} \tag{10}$$

According to Fig. 3(a), the average and RMS current of switch S_1 can be obtained as (11).

$$\begin{cases} I_{S1} = I_o \cdot \dfrac{3D}{1-D} \\ I_{S1\text{-RMS}} = \sqrt{\left(\dfrac{3I_o}{1-D}\right)^2 \cdot D} \end{cases} \tag{11}$$

When extending the analysis to the converter with n basic cells, equation (12) can be obtained.

$$\begin{cases} I_{D1} = I_{D11} = I_{D21} = ... = I_{Dn1} = I_o \\ I_{L2} = I_{L11} = I_{L21} = ... = I_{Ln1} = I_o \\ I_{L1} = I_{S1} = I_o \cdot \dfrac{(n+1) \cdot D}{1-D} \\ I_{S1\text{-RMS}} = \sqrt{\left(\dfrac{(n+1) \cdot I_o}{1-D}\right)^2 \cdot D} \end{cases} \tag{12}$$

C. Characteristics of DC-DC Converters with and without the Proposed Coat Circuits

The characteristics of basic DC-DC converters with and without coat circuits are shown in Table I. With the number of basic unit n increases, the voltage conversion ratio of basic DC-DC converters is improved and the voltage stress on semiconductor components is decreased. Moreover, no additional switch is needed in coat circuit, which means the control and drive circuit of the converter with the coat circuit is as simple as the corresponding basic DC/DC converter.

TABLE I
COMPARISON OF THE DC-DC CONVERTERS WITH AND WITHOUT THE PROPOSED COAT CIRCUITS.

Topology	Boost converter		Buck-boost converters		Cuk, SEPIC, Zeta converters	
	with coat circuit	without coat circuit	with coat circuit	without coat circuit	with coat circuit	without coat circuit
Number of switches	1	1	1	1	1	1
Number of diodes	$1+n$	1	$1+n$	1	$1+n$	1
Number of inductors	$1+n$	1	$1+n$	1	$2+n$	2
Number of capacitors	$1+n$	1	$1+n$	1	$2+n$	2
Voltage conversion ratio	$\frac{1+n\cdot D}{1-D}$	$\frac{1}{1-D}$	$\frac{(n+1)\cdot D}{1-D}$	$\frac{D}{1-D}$	$\frac{(n+1)\cdot D}{1-D}$	$\frac{D}{1-D}$
Diode and Switch voltage stress	$\frac{u_o}{1+n\cdot D}$	u_o	$\frac{u_o}{(n+1)\cdot D}$	u_o+u_{in}	$\frac{u_o}{(n+1)\cdot D}$	u_o+u_{in}

IV. DISCONTINUOUS CURRENT MODE AND BOUNDARY CONDITION

To simply the analysis process, assuming $L_1 = L_2 = L_{11} = L_{21} = L$, that means peak to peak current ripples of inductor L_1, L_2, L_{11} and L_{21} are equal as shown in (13) and according to (1)-(3).

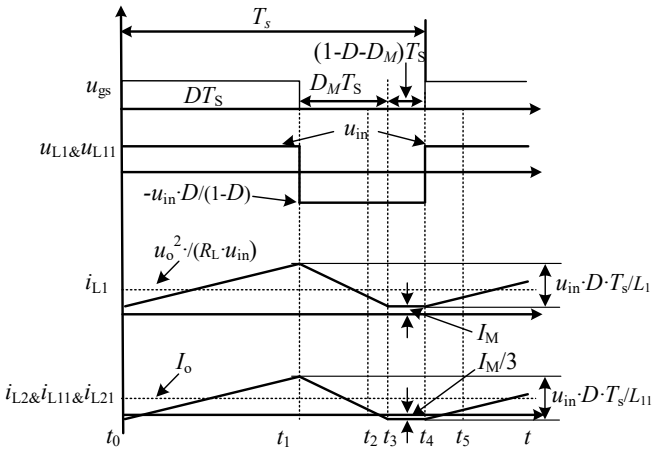


Fig. 5. Key waveforms of the converter working in DCM.

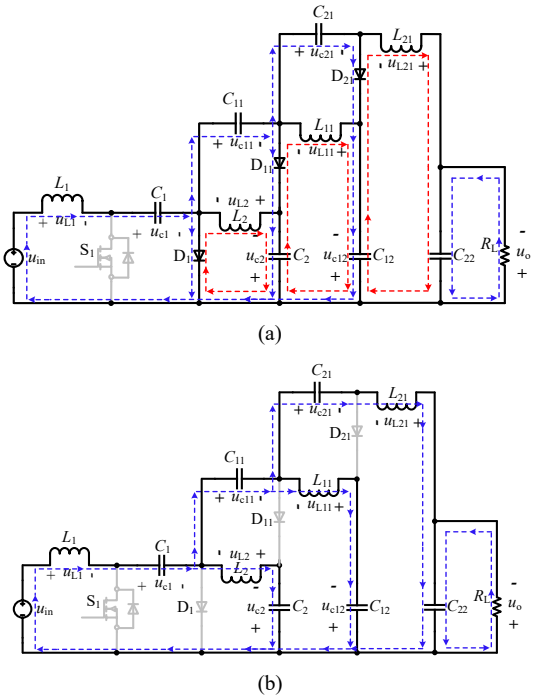


Fig. 6. Equivalent circuits of the DCM.

$$\Delta i_{\mathrm{L1}} = \Delta i_{\mathrm{L2}} = \Delta i_{\mathrm{L11}} = \Delta i_{\mathrm{L21}} = \Delta i_{\mathrm{L}} = \frac{u_{\mathrm{in}} \cdot DT_s}{L} \tag{13}$$

As shown in Fig 5, after the sum of i_{L2}, i_{L11} and i_{L21} decreases to zero at t_2, the current direction of the inductors L_2, L_{11} and L_{21} are reversed as shown in Fig. 6(a). During t_2 to t_3, i_{L1} decreases while i_{L2}, i_{L11} and i_{L21} increase in the negative direction. When the amplitudes of i_{L1} and the sum of currents i_{L2}, i_{L11} and i_{L21} are equal at t_3 which is denoted as I_M, diodes D_1, D_{11} and D_{21} are turned off. During t_3 to t_4, i_{L1}, i_{L2}, i_{L11} and i_{L21} are kept constant, as shown in Fig. 6(b).

By applying the principle of inductor volt-second balance to L_1, L_2, L_{11} and L_{21}, (14) and (15) can be obtained.

$$\begin{cases} u_{\mathrm{C1}} = u_{\mathrm{in}} \cdot \dfrac{D + D_M}{D_M} \\ u_{\mathrm{C11}} = u_{\mathrm{C21}} = u_{\mathrm{C2}} = u_{\mathrm{C1}} \cdot \dfrac{D}{D + D_M} = u_{\mathrm{in}} \cdot \dfrac{D}{D_M} \\ u_{\mathrm{C12}} = u_{\mathrm{in}} \cdot \dfrac{2D}{D_M} \\ u_{\mathrm{o}} = u_{\mathrm{C22}} = u_{\mathrm{in}} \cdot \dfrac{3D}{D_M} \end{cases} \tag{14}$$

$$M = \frac{u_{\mathrm{o}}}{u_{\mathrm{in}}} = \frac{3D}{D_M} \tag{15}$$

The duty cycle D is the control signal of the converter and can be considered known. But D_{M} is unknown, and hence another equation is needed to eliminate D_{M} to obtain the voltage conversion ratio M.

By capacitor charge balance of C_1, C_2, C_{11}, C_{12}, C_{21} and C_{22}, the average current of inductors L_2, L_{11} and L_{21} is equal to the average output current I_{o}. Additionally, according to the balance of input and output power of the converter, (16) can be deduced. Based on Fig. 5, the average current of inductors L_1, L_2, L_{11} and L_{21} can also be calculated as in (17).

$$\begin{cases} I_{\mathrm{L2}} = I_{\mathrm{L11}} = I_{\mathrm{L21}} = I_{\mathrm{o}} = \dfrac{u_{\mathrm{o}}}{R_L} \\ I_{\mathrm{L1}} = \dfrac{{u_{\mathrm{o}}}^2}{R_L \cdot u_{\mathrm{in}}} \end{cases} \tag{16}$$

$$\begin{cases} I_{\mathrm{L2}} = I_{\mathrm{L11}} = I_{\mathrm{L21}} = \dfrac{u_{\mathrm{in}} \cdot DT_s}{2L} \cdot (D + D_M) - \dfrac{I_M}{3} \\ I_{\mathrm{L1}} = \dfrac{u_{\mathrm{in}} \cdot DT_s}{2L} \cdot (D + D_M) + I_M \end{cases} \tag{17}$$

By using (15)-(17), the voltage conversion ratio of the converter in DCM can be obtained as follows:

$$M = \frac{u_{\mathrm{o}}}{u_{\mathrm{in}}} = \sqrt{\frac{2R_L D^2 T_s}{L}} \tag{18}$$

In the boundary condition mode (BCM), the voltage conversion ratio of the CCM is equal to that of the DCM, then from (4) and (18), the boundary factor which is defined as α here, can be obtained by (19). If α is larger than 1, the converter works on DCM and if α is smaller than 1, the converter works on CCM.

$$\alpha = \frac{2(1-D)^2 \cdot T_s \cdot R_L}{9L} \tag{19}$$

Extending the above analysis to a converter with n basic cells, the following equations can be obtained.

$$M = \frac{u_{\mathrm{o}}}{u_{\mathrm{in}}} = \sqrt{\frac{(n+2)R_L D^2 T_s}{2L}} \tag{20}$$

$$\alpha = \frac{(n+2) \cdot (1-D)^2 \cdot T_s \cdot R_L}{2L \cdot (n+1)^2} \tag{21}$$

The characteristics of the boost, buck-boost and other basic DC/DC converters with the proposed coat circuits are summarized in Table II. Expressions for the boundary factor α, as well as for the solutions of the dc conversion ratios in CCM and DCM are given.

TABLE II
SUMMARY OF CCM-DCM CHARACTERISTICS FOR THE BASIC DC-DC CONVERTERS WITH THE PROPOSED COAT CIRCUITS.

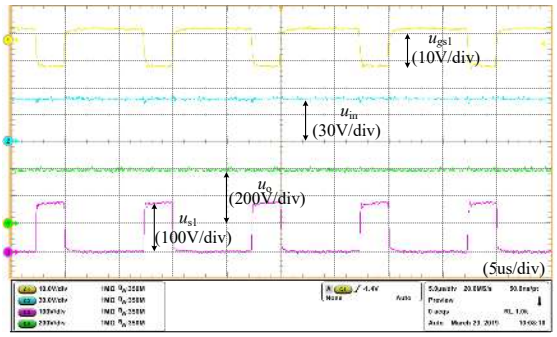
Topology	α (α>1, DCM)	DCM M	CCM M
Boost	$\dfrac{(1-D)^2 \cdot D \cdot T_s \cdot R_L}{2L \cdot (1+n \cdot D)}$	$\dfrac{1+\sqrt{1+\dfrac{2(n+1) \cdot D^2 \cdot T_s \cdot R_L}{L}}}{2}$	$\dfrac{1+n \cdot D}{1-D}$

Buck-boost	$\frac{(1-D)^2 \cdot T_s \cdot R_L}{2L \cdot (n+1)}$	$\sqrt{\frac{(n+1)R_L D^2 T_s}{2L}}$	$\frac{(n+1) \cdot D}{1-D}$
Zeta, Sepic, Cuk	$\frac{(n+2) \cdot (1-D)^2 \cdot T_s \cdot R_L}{2L \cdot (n+1)^2}$	$\sqrt{\frac{(n+2)R_L D^2 T_s}{2L}}$	$\frac{(n+1) \cdot D}{1-D}$

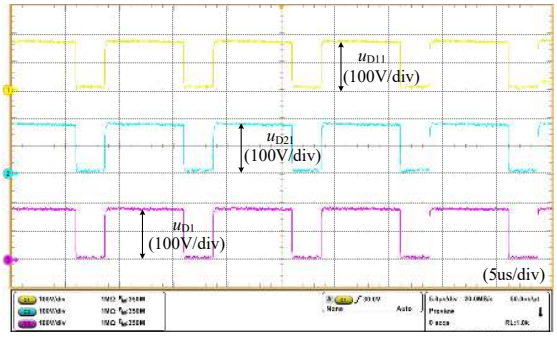
(c)

V. Experimental Results

A 200W Cuk-TBC experimental prototype has been built to verify the accuracy of the above theoretical analysis. The specifications of the prototype are shown in Table III. And the experimental waveforms are shown in Fig. 7.



(a)



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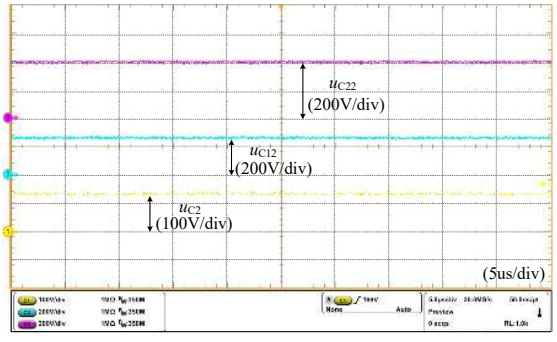
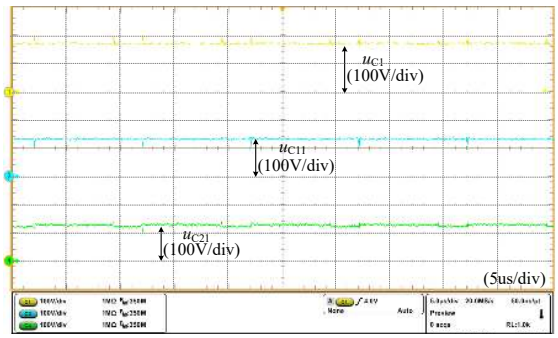
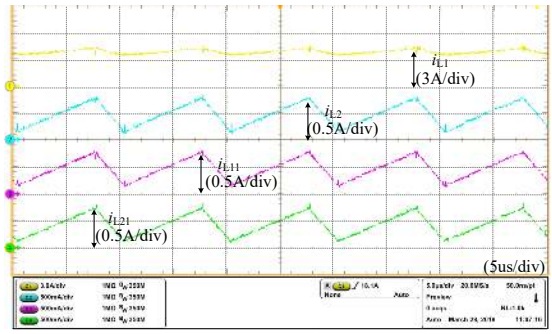
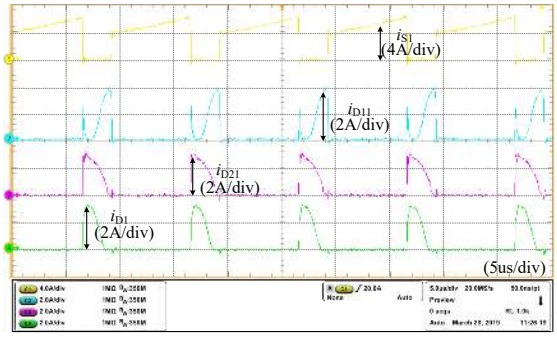




(d)



(e)



(f)

Fig. 7. Experimental waveforms of the prototype when the input voltage is 48V: (a) duty cycle, input voltage, output voltage and Voltage across S_1, (b) Voltage across diodes, (c) and (d) Voltage across capacitors, (e) Inductor currents, (f) diodes and S_1 currents.

Table III
SPECIFICATIONS OF THE EXPERIMENTAL PROTOTYPE.

Parameter	Values
Input voltage (u_{in})	48V
Output voltage (u_o)	24-400V
Output power (P_o)	200W
Switching frequency (f_s)	100kHz
Switch (S_1)	IRFB4332
Diodes (D_1, D_{11}, D_{21})	IDT12S60C
Capacitors(C_1, C_{11}, C_{21}, C_2, C_{12}, C_{22})	5μF
Inductors (L_1, L_2, L_{11}, L_{21})	500μH
Load resistance (R_L)	800Ω

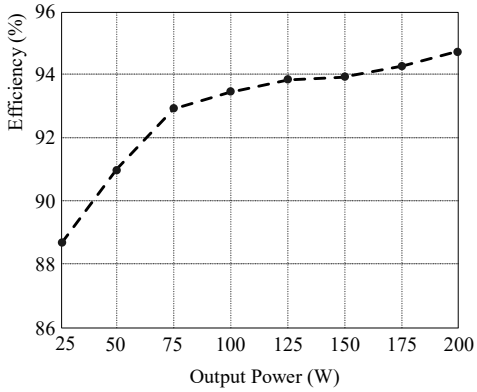
Fig. 7(a) shows the waveforms of u_{gs1}, u_{in}, u_o and u_{s1}, the voltage conversion gain is approximately 8.4 when the duty cycle is near 0.75, which is nearly to (6). Voltage waveforms across D_1, D_{11} and D_{21} are shown in Fig. 7(b), and voltage stress of the above diodes and S_1 is approximately 187V which is consistent with (7). Fig. 7(c) and (d) show the waveforms of u_{c2}, u_{c12}, u_{c22}, u_{c11}, u_{c21} and u_{c1}. The average values of u_{c1}, u_{c12} and u_{c22} are about 185V, 267V and 400V respectively, and the average value of u_{c11}, u_{c21} and u_{c2} is approximately 133V which is consistent with equation (5). Fig. 7(e) shows the current waveforms of L_1, L_2, L_{11} and L_{21}. The DC value of i_{L1} is about 4A, and the DC value of i_{L2}, i_{L11} and i_{L21} is about 0.5A. Fig. 7(f) shows the current waveforms of i_{D1}, i_{D11}, i_{D21} and i_{s1}. The DC value of i_{s1} is about 4A, and the DC value of i_{D1}, i_{D11} and i_{D21} is about 0.5A, which is consistent with equation (12).

Table IV
VOLTAGE STRESSES ON ALL COMPONENTS OF THE EXPERIMENTAL PROTOTYPE.

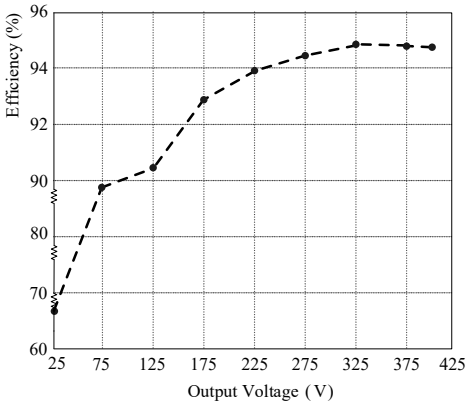
Parameter	Theoretical analysis values (V)	Experimental results (V)
Switch (S_1)	181.1	187
Diodes (D_1, D_{11}, D_{21})	181.1	187
Inductor (L_1)	48 (S_1 on) -133.1 (S_1 off)	48 -135
Inductors (L_2, L_{11}, L_{21})	48 (S_1 on) -133.1 (S_1 off)	50 -135
Capacitor C_1	181.1	186
Capacitors (C_{11}, C_{21}, C_2)	133.1	137
Capacitor C_{12}	266.3	270
Capacitor C_{22}	400	401

Moreover, theoretical analysis and experimental results of the voltage stress on all the components of the prototype are given in Table IV when output voltage is 400V. The experimental results are the maximum voltage on the components of the prototype, due to the influence from capacitor ripple, the actual voltage stress on all the components of the converter will be higher than that under the ideal condition. Generally, the experimental results match well with those obtained from the theoretical analysis.

The efficiency waveform of the converter under different loading condition is shown in Fig. 8(a). When the output power is 200W, the maximum efficiency of the converter is nearly to 94.7%. The efficiency waveform of the converter with different output voltages is plotted in Fig. 8(b). When the output voltage is 325V, the maximum efficiency of the converter is nearly to 95%.



(a)

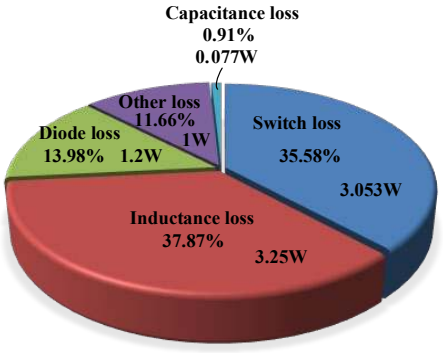


(b)

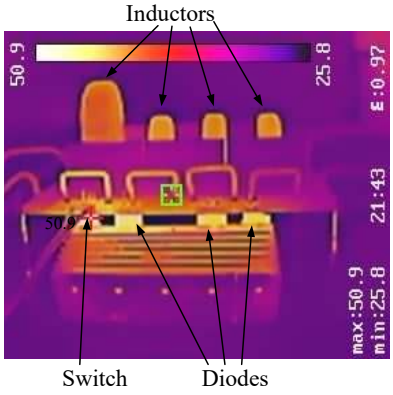
Fig. 8 The efficiency waveforms of the converter: (a) the output voltage is 400V with different load resistance, (b) the load resistance is 800Ω with different output voltage.

The calculated loss distribution of the experimental prototype is shown in Fig. 9(a) when the output voltage is 400V, the main losses are on switch, diodes and inductors, which are nearly to 3.05W, 1.2W and 3.25W, respectively. The thermal image of the prototype is given in Fig. 9(b) under the same working conditions. The ambient temperature is 25.8 ° C, and the maximum temperature of the switch is about 50.9°C. The thermal image has also proved the effectiveness of the

calculation results.



(a)



(b)

Fig. 9 The loss distribution and thermal image of the prototype: (a) loss distribution of the converter, (b) thermal image.

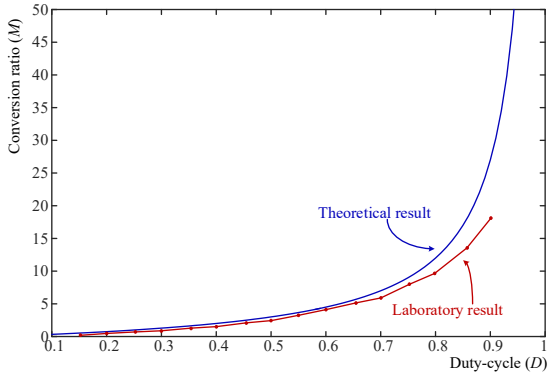


Fig. 10 The conversion ratio M vs duty-cycle (D).

Fig. 10 shows a graph of conversion ratio (M) vs duty cycle (D, 0.1<D<1). The theoretical results are shown in blue while the experiment results are depicted in red. The experiment results are obtained when the input voltage is 10V and the load resister is 800 ohms. Evidently, when the duty cycle smaller than 0.8, the experiment results are close to the theoretical results. It is worth noting that the proposed "coat circuits" can extend the conversion ratio of traditional converter topologies but cannot neutralize the effects of parasitic components on traditional topologies.

VI. Conclusion

A family of coat circuits for basic DC/DC converters to improve voltage conversion ratio have been proposed in this paper. Theoretical analysis and experimental results show that the proposed circuits have the following advantages: (1) No additional active switches are needed, and the control and driver circuit are as simple as those of basic DC/DC converters; (2) Voltage conversion ratio of the DC/DC converters have been improved effectively, and wide range input-output voltage conversion can be realized; (3) The number of basic units in the coat circuits can be optimized to meet the requirements of different applications.

Appendix

The averaged switch model of the basic DC/DC converters with coat circuits can be obtained by using the circuit averaging method proposed in [3]. The averaged switch model of the Cuk-TBC in CCM are presented in Fig A1. The symbol ($\hat{}$) shows the dynamic changes of the parameter as shown in (A1) and (A2). T_p is transformer primary winding, T_{s1}, T_{s2} and T_{s3} are transformer secondary windings (the transformer windings represent the active switch and diode operation in the average switched model).

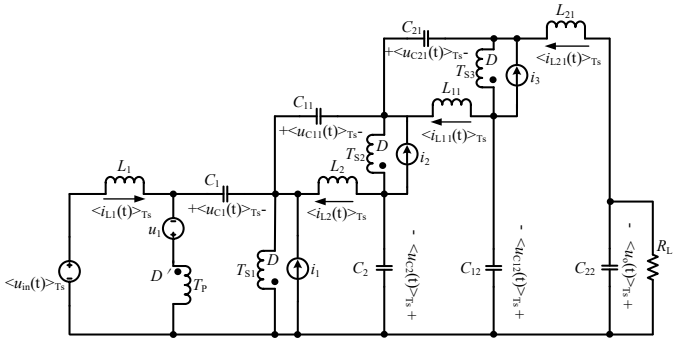


Fig. A1 Averaged switch model of the Cuk-TBC in CCM.

$$\begin{cases} \langle d(t)\rangle_{Ts} = D + \hat{d}(t) \\ \langle u_{in}(t)\rangle_{Ts} = U_{in} + \hat{u}_{in}(t) \\ \langle u_o(t)\rangle_{Ts} = U_o + \hat{u}_o(t) \\ \langle u_{Ci}(t)\rangle_{Ts} = U_{Ci} + \hat{u}_{Ci}(t) \\ \langle i_{Lj}(t)\rangle_{Ts} = I_{Lj} + \hat{i}_{Lj}(t) \end{cases} \quad \text{(A1)}$$

Where i is 1, 2, 11, 12 or 21, and j is 1, 2, 11 or 21.

$$\begin{cases} u_1 = \hat{d}(t) \cdot \dfrac{U_{in}}{D \cdot D'} \\ i_1 = \hat{d}(t) \cdot \dfrac{I_{D1}}{D \cdot D'} \\ i_2 = \hat{d}(t) \cdot \dfrac{I_{D11}}{D \cdot D'} \\ i_3 = \hat{d}(t) \cdot \dfrac{I_{D21}}{D \cdot D'} \end{cases} \tag{A2}$$

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