Combination of rule and pattern based lithography unfriendly pattern detection in OPC flow

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ABSTRACT

Foundry companies encounter again and again the same or similar lithography unfriendly patterns (Hot-spots) in different designs within the same technology node and across different technology nodes, which eluded design rule check (DRC), but detected again and again in OPC verification step. Since Model-based OPC tool applies OPC on whole-chip design basis, individual hot-spot patterns are treated same as the rest of design patterns, regardless of its severity.

We have developed a methodology to detect those frequently appeared hot-spots in pre-OPC design, as well as post OPC designs to separate them from the rest of designs, which provide the opportunity to treat them differently in early OPC flow. The methodology utilizes the combination of rule based and pattern based detection algorithms. Some hot-spot patterns can be detected using rule-based algorithm, which offer the flexibility of detecting similar patterns within pre-defined ranges. However, not all patterns can be detected (or defined) by rules. Thus, a pattern-based approach is developed using defect pattern library concept. The GDS/OASIS format hot-spot patterns can be saved into a defect pattern library. Fast pattern matching algorithm is used to detect hot-spot patterns in a design using the library as a pattern template database. Even though the pattern matching approach lacks the flexibility to detect patterns' similarity, but it has the capability to detect any patterns as long as a template exists. The pattern-matching algorithm can be either exact match or a fuzzy match. The rule based and pattern based hot-spot pattern detection algorithms complement each other and offer both speed and flexibility in hot spot pattern detection in pre-OPC and post-OPC designs.

In this paper, we will demonstrate the methodology in our OPC flow and the benefits of such methodology application in production environment for 90nm designs. After the hot spot pattern detection, examples of special treatment to selected hot spot patterns will be shown.

Key words: Optical proximity correction (OPC), hot spot detection, defect pattern library, pattern matching,

1. INTRODUCTION

Simulation based OPC verification has become standard part of OPC flow since 130nm technology node. One of the best method to prospect mask respin process and to reduce development TAT(turn around time) of process is to carry out OPC verification[1]. At the low-k1 imaging which means lithography extended to the sub-90 nm resolution limited area, the performance of OPC verification is dramatically increased OPC TAT due to OPC rework for solving weak points which are defecting from repeated verification after each OPC. Indeed, we have to analyze how important weak points are to process when each step of verification is done. Why the weak points are detected after OPC verification, the roots causes are classified by OPC model and recipe. If weak points come from OPC model accuracy, it is easy to solve to OPC engineers. Despite of having a good accuracy model, if so-called hot spots break out OPC recipe, we must analyze again the main issue either design error or only OPC recipe issue. In case of process unfriendly design, we couldn't avoid

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several times OPC rework by modifying OPC recipe. Even though over than 10 times, weak points might be still existed. Table 1. shows example of completion of 5 turns OPC in the logic device. From 1st to 5th iteration we had to change OPC recipe and rule many hot spots to reduce and remove. We managed to get a satisfying OPC results in 5 iterations no critical weak points. For 5 turns run time took about 30hr. we could not fix weak points within 2 turns that's because pattern is so complicated and various that we don't know OPC recipe corrected by each of iteration does harm other patterns in the SoC product. Namely weak patterns should be modified through trial and error, which is time-consuming. Most of hot spots were caused by unfriendly design issue. The best solution of hot spot treatment is that when developing circuit, designer considers how to improve process weakness. However, it is hard to come true, because designer has to develop design in aspect of not circuit integration but unit process. None the less we have to modify design before OPC for reducing TAT and improving process margin. Lately, many device companies and engineer are pushing on study of DFM (design for manufacturing).

In this paper, we want to introduce another methodology which can reduce the OPC TAT in the SoC product with the various weak pattern and hot spots. We can detecting weak point original database by using YAM(yield analysis module) and DPL(DFM pattern library) which are able to check and modify hot spots easier than DRC rule before OPC. New OPC flow adds on hot spots searching and fixing procedure. And I will explain how to setup DFM guideline and different experiment results between new method and normal OPC flow.

Table 1. According to iteration of OPC verification defect results

Iteration	Num of defect			Run Time
	Bridge	Break	LE-Short	
1	309608 (Min : +14.2%)	5055 (Min : -17.5%)	1283 (Min : -45nm)	338min
2	160382 (Min : +11.0%)	1826 (Min : -13.2%)	259 (Min : -38nm)	396min
3	2501 (Min : +9.3%)	1094 (Min : -9.8%)	481 (Min : -33nm)	375min
4	266 (Min : +7.0%)	420 (Min : -6.2%)	36 (Min : -27nm)	382min
5	3 (Min : +4.0%)	2 (Min : +3.0%)	25 (Min : -13nm)	374min

2. HOT SPOT SEARCHING AND FIXING

2-1 NEW OPC FLOW

Figure 1 illustrates conventional OPC flow and new OPC flow using YAM. At the normal design flow if we can't detect hot spot area at the layout drawing step, we will find out hot spots after verification step. However design modification after verification step have a bad influence on development TAT[2,3,4]. So, we suggested new OPC methodology considering hot spot management at the early stage of development. In this new OPC flow, YAM running is performed to searching and fixing hot spots before DRC/MDP step. OPC engineers or Designers can find out hot spots in YAM running results, then they can modify layout before OPC running. We are able to improve process margin due to change from unfriendly design to friendly one and to save the OPC TAT using this method. It is easier checking and modifying hot spots than DRC rule.

2-2 HOT SPOTS SEARCHING

YAM which stands for Yield analysis module could be find out litho unfriendly pattern based on rule, while those patterns can not be detected by DRC. Following figure 2 shows the example of YAM analysis. YAM detects specific

given size for weak pattern and mark error boundary. It is good at 2D pattern search by using simple cording rule and easier application than other DFM tool. Additionally, YAM is good performance of speed[5,6].

We used many commands to find out weak points at table 3. Surly, there are available commands for detecting hot spots strongly rely on technology node and manufacturing process. We divided 3 types of hot spots by how to fix them. First, lineend, Triple line and line-end T-juction shape patterns should be change size to solve correct CD target as like line-end pull back. It is hard to fix perfectly because of considering other layer design and they should need to DFM guide. Second, 90 degree bend line and dumbbell pattern need to change design. It is easier than 1st one. But, they are essential process test and thinking about other layers too. Last, jog, nub, notch are able to fix easily with additional layout which can get hot spots map. We can get a modified DB using hot spots map and design change with DFM guide line.

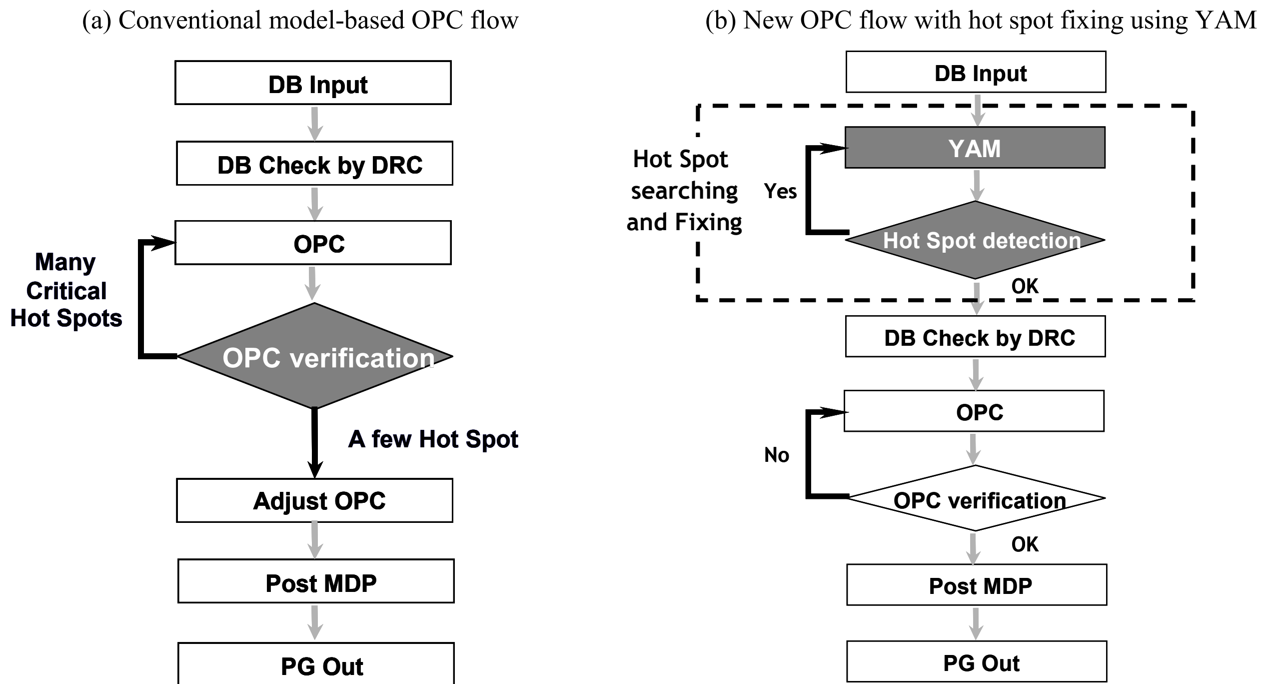


Figure 1. Compare with OPC Process Flow

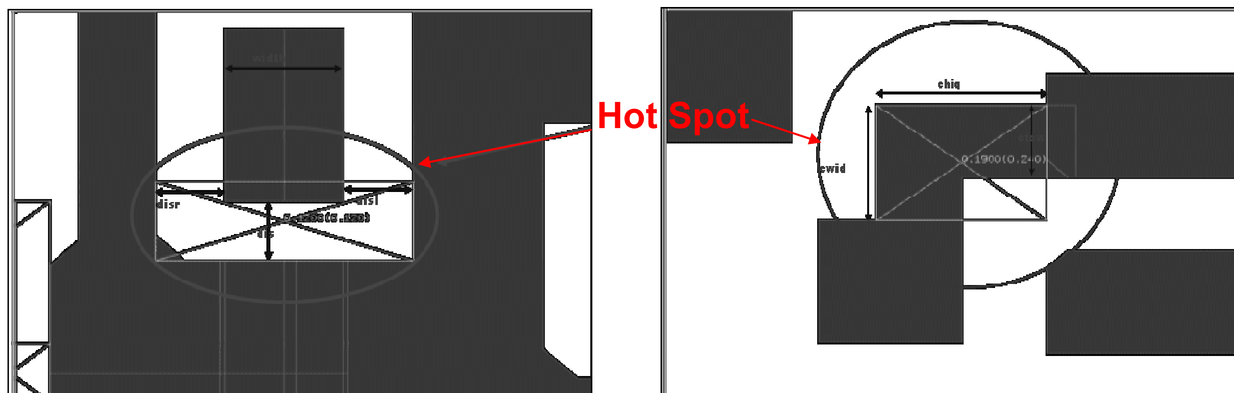


Figure 2. Example of YAM analysis (a): check line end on metal or poly whose length and/or width and/or spacing meet the spec. (b): check small connecting segments (corner crack)

Table 2. Hot spot command (Weight* : Order of importance and difficulty)

Command	Example	Fixing Method	Requirement	Weight*
Line end		Resizing	Test, DFM Guide	7
Triple line		Resizing	Test, DFM Guide	9
Line end T-J		Resizing	Test, DFM Guide	9
90 degree bend		Change design	Test, DFM Guide	8
Parallel bend line		Change design	Test, DFM Guide	10
Dumbbell		Change design	Test, DFM Guide	8
Jog		DB Cut & Add	DB	2
Nub		DB Cut & Add	DB	2
Notch		DB Cut & Add	DB	2

2-3 DESIGN MODIFICATION METHOD

The easiest method of DB modification is jog and notch treatment. Left side flow chart (a) of figure 3 is explaining these procedures. As shown (b), we can make only jog and notch gds from hotspot map. And then, the final gds can be modified by merging two gds between org gds and jog, notch gds. Last, we check design rule check with revised DB. If the revised DB violates DRC, we have to recover to original design. If the result is not violation, we can run OPC with revised DB. Advantage of this method is all type of jogs can to treat without missing points.

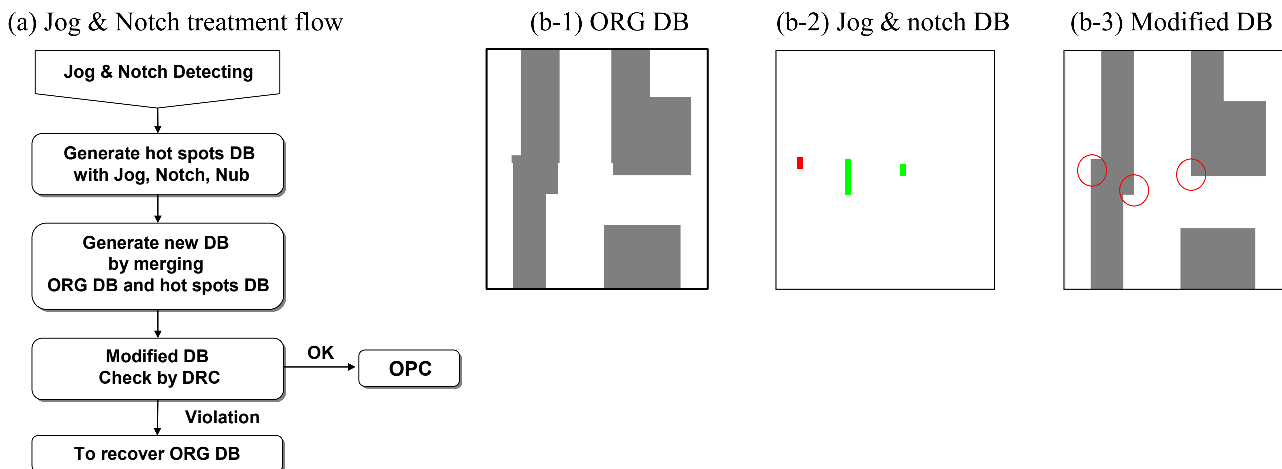
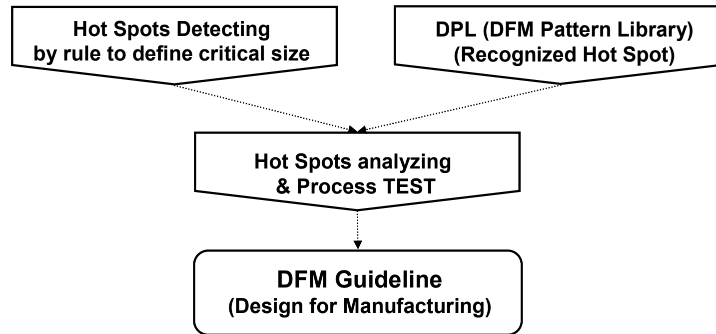


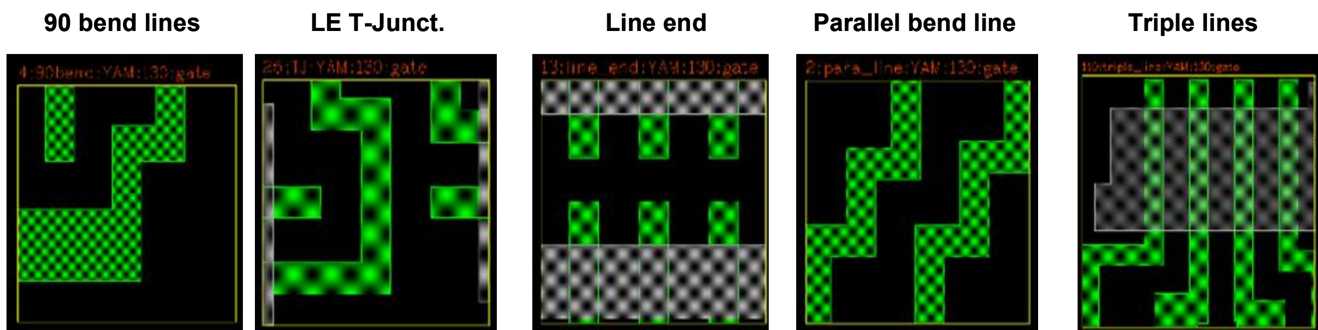
Figure 3. 1st method of DB modification a): Jog & Notch treatment flow, (b-1) ORG DB contained jog and notch, (b-2) Only jog & notch GDS from hot spot map, (b-3) Final modified DB

Second method to revise DB for litho friendly design is fixed hot spots based on DFM guide line. Hot spot detecting is fulfilled combination of YAM command by rule to define critical size and DFM pattern library by recognized known hot spots library. We have about 70 patterns library which are confirmed as hot spots with YAM rules such as triple lines, line end, line end T-junction. % pictures in the below are examples of DPL for poly layer. If the input DB have same pattern, we can find out with DPL without any rule and YAM. Then, we have to execute process test for satisfying size and shape of hot spots. After several test, we can make DFM guideline for considering process margin. So, 2nd DB fixing method is based on DFM guide line. The best method is IP developed engineer keep the DFM guideline when

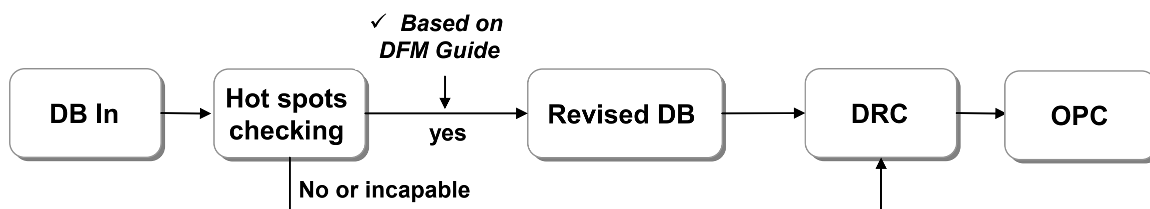
they made IP library. It would be reduce IP development time. Everybody knows that designers are difficult to fully understand about process weakness. Anyway, as decreased tech node, we might observe the DFM guideline for yield and TAT.



(a) Setup flow of DFM guideline



(b) The example of currently built GC DPL Rev.01



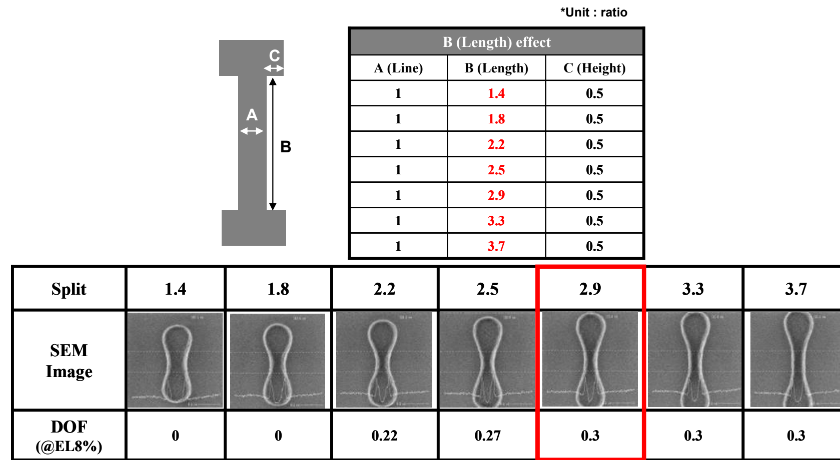
(c) Design verify & develop flow with rule based hot spot searching

Figure 4. 2nd method of DB modification

2-4 EXPERIMENT OF DFM GUIDE LINE

After hot spots searching process with YAM and DPL, we have to setup DFM guideline. Figure 5 is results data what we test for DFM guideline. First, figure 5-a) is dumbbell pattern .The dumbbell is weak pattern of larger than target CD or smaller than target CD by A and B size. So, we did length B split test, and we confirmed at least length of B is about 3times larger than A. In the below SEM images show change of pattern shape and CD trend by change length of B. 2nd example is triple line which always cause concerning about center line CD margin and shape. Although confirmed minimum design rule, in case to min design triple line is very weak pattern. Under the SEM images show change of pattern shape and CD trend by change space of B. So, the space size of B is larger than 1.6 times of width A for process margin. Last example is 90 degree bend line. 90 degree bend line show similar trend as like dumbbell. In the 90 degree

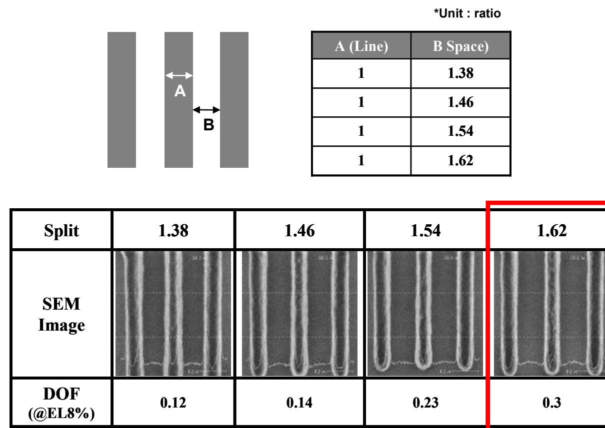
bend line weakness depend on length B which keep suitable length neither too long nor too short. As the wafer test results, like below SEM pictures, length of B would be keep over than 3.5 times of width A.



B (Length) effect		
A (Line)	B (Length)	C (Height)
1	1.4	0.5
1	1.8	0.5
1	2.2	0.5
1	2.5	0.5
1	2.9	0.5
1	3.3	0.5
1	3.7	0.5

Split	1.4	1.8	2.2	2.5	2.9	3.3	3.7
SEM Image							
DOF (@EL8%)	0	0	0.22	0.27	0.3	0.3	0.3

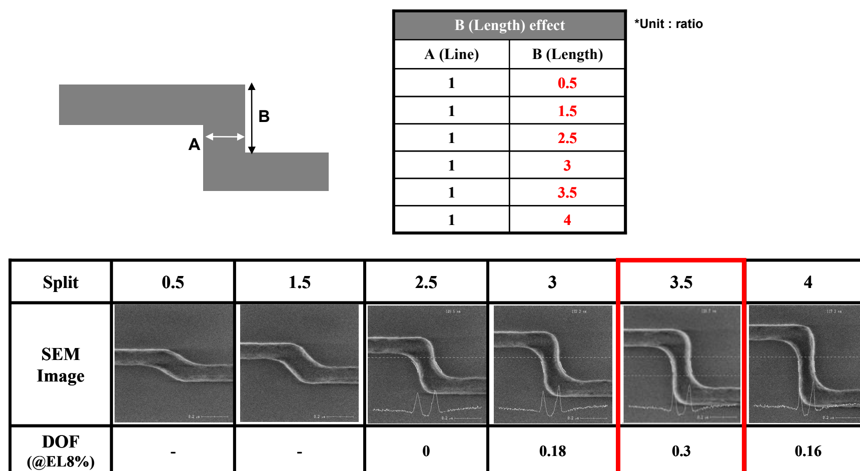
(a) Example of dumbbell pattern



A (Line)	B Space)
1	1.38
1	1.46
1	1.54
1	1.62

Split	1.38	1.46	1.54	1.62
SEM Image				
DOF (@EL8%)	0.12	0.14	0.23	0.3

(b) Example of triple line pattern



B (Length) effect	
A (Line)	B (Length)
1	0.5
1	1.5
1	2.5
1	3
1	3.5
1	4

Split	0.5	1.5	2.5	3	3.5	4
SEM Image						
DOF (@EL8%)	-	-	0	0.18	0.3	0.16

(c) Example of 90 degree bent line

Figure 5. Process test results of hot spots to setup DFM guide line

Figure 6 shows DFM guide line which is tested and confirmed on the wafer should be included in the design rule book. We recommended specific size and shapes for hot spots to improve process margin in the DFM guideline. Our DFM guideline is to be contained more profitable design rule of weak points. As I mentioned, DFM guideline is for designer. When they developed libraries and design, they considered of process limitation in order to reduce developing TAT. Actually, if the designers ignored this guideline, the time of YAM checking and fixing process longer than we expected.

	Description	Priority
1	Length of ⓑ is recommended to be 3 times longer than ⓐ	2
2	Length of ⓒ is recommended to be shorter than ⓐ width	2
3	Length of ⓔ is recommended to be 3.5 times longer than ⓐ	2
4	Space ⓑ between "3 parallel line" is recommended to be 1.6 times larger than ⓐ	2

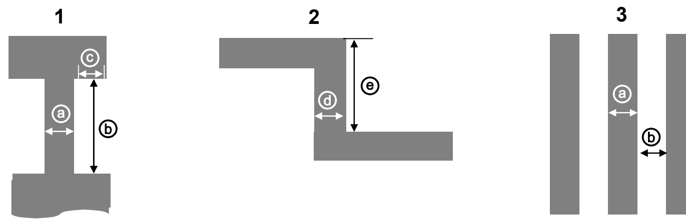


Figure 6. Example of DFM guide line

2-5 EXPERIENCE OF DFM GUIDE LINE

The comparison data of hot spot change between ORG DB and revised DB through the YAM and DPL. As shown the table 3, all commend which we used, the hot spots reduced markedly. We've achieved over 80% reduction in the total hot spots. Especially, jog, nub, notch are improved nearly 100%. Line end is fixed 45% due to active layer design. Finally, we ran OPC with two types DB which are ORG and revised DB. The summary table 4 is explaining OPC verification results and run time. After 4 turns OPC with ORG gds, number of defects are still detected all type of defect like bridge and break. But, Defects of revised DB didn't detect any bridge and break weak points only 1 turn OPC. In case of LE-shortening revised DB is improved. And we got 60% reduction in the total OPC time. Additionally, revised DB applied YAM checking process, hierarchy ratio and data volume are improved too.

Table 3. Hot spot modify rate after New OPC Flow for poly layer

Command	Example	Num. of Hot spots		Fixing Ratio
		ORG DB	Revised DB	
Line end		329	179	45.5%
Triple line		1082	291	73%
Line end T-J		2124	59	97%
90 degree bend		43249	7920	81%
Dumbbell		15363	2972	80%
Jog		36280	846	94.8%
Nub		1630	0	100%
Notch		48282	1019	97.9%

Table 4. Comparison results of OPC with Original gds and revised gds

DB	Num of defect			Run Time	Hier. Ratio	Volume
	Bridge	Break	LE-Short			
ORG DB (4 Turns)	266 (Min : +7.0%)	420 (Min : -6.2%)	36 (Min : -27nm)	382min	2.7	3.7G
Revised DB	0	0	30 (Min : -22nm)	111min	3.6	2.5G

3. CONCLUSION

The attempt to correct various error occurred during OPC performance is not a help to improve OPC TAT. Particularly we repetitive correct OPC recipe to solve error detected after OPC verification in logic device including various pattern shape. Global fragmentation using one factor must have more than three times OPC and verification process. This gives us a negative effect on OPC TAT. The new OPC method using Dynamic Fragmentation detects OPC weak points by using optical parameters in original DB before OPC Run and to handle a specific fragment at weak point. This new OPC method is the best solution to shorten OPC TAT. If we separated the critical and non-critical points from the original database, we can reduce the OPC TAT by applying the high frequency fragmentation at the area of critical points and low frequency fragmentation at the area of non-critical points.

Sub-90nm technology process had more complicated design rules than the previous process technology. Sub-90nm technology lithography causes the situation that hot spots appear frequently. To overcome hot spot issues under low-k_1 lithography condition, the new OPC flow with the YAM running and hot spot fixing flow was developed. The methods and criteria to find the weak points depend on the lithography process and the shape of patterns. The main factor of repeated OPC and verification which is increased TAT depends on pre-OPC DB. To reduce OPC TAT and to achieve process margin, we should consider design change of hot spots before OPC. The hot spots are possible to check and fix output from DPL and YAM either designers or OPC engineers. Advantage of this approach, hot spots fixing on the pre-OPC can be improved remarkably the OPC TAT as well as weak points. Totally, hot spots checking and fixing before OPC should be applied to get a good OPC results. This result is very bright possibility. Therefore, this newly developed OPC flow is going to be very effective for application at 90nm node and beyond.

4. REFERENCE

[1] J.H. Kang et al, "Simulation based post OPC verification to enhance process window, critical failure analysis and Yield", Proc. SPIE Vol. 6154-137 (2006)

[2] T. Kotani et al, "Development of hot spot fixer", Proc. SPIE Vol. 6156-51(2006)

[3] S. Kobayashi et al, "Process window aware layout optimization using hot spot fixing system", Proc. SPIE Vol. 6521-9(2007)

[4] S. Kyoh et al, "Lithography oriented DFM for 65nm and beyond", Proc. SPIE Vol. 6156-14(2006)

[5] Y.Shim et al, "Improvement on OPC completeness through pre-OPC hot spot detection and fix", Proc. SPIE Vol. 6925-37 (2008)

[6] T. Kotani et al, "Yield enhanced layout generation by new design for manufacturing", Proc. SPIE Vol. 5379(2003)

[7] Y. Kim et al, "Application of modified Jog-fill DRC rule on LFD OPC flow", Proc. SPIE Vol. 6730-137 (2007)