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Common DC-Link Capacitor Harmonic Current Minimization for Cascaded Converters by Optimized Phase-Shift Modulation

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Abstract: This paper investigates the influence of a constant carrier phase shift on the DC-link capacitor harmonic current of cascaded converters used in fuel-cell and mild-hybrid electric vehicles. In these applications, a DC-DC converter can be adopted between the battery and the motor drive inverter in a cascaded structure, where the two converters share the same DC-link. Since the DC-link capacitor of such a system represents a critical component, the optimization of the converter operation to limit the current stress and extend the lifetime of the capacitor is an primary objective. This paper proposes the use of a carrier phase shift between the modulations of the two converters in order to minimize the harmonic current of the DC-link capacitor. By harmonic analysis, an optimal carrier phase shift can be derived depending on the converter configuration. Analytical results are presented and validated by hardware-in-the-loop experiments. The findings show that the pulse width modulation carrier phase shift between the interleaved boost converter and the voltage source motor drive inverter has a significant influence on the DC-link capacitor current and thus on its lifetime. A case study with two-cell and three-cell interleaved boost converters shows a possible DC-link capacitor lifetime extension of up to 390%.

Keywords: DC-link capacitor; capacitor harmonic current; harmonic minimization; interleaved boost converter; phase-shift modulation

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Citation: Zhou, X.; Choy, W.J.; Alcaide, A.M.; Wang, S.; Guenter, S.; Leon, J.I.; Monopoli, V.G.; Franquelo, L.G.; Liserre, M.; Galea, M.; et al. Common DC-Link Capacitor Harmonic Current Minimization for Cascaded Converters by Optimized Phase-Shift Modulation. *Energies* **2023**, *16*, 2098. https://doi.org/10.3390/en16052098

Academic Editors: Ralph Kennel and Mohamed Abdelrahem

Received: 7 December 2022
Revised: 25 January 2023
Accepted: 26 January 2023
Published: 21 February 2023

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1. Introduction

The electrification of transportation modes, both passenger and freight, is considered to be one of the key approaches for tackling carbon emissions in order to address the pressing environmental issues [1]. In fuel-cell and mild-hybrid applications, a low-voltage battery typically powers a voltage source inverter that controls the electric machine. In order to optimize the electric drive design, a DC-DC converter can be adopted between the battery and the inverter, and the two converters share the same DC-link. The lifetime of the DC-link capacitor is very important for the reliability of the whole converter system [2–5]. The capacitor lifetime heavily depends on the temperature of the capacitor, which is related to the root-mean-square (RMS) of the DC-link capacitor harmonic current. To reduce the capacitor harmonic current, many related studies have been carried out, aimed at either hardware solutions or modulation strategies.

Many different hardware topologies have been discussed to achieve a current ripple reduction for the DC-link in different areas [6–15]. Owing to the requirement for highly

constrained systems with low volume and low weight, ref. [6] pointed out a generalized method to optimize a DC capacitor tank. In this case, different systems require different DC capacitor tanks, thus the cost could not be ignored. Consequently, adding one more power conversion stage between the battery and the inverter is explored as the highest adoption technique to balance the current energy of the DC-link [7–15]. The method utilizes a back-to-back converter containing a rectifier and an inverter, which could reduce the capacitor harmonic current when the pulsed DC-link current of the rectifier and inverter are synchronized [7]. However, this method only explains the harmonic current could be controlled at an acceptable range. A bidirectional buck-boost converter is operated as a power decoupling stage to handle the harmonic content of the DC-link. This system increases the complexity, and some instability is caused by the difference between the stored and released energy of the decoupling capacitor [8]. In [9], an active power filter is added to a three-phase traction system and the capacitor of the DC-link is decreased from 2200 µF to 100 µF. With the concerns of larger inductor current, high operation frequency, and power loss, this method is hard to use in practical applications. Additionally, for converter systems in fuel-cell applications, a comparative study pointed out that the voltage source inverter (VSI) connected in cascade with a boost converter is the best choice for the transformerless converter when considering the system complexity and power rating with other topologies, such as current source inverter, z-source inverter, and current fed full-bridge converter [10]. Consequently, one conventional boost converter and one VSI are connected to reduce the current ripple of the DC-link capacitor current in [11–13]. In particular, the modulations and power factor are unity in [11] and various power factors are used in [13]. For the harmonic current ratios, it reached 17–20% in [11,12] and 37% in [13], and all values were less than 40%. In addition, according to the performance analysis of interleaved boost converters in [14], the two-cell interleaved boost converter shows a better current ripple reduction than the conventional boost converter. Consequently, interleaved converters have been widely used in electric vehicles (EVs) to extend the power capability of such systems [15]. Therefore, the topology used for the investigation presented in this paper contains one VSI cascaded with two/three-cell interleaved boost converters to achieve a reduced capacitor current.

Despite hardware-based methods, another way to achieve a reduction in capacitor current is via modulation strategies, which are presented in the following. A method to reduce the current ripple is presented in [7]; while the achieved reduction is acceptable, the procedure increases the capacitor stress depending on the output modulation index and power factor. In [16], the authors proposed a special single-phase modulation method that only switches on or off one of the three-phase legs in each PWM-carrier period. The experimental results show that the harmonics distortion is reduced from 4.9% to 4.1%. The carrier can shift the output current pulse of the DC-DC converter to match with the inverter input current, so that the current ripple could be decreased, but the reduction ratio is no more than 20% [11]. An optimal space vector modulation method was studied in [17]. The current ripple reduction of DC-link can be achieved without increasing the switching frequency or inductance, but the ripple factor can only be reduced from 100% to 56.7%. With calculation, the harmonic current reduction is 43.3%. In hybrid electric vehicle (HEV) DC-DC-AC systems, a modified triangle carrier is utilized with a double switching frequency like that of the inverter, and the capacitor current ripple could achieve a 50% reduction rate [18]. Table 1 summarizes some of previous current cancellation methods alongside the harmonic reduction ratio. The proposed method aims to improve the ratio of harmonic reduction. As the adaptive phase shift technology has been widely used for different applications [19–21], this paper proposed the use of a phase shift between the PWM carriers of the cascaded converters.

Table 1. Comparisons of previous harmonic cancellation methods.

Methods	[11]	[12]	[13]	[16]	[17]	[18]
Harmonic reduction ratio	17%	20%	37%	4.9–4.1%	43.3%	50%

If one signal processor is used to control both cascaded converters, it is possible to set a constant carrier phase shift in between the pulse-width modulation (PWM) of two converters. Thus, this paper proposes to set a constant PWM carrier phase shift to minimize the DC-link capacitor harmonic current. A comparison between a two-cell and three-cell interleaved boost converter cascaded with a VSI motor drive is conducted in order to find the optimal PWM carrier phase displacement. Furthermore, due to the interleaved topologies of the boost converter, an optimal switching frequency ratio between the PWMs of the cascaded converters is derived from analytic harmonic analysis. These optimal switching frequency ratios and the PWM carrier phase displacement lead to a minimized DC-link capacitor harmonic current and thus extend its lifetime.

This manuscript is structured as follows. After a brief system description in Section 2, in Section 3 the common capacitor DC-link is analyzed and equations for the DC-link currents are derived. In Section 4 the details of the proposed current harmonic minimization are illustrated. Then, experimental results are given in Section 5 with some extended theoretical analysis of capacitor lifetime. Finally, Section 6 is summarized to explain the main contribution of the proposed method.

2. System Description of the Proposed Cascaded Converter

In Figure 1, the structure of the proposed cascaded converter is shown, which contains a two-cell interleaved DC-DC converter and a VSI connected to a permanent magnet synchronous motor (PMSM). For the DC-AC stage, six insulated gate bipolar transistors (IGBT) switches are used as the top switches (S_a,S_b,S_c) and bottom switches ($\bar{S_a}$,$\bar{S_b}$,$\bar{S_c}$), respectively. Similarly, the DC-DC converter consists of top switches (S_1,S_2) and bottom switches ($\bar{S_1}$,$\bar{S_2}$). Here, $i_{c,dcdc}$ is the DC-link current of the interleaved boost converter and $i_{c,vsi}$ is the VSI demand current. The current through the capacitor is i_c and the relationship can be expressed as Equation (12). In a complex power conversion system such as the one proposed in Figure 1, the capacitor stress of the common DC-link is of crucial importance for the reliability of the whole power conversion system and also affects the overall loss of the system. Thus, these three currents are the key points to investigate. Futhermore, V_d is the input voltage, V_o is the output voltage of the interleaved DC-DC converter, and i_a, i_b, and i_c represent the AC current, which flow out from the VSI. i_1 and i_2 represent the DC-DC inductor current.

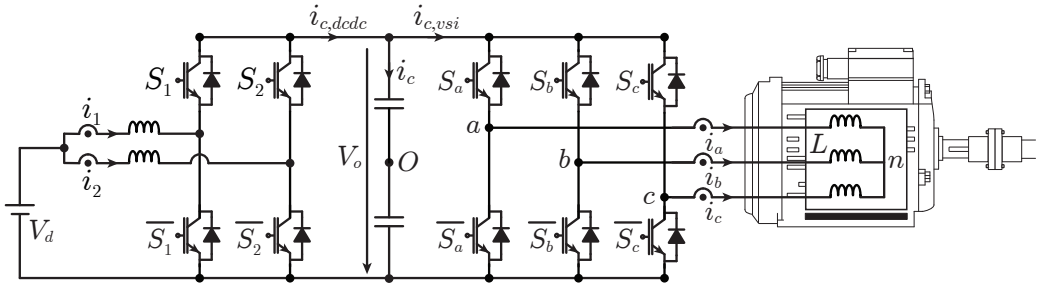

Figure 1. Simplified multi-port converter composed of a two-cell boost converter and a traditional two-level VSI. ©2021 IEEE [22].

Furthermore, Figure 2 displays the relationship between current ripple cancellation factor and the duty cycle variations. The current ripple cancellation factors include the DC-DC converter current $i_{c,dcdc}$ and the inverter demand current $i_{c,vsi}$. The duty cycle depends on the voltage ratio between V_d and V_o, and the optimal harmonic cancellation phase number N of the interleaved converter is obtained. However, for a system containing several converters in a cascaded structure, the influence of the other converters needs to be taken into account in order to find the optimal number of interleaved phases. Moreover, considering the proposed harmonic current reduction method, a certain harmonic current of the DC-DC converter can be beneficial in order to compensate for the harmonic current of the VSI and thus reduce the DC-link capacitor current. Furthermore, depending on the application, the number of parallel connected modules can be varied. Therefore, in the following analysis, the cases with two and three interleaved DC-DC converters will be considered.

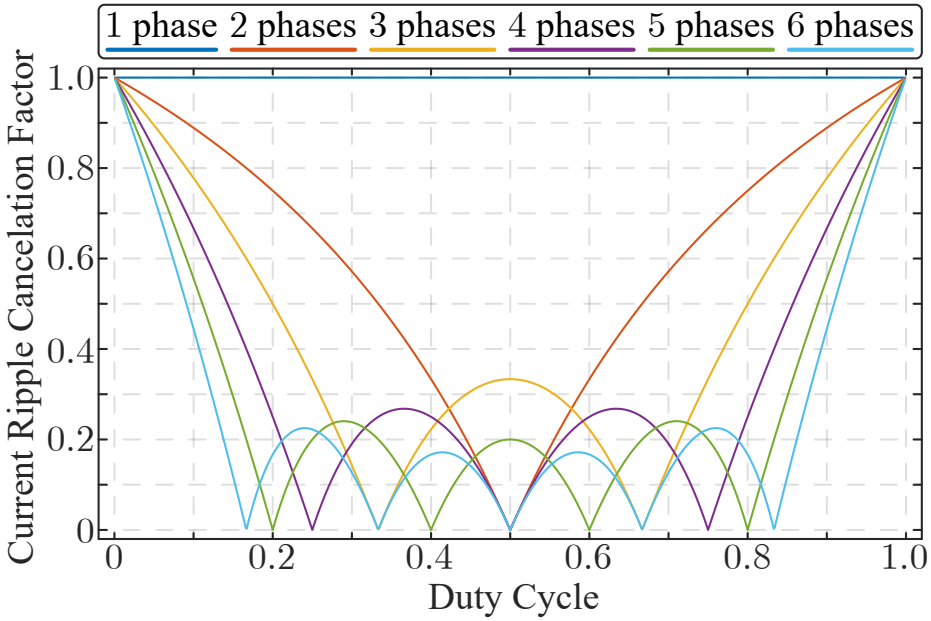

Figure 2. Second terminal capacitor current ripple cancellation factor as a function of duty cycle for a different number of active phases. ©2022 IEEE [23].

3. Analysis of the Common Capacitor DC-Link

The main stressors for the capacitors are represented by the voltage, the temperature, and the humidity [4]. The latter is often ignored under the assumption of proper environmental isolation of the power electronics.

The most common lifetime model for capacitors can be expressed as:

$$L = L_0 \left(\frac{V}{V_0} \right)^{-n} e^{\left(\frac{E_a}{k_B}\right)\left(\frac{1}{T} - \frac{1}{T_0}\right)} \quad (1)$$

where L and L_0 are the lifetime under the operational conditions and testing conditions (usually given by the manufacturer), respectively. The temperatures T and T_0 are defined in the same manner. K_B is the Boltzmann's constant. The activation energy E_a and the exponent n are specific for the capacitor type. For aluminum electrolytic capacitors, n is about 3 to 5 and E_a is 0.94 eV [4]. Since the temperature and voltage represent the main stressors, it is important to estimate the hotspot temperature for the correct design of the DC-link. An overall model of an electrolytic capacitor is reported in Figure 3a, where C represents the main capacitance value, and the other elements represent the temperature-dependent ($R_t = R_{t0} e^{\frac{T_b - T}{SF}}$, with T_b as the base temperature and SF as the temperature sensitivity factor) and frequency-dependent (parallel of R_D and C_D) components of the

equivalent series resistance (ESR). R_0 is the base value. It was highlighted in [24] that for the PWM harmonics (kHz range) the variation of the ESR due to the dielectric loss is minimal, whereas it is important to correctly estimate the temperature, since R_t has a wide range of values (as shown in Figure 3b).

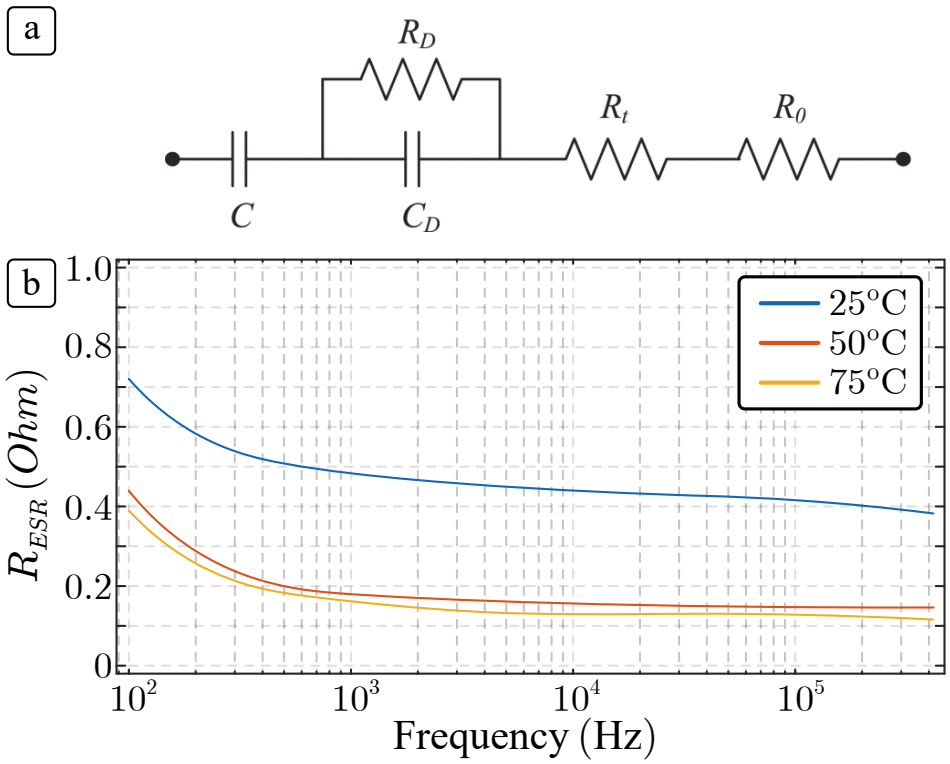

Figure 3. (**a**) Electrolytic capacitor series model. (**b**) Example of the dependence of the ESR parameter in a electrolytic capacitor with frequency and temperature. ©2022 IEEE [23].

The power loss due to the harmonic current components and the ESR represents the heat source, and with the knowledge of the thermal impedance of the capacitor and ambient temperature, the overall hotspot temperature can be determined.

It appears evident that, given the operating point of the electrical machine, the power balance between the two stages must be ensured, meaning that the average values of the input/output current are fixed. The degrees of freedom are represented by the frequencies of the single converters and their relative phase-shift. Other degrees of freedom (i.e., the modulation) are not explored for the sake of simplicity.

3.1. Harmonic Analysis of the Current Injected by Interleaved DC-DC Converters

The influence of the interleaved DC-DC boost converter over the harmonic spectrum of the current absorbed on the DC side of the inverter is studied by the Fourier Series, because it is a uni-dimensional problem [25]. In other words, the duty cycles, which are to be compared with the triangular carriers, do not vary periodically with time in a steady state system. In these terms, this mathematical tool enables the decomposition of any periodic signal to a DC component plus an infinite sum of sines and cosines as

$$\begin{aligned} f(t) &= \frac{a_0}{2} + \sum_{n=1}^{\infty} \Big[a_n \cos(n\omega t) + b_n \sin(n\omega t) \Big] \\ a_n &= \frac{2}{T} \int_0^T f(t) \cos(n\omega t) dt \\ b_n &= \frac{2}{T} \int_0^T f(t) \sin(n\omega t) dt. \end{aligned} \tag{2}$$

where ω is the frequency under study, that is, the carrier frequency of the DC-DC system ($f_{c,dcdc}$) in this case and a_n and b_n are Fourier's coefficients.

In addition, if the DC-DC interleaved converter is composed of several power cells, the resulting output is determined by the summation of the current of each power cell in an independent way. The resulting output current is highly influenced by the phase-angle displacement adopted in the operation of the parallel converter. This influence is determined by

$$\sum_{j=1}^{N} i_j(t) = \sum_{j=1}^{N} \frac{a_{0j}}{2} + \sum_{j=1}^{N} \sum_{n=1}^{\infty} \Big[a_{nj} \cos(n\omega t - n\phi_j) + b_{nk} \sin(n\omega t - n\phi_j) \Big] \tag{3}$$

where ϕ_j is the phase-displacement angle applied to the j-th power cell.

After some mathematical manipulation, each particular harmonic component (n) injected in the common capacitor DC-link shown in (3) can be re-written in a compact form as

$$\begin{aligned} i_{c,dcdc,n}(t) &= \cos(n\omega t) \left[\sum_{j=1}^{N} \frac{a_{nj} - b_{nj} \tan(n\phi_j)}{\sqrt{1 + \tan(n\phi_j)^2}} \right] \\ &+ \sin(n\omega t) \left[\sum_{j=1}^{N} \frac{b_{nj} + a_{nj} \tan(n\phi_j)}{\sqrt{1 + \tan(n\phi_j)^2}} \right] \\ &= C_{1n} \cos(n\omega t) + C_{n2} \sin(n\omega t) = H_n \end{aligned} \tag{4}$$

where it is possible to decompose the magnitude and phase as

$$\begin{aligned} \|H_n\| &= \sqrt{C_{1n}^2 + C_{2n}^2} \\ \angle H_n &= \arctan\left(\frac{C_{2n}}{C_{1n}}\right) \end{aligned} \tag{5}$$

Remark: Note that index n represents a harmonic order, meaning a multiple of the particular carrier frequency.

On the other hand, the coefficient values for a_{nk} and b_{nk} are strictly determined by the specific DC-DC converter topology under study. In the application case of the bidirectional DC-DC interleaved boost converter considered in Figure 1 and also illustrated in Figure 4b, the resulting output current can be defined as

$$i_{ak}(t) = mt + I_L \qquad \text{where} \qquad m = \frac{V_d - V_o}{L} \tag{6}$$

Then, considering (2) and the definitions shown in Figure 4, the coefficients a_n and b_n can be calculated as

$$\begin{aligned} a_n &= \frac{2}{T} \int_{-\frac{(1-D)T}{2}}^{\frac{(1-D)T}{2}} (I_L + mt) \cos(n\omega t) dt \\ &= \frac{2I_L}{n\pi} \sin(n\pi(1-D)) \\ b_n &= \frac{2}{T} \int_{-\frac{(1-D)T}{2}}^{\frac{(1-D)T}{2}} (I_L + mt) \sin(n\omega t) dt \\ &= \frac{mT}{n^2\pi^2} \Big[\sin(n\pi(1-D)) \\ &+ n\pi(1-D) \cos(n\pi(1-D)) \Big] \end{aligned} \tag{7}$$

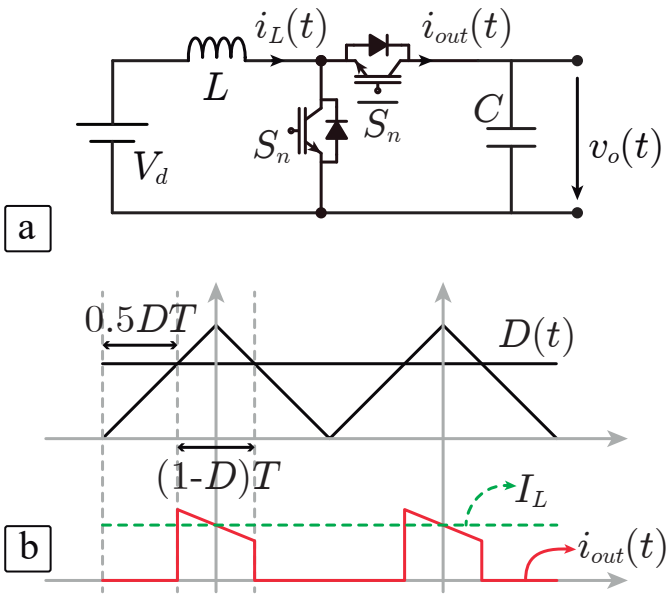

Figure 4. (**a**) Bidirectional DC-DC boost converter topology (**b**) Triangular carrier, modulating signal, and output current (the average value of the inductor current I_L is also represented). ©2022 IEEE [26].

3.2. Harmonic Analysis of the Current Demanded by the Inverter

The influence of the inverter drive connected to the system over the common capacitor DC-link is studied by the double Fourier Transform, since, unlike the DC-DC system, it is a two-dimensional problem because of the variation of the duty cycle during the fundamental period [27]. Considering a conventional two-level voltage source inverter (2L-VSI), as shown in Figure 1 and using the double Fourier Transform, the resulting harmonic spectrum of the current absorbed on the DC side of the inverter is given by

$$\begin{aligned} i_{c,vsi}(t) &= \frac{3}{4} M I_0 \cos(\Phi) \\ &+ \sum_{m=1}^{\infty} \sum_{n=-\infty}^{\infty} \left[A'_{mn} \cos\left(m\omega_c t + n\omega_0 t\right) \right. \\ &\left. + B'_{mn} \sin\left(m\omega_c t + n\omega_0 t\right) \right] \end{aligned} \tag{8}$$

where M is referred to as the modulation index, I_o is the fundamental output current, and Φ is the resulting power factor. Additionally, coefficients A'_{mn} and B'_{mn} are determined by:

$$\begin{aligned} A'_{mn} &= A_{mn}\left[1 + 2\cos\left(n\frac{2}{3}\pi\right)\right] \\ B'_{mn} &= B_{mn}\left[1 + 2\cos\left(n\frac{2}{3}\pi\right)\right] \\ \mu &= \frac{I_0 \cos\left((m+n)\frac{\pi}{2}\right)\cos(\Phi)}{m\pi} \\ A_{mn} &= \mu\left[J_{n+1}\left(m\frac{\pi}{2}M\right) - J_{n-1}\left(m\frac{\pi}{2}M\right)\right] \\ B_{mn} &= \mu\left[J_{n+1}\left(m\frac{\pi}{2}M\right) + J_{n-1}\left(m\frac{\pi}{2}M\right)\right] \end{aligned} \tag{9}$$

where coefficients m, n are referred to as the specific harmonic group (m) and the particular harmonic component inside the group (n). The decomposition in terms of magnitude and phase (denoted as Z_k for convenience) of each particular harmonic component can be performed in a similar way, as carried out in (5).

$$\|Z_k\| = \sqrt{\left(A'_{mn}\right)^2 + \left(B'_{mn}\right)^2}$$
$$\angle Z_k = \arctan\left(\frac{B'_{mn}}{A'_{mn}}\right) \tag{10}$$

Remark: Note that indexes m and n are different from those used in the analysis presented in Section 3.1. Index k is related to the specific harmonic order, which is calculated as

$$k = mR + n \tag{11}$$

where parameter R is referred to as the ratio between the fundamental frequency and the carrier frequency.

From the analysis used in (8), it can be seen that the current demanded by the inverter is decomposed by a DC component plus a sum of carrier harmonic and side-bands harmonic components. These carrier harmonic components are highly influenced by the operational condition of the drive inverter, that is, the magnitude of the coefficients A'_{mn} and B'_{mn} is determined by the fundamental output current, as well as the resulting power factor (i.e., the active and reactive powers).

Additionally, it is also possible to observe that the main harmonic component of the capacitor current is located at the frequency given by $m = 2$ and $n = 0$, as shown in Figure 5 [27,28].

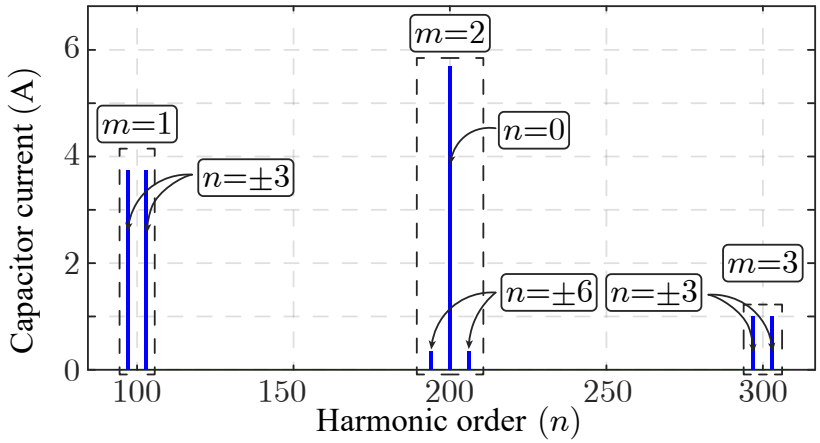

Figure 5. Example of the capacitor current harmonic spectrum decomposition by using the Double Fourier integral. ©2022 IEEE [23].

4. Capacitor Current Harmonic Minimization

The operation of the whole power conversion system is, in general terms, decoupled. As shown in Figure 6, each subsystem is operated by an independent control structure and the time-synchronization between both systems is not strictly required.

On one hand, the conventional control scheme for a DC-DC interleaved converter is shown in Figure 6a. As a result, the energy in the harmonic spectrum of the current injected to the common DC-link is located at N times $f_{c,dcdc}$, considering a completely balanced operation.

On the other hand, the conventional stationary dq-frame control strategy for a motor drive is also shown in Figure 6b. As previously discussed, not only the magnitude and phase of the harmonic spectrum are highly dependent on multiple factors such as the fundamental current magnitude and resulting power factor, but also the location of these harmonic components is dependent on the fundamental output frequency. In general terms, only the harmonic component located at $m = 2$ and $n = 0$ remains in this location during the operation of the inverter, as shown in Figure 5. Fortunately, this harmonic component is the main harmonic component in the demanded current by the inverter drive. In fact, the

frequency of the base-band harmonics normally changes because it is necessary to change the modulating signal frequency to achieve speed regulation.

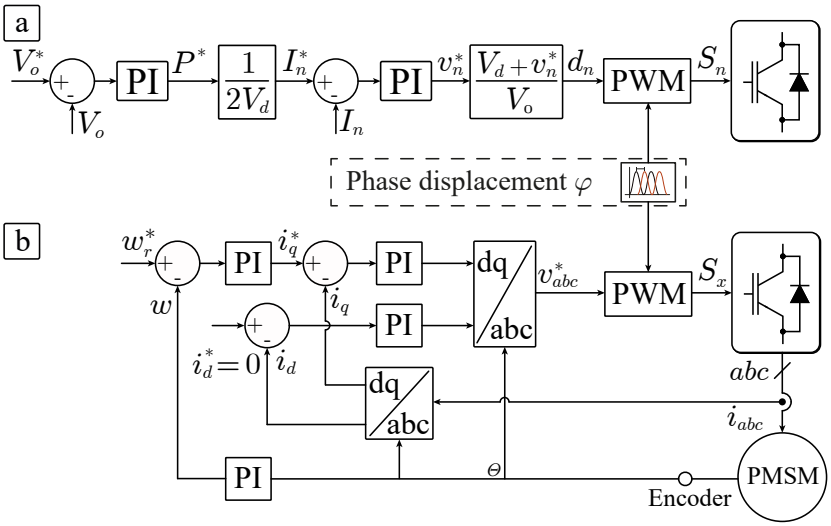

Figure 6. Conventional control structure for (**a**) an interleaved DC-DC boost converter. (**b**) Conventional stationary dq-frame control strategy for a motor drive. ©2021 IEEE [22].

Finally, applying Kirchoff's first law in the common DC-link capacitor, it is possible to obtain the resulting current flowing through the capacitor as

$$i_c(t) = i_{c,dcdc}(t) - i_{c,vsi}(t) \tag{12}$$

Thus, a partial harmonic minimization can be achieved if a specific carrier frequency ratio between subsystems is adopted and an optimum phase-shifting is applied between them. In other words, and considering the system shown in Figure 1, the carrier frequency of both subsystems should fulfill

$$2f_{c,inv} = Nf_{c,dcdc} \tag{13}$$

which ensures that the main harmonic components of both subsystems are located at the same frequency. At the same time, the phase displacement angle between carriers of both subsystems should minimize the resulting $i_c(t)$. That is,

$$\varphi : \min\left(H_n + Z_k\right) \tag{14}$$

where coefficients n and k should be selected according to the appropriated harmonic order.

5. Experimental Results

In order to verify the performance of the proposed method, several sets of experiments have been conducted to highlight the reduction in the capacitor harmonic current. The real-time experiment setup is shown in Figure 7, and an oscilloscope was used for data measurement. The PLEXIM RTBox 3 was connected with the LAUNCHXL-F28069M by an interface PLEXIM board. The prototype was separated into a controller part and a plant part. The controller part is displayed in Figure 6, and the plant part is set up as shown in Figure 1. The DC voltage power supply is 250 V and boosts to 800 V when using the multi-phase interleaved converter. Moreover, with the hardware-in-the-loop technique, the controllers of the two converters can be synchronized. The plant specifications are listed below in Table 2.

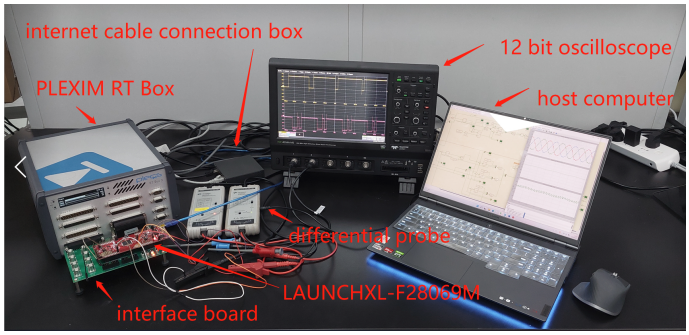

Figure 7. Experimental setup.

To illustrate the effects of the phase displacement, three cases are presented as evaluation scenarios for both two-cell and three-cell interleaved boost converters. As shown in Table 3, the switching frequency of the inverter is 6 kHz and the main harmonic component is located at $m = 2$ and $n = 0$. To consider the balanced operation, the input of the DC-link harmonic spectrum is located at N-times $f_{c,dcdc}$. In case 1 and case 2, the interleaved boost converter and the inverter operate at the same switching frequency at different rotational speeds of the electrical machine. For the three-cell interleaved converter, case 1 and case 2 use 6 kHz and 4 kHz for the inverter and boost converter switching frequency, respectively, to operate at the same harmonic spectrum location. Case 1 and case 3 were tested with the same machine speed and torque, but the two-level inverter had a different switching frequency, which led to a mismatch of the harmonic spectrum. Table 3 summarizes the test cases.

Table 2. Basic data of the laboratory setup.

Parameters	Value
Input voltage V_d	250 V
Inductor	5 mH
Capacitor	2.2 mF
Machine type	IPMSM
Pole pairs	4
Stator resistor R	0.394 Ω
Stator inductance $[L_d, L_q]$	[7.8, 11.5] mH
Flux induced by magnet ψ	0.737 Wb
Power cells	2/3
Inertia J	0.012 Kg/Nms^2

Table 3. Evaluated states to validate the phase displacement effectiveness.

	Test Name	Speed [rpm]	Torque [N/m]	Switching Frequency [kHz]	
				Inverter	Boost
Two- cell boost converter	Case 1	600	200	6	6
	Case 2	500	200	6	6
	Case 3	600	200	6	7.2
Three-cell boost converter	Case 1	600	200	6	4
	Case 2	500	200	6	4
	Case 3	600	200	6	7.2

The DC-link capacitor current i_c (RMS value) is used as a performance indicator when the phase displacement ψ varies from 0° to 180°. The two-cell interleaved converter i_c results are shown in Figure 8 and the three-cell interleaved converter results are shown

in Figure 9. Three different colors are used to express the RMS values of the capacitor current over the displacement angle of three different cases. The optimal point of each case is highlighted with a small black circle.

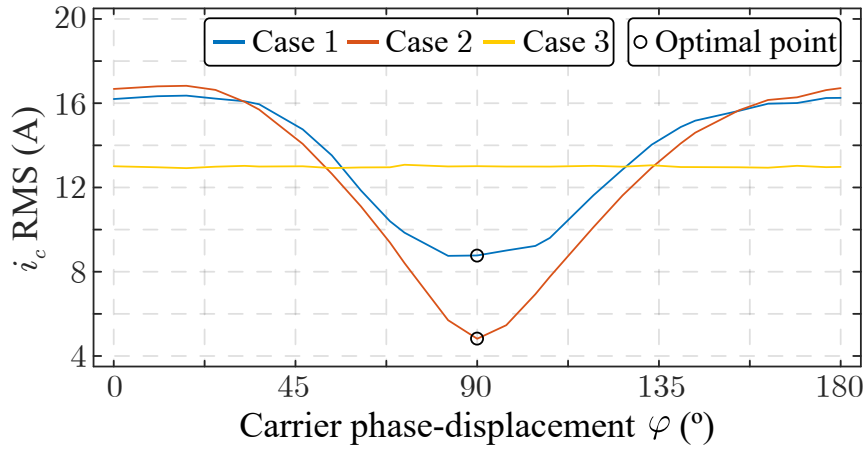

Figure 8. Evaluation of the effective current in the capacitor bank (two-cell interleaved converter) at different operational points.

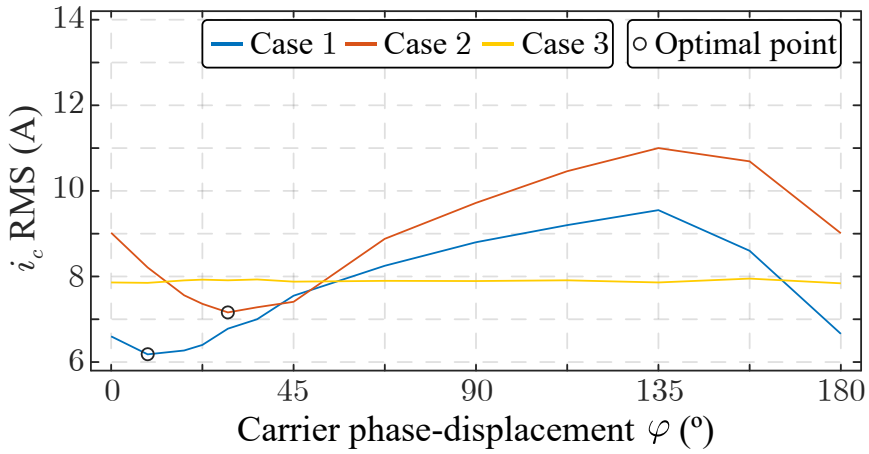

Figure 9. Evaluation of the effective current in the capacitor bank (three-cell interleaved converter) at different operational points.

It is obvious that the phase displacements lead to i_c RMS variations, with the different phase displacements in case 1 and case 3 being shown in the experimental results. Moreover, as the small black circle illustrates, the optimum phase displacement angle for two-cell interleaved converter is 90°, as the maximum effective value reduction can be found at this point. On the contrary, if the switching frequencies are mismatched, as in case 3, the harmonic cancellation does not happen and i_c RMS is maintained at 13 A. Similarly, for the three-cell cascaded converter, case 1 and case 2 show excellent harmonic cancellation by altering the phase displacement angle, but in case 3 the capacitor current remains constant, i_c RMS around 7.9 A, and without any harmonic reduction. To achieve the best harmonic reduction in the three-cell interleaved converter, the optimum phase displacement angle is around 9° (speed = 600 rpm) and 30° (speed = 500 rpm), as illustrated by the optimal point. Additionally, regarding the variation in the i_c RMS value, case 1 and case 2 show a similar trend for both two- and three-cell cascaded converters. The experimental results demonstrate good performance and the possibility of implementing the proposed control with standard real-time microcontrollers.

To observe the effectiveness of harmonic cancellation, Figures 10 and 11 provide the DC-link current spectra for both two-cell and three-cell interleaved converters in their

respective optimal cases and one non-optimal cases. The operation settings of the system are the same as in case 1, where the speed is 600 rpm; thus, the 90° and 9° angles are adopted for the analysis as the optimal point for two- and three-cell cascaded converter, respectively. According to the current curves in Figures 8 and 9, 144° is adopted as the non-optimal point for both two- and three-cell cascaded converter. The current $i_{c,dcdc}$ and $i_{c,vsi}$ are shown, as well as the effective capacitor current. With the FFT analysis results for both two- and three-cell systems, the capacitor harmonic current shows an obvious reduction, as illustrated in Figures 10c and 11c. Additionally, it can be seen that the DC-DC converter and the inverter currents present a balanced DC component and that the main harmonic components are located at 12 kHz for all cases. From the two FFT (Fast Fourier Transform) plots, it can be deduced that due to harmonic cancellation, the overall current component at 12 kHz is reduced. When compared to other cases, the harmonic cancellation presents a good operation at the optimal point. An overall good agreement between the theoretical analysis and experiments can also be seen.

Finally, in order to evaluate the possible impacts on the capacitor lifetime of the proposed phase-shift PWM, Table 4 lists the normalized capacitor lifetime ΔL_c in the different cases and with different assumptions regrading the thermal resistance R_{th}. For the model, an ambient temperature of 25 °C, an R_0 of 35 mΩ, an R_{t0} of 15 mΩ, a sensitivity factor of 20 °C, and a base temperature of 50 °C were adopted. It can be seen that the strong ripple reduction would theoretically allow for an extended lifetime of the DC-link capacitor bank.

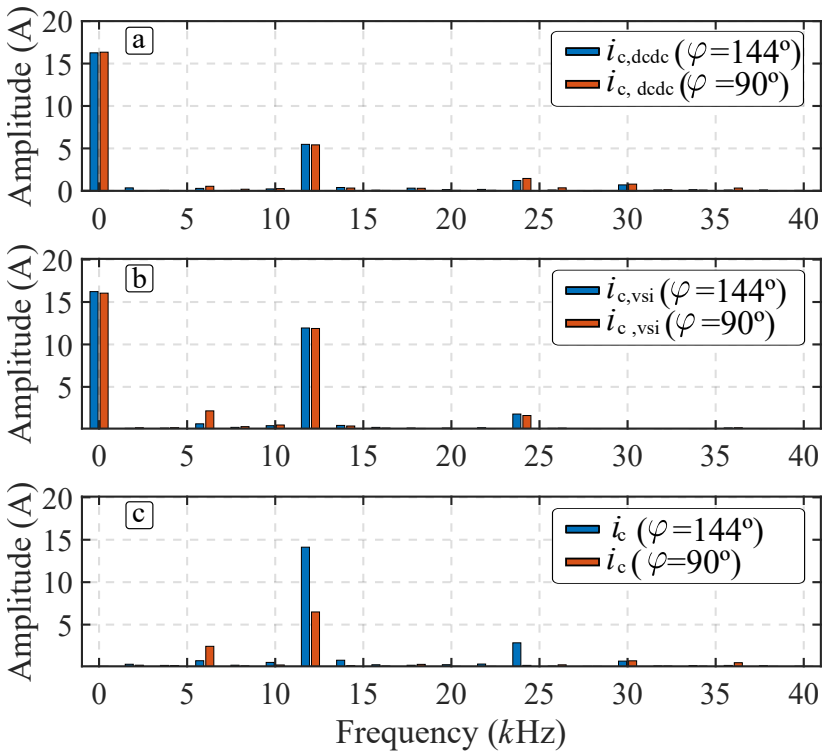

Figure 10. Harmonic spectrum of the currents for a two-cell interleaved boost converter: (**a**) interleaved DC-DC output current, (**b**) inverter demanded current, (**c**) capacitor current.

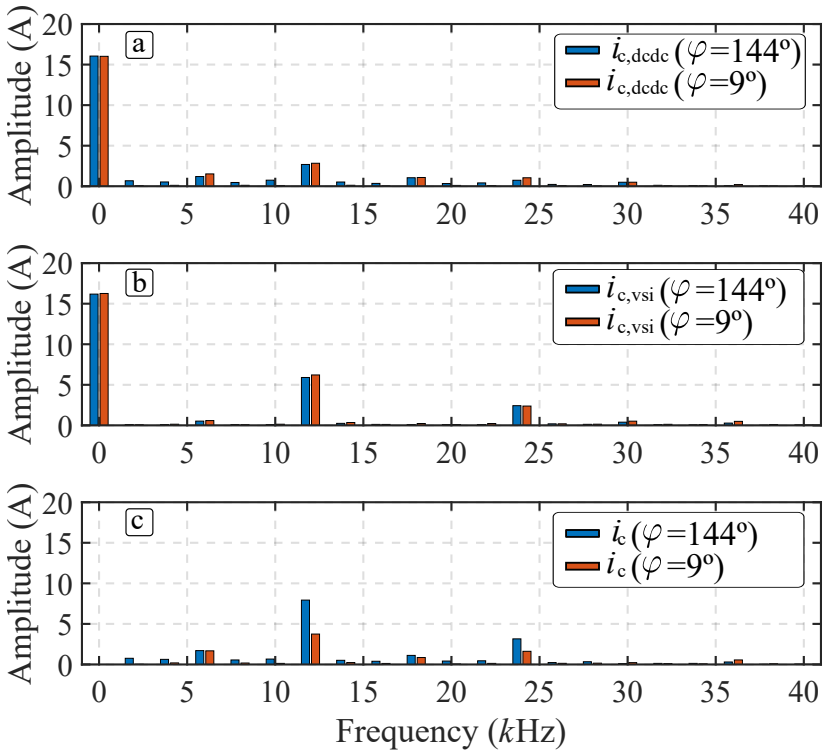

Figure 11. Harmonic spectrum of the currents for a three-cell interleaved boost converter: (**a**) interleaved DC-DC output current, (**b**) inverter demanded current, (**c**) capacitor current.

Table 4. Evaluation of the capacitor hotspot temperature and the corresponding capacitor lifespan extension.

Topology	Case	I_c RMS	R_{th} = 2 K/W		R_{th} = 5 K/W	
		(A)	T_h (°C)	ΔL_c	T_h (°C)	ΔL_c
2-cells	1	9.31	36.2	3.1	47.5	4.9
dc-dc	3	13.4	44.6	1.0	63.3	1.0
3-cells	1	6.44	31.1	1.7	37.9	2.6
dc-dc	3	9.05	35.7	1.0	46.6	1.0

6. Conclusions

This work proposes a capacitor harmonic current reduction algorithm for voltage source inverters cascaded to interleaved DC-DC converters. The core of the method is the optimal phase shift between the PWM carriers of the individual converters composing the system. Theoretical analysis and hardware-in-the-loop verification are adopted to highlight how the optimal phase shift angle changes depending on the number of interleaved cells composing the DC-DC converter. Maximum reduction of 70% (for the 2-interleaved case) and 27% (for the 3-interleaved case) are achieved in terms of capacitor current ripple. A theoretical analysis of the possible lifetime extension of the capacitor shows a significant increase when the proposed method is adopted. Furthermore, the 70% harmonic current reduction shows a higher cancellation ratio in comparison with other methods. Therefore, the capacitor lifetime is extended by more than 390%.

Author Contributions: Methodology, W.J.C. and A.M.A.; Software, X.Z. and S.G.; Formal analysis, A.M.A.; Investigation, X.Z.; Writing—original draft, X.Z., A.M.A. and G.B.; Writing—review & editing, W.J.C., S.W., S.G. and G.B.; Supervision, S.G., J.I.L., V.G.M., L.G.F., M.L., M.G., C.G. and G.B. All authors have read and agreed to the published version of the manuscript.

Funding: The authors gratefully acknowledge financial support provided Ministerio de Ciencia e Innovación under the project PID2020-115561RB-C31, Junta de Andalucía under the project P18-RT-1340. Abraham M. Alcaide gratefully acknowledges the financial support provided by Contratacion de Personal Investigador Doctor. (Convocatoria 2019) 43 Contratos Capital Humano Línea 2. Paidi 2020, supported by the European Social Fund and Junta de Andalucía. Additionally, this work is supported by Natural Science Foundation of China with project code 52250610219 and by the Ministry of Science & Technology under National Key R&D Program of China, under Grant 2021YFE0108600.

Data Availability Statement: All the information is in this work.

Conflicts of Interest: The authors declare no conflict of interest.

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