Common-Mode Voltage Mitigation Strategies Using Sigma-Delta Modulation in Five-Phase VSIs

Fernando Acosta-Cambranis, *Student Member, IEEE,* Jordi Zaragoza, *Member, IEEE,* Néstor Berbel, *Member, IEEE,* Gabriel J. Capella, and Luis Romeral, *Member, IEEE*

***Abstract*—Various sigma-delta ($\Sigma\Delta$) modulation techniques for reducing the maximum peak-to-peak amplitude of common-mode voltage (CMV) by 80% in a five-phase, high-frequency voltage source inverter (VSI) are proposed and evaluated in this paper. These techniques are based on choosing a set of vectors that limits the CMV amplitude. Operating the VSI under high-frequency pulse width modulations (PWM) generates a large number of changes in the CMV levels, which leads to common-mode currents (CMCs) and conducted electromagnetic interferences (EMIs). The proposed modulation techniques achieve the following: 1) high-efficiency converter operation and output voltage with low THD; 2) an 80% reduction in CMV peak-to-peak amplitude; 3) a decrease in the number of the CMV transitions, thus reducing the CMCs; and 4) a decrease in the conducted EMI amplitude. The use of single-loop and double-loop $\Sigma\Delta$ modulators are analyzed by means of Matlab/Simulink and PLECS simulations. The implementation of the proposed modulation techniques has been experimentally evaluated using a five-phase VSI with silicon carbide (SiC) semiconductors. In order to demonstrate the improved performance, the results obtained are compared with those of other PWM and space vector modulation (SVM) techniques that also mitigate the CMV amplitude by 80% but lack the other improvements.**

***Index Terms*—Common-mode Voltage, Five-phase VSI, Power Losses, Sigma-Delta Modulation, Total Harmonic Distortion, Conducted EMIs.**

I. Introduction

THESE days, wide-bandgap (WBG) devices, like those based on silicon carbide (SiC) and gallium nitride (GaN) have become attractive in the design of power converters because they can operate at high voltage levels, high temperatures, and high frequencies. Therefore, power converters with high efficiency, fast dynamic response, and high-power density can be designed [1], [2]. However, operating at high frequencies can lead to electromagnetic interference (EMI) [3].

Common-mode voltage (CMV) is one of the issues that are affected by high switching frequencies. Using pulse width modulation (PWM) and space vector modulation (SVM) techniques at high switching frequencies generates a large number of CMV transitions [4], [5]. In motors, high-frequency CMV changes cause insulation damage, bearing currents, shaft voltages, and mechanical vibrations [6], [7]. In applications where the resonant frequency is relevant (such as in photovoltaic systems, due to their large capacitance), the high-frequency CMV content can lead to common-mode currents (CMC). These CMCs can generate EMI issues, extra power losses, and distortion of voltages and currents [8], [9].

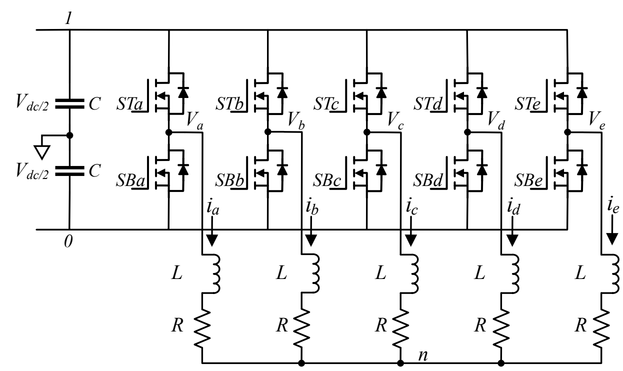


Fig. 1: Five-phase voltage source converter.

Several methods exist for reducing or eliminating CMV, such as the use of filters [10], advanced converter topologies [11]–[13], or specific modulation techniques [11], [14]–[16]. The latter method allows for a reduction or elimination of CMV without the need of output filters or advanced converter topologies, thus avoiding the additional cost of the components, designing, and manufacturing.

Multiphase electrical systems are gaining attention for high-power industrial applications, renewable energy generation, propulsion, and electric traction [17], [18]. Some of the advantages that multiphase systems have over traditional three-phase electrical systems are lower current per phase, more degrees of freedom, higher reliability, and better fault tolerance [19], [20]. Fig. 1 shows the structure of a five-phase voltage source inverter (VSI) based on SiC devices.

In two-level converters, increasing the number of converter phases increases the number of CMV levels and transitions. In a three-phase VSI, there can be up to four CMV levels and up to six possible transitions among them, whereas in a five-phase VSI, there can be up to six CMV levels and up to ten transitions. However, depending on which modulation technique is implemented, it is possible to reduce or eliminate the number of CMV levels and their transitions. In [21], the authors analyze the CMV waveforms generated by standard modulation techniques for a five-phase VSI. According to the applied switching sequence, the amplitude and number of CMV levels and transitions will vary. Besides, the use of discontinuous versions of the standard modulation techniques

F. Acosta-Cambranis and L. Romeral are with the Motion Control and Industrial Applications (MCIA) research group, Department of Electronic Engineering, Universitat Politècnica de Catalunya (UPC), 08222 Terrassa, Spain.

J. Zaragoza, N. Berbel and Gabriel J.Capella are with the Terrassa Industrial Electronics Group (TIEG), Department of Electronic Engineering, Universitat Politècnica de Catalunya (UPC), 08222 Terrassa, Spain.

reduce the number of CMV transitions and the CMV amplitude between 20% and 40%.

The active zero-state PWM (AZSPWM) modulation technique that was introduced in [22] implements a switching sequence that exchanges zero vectors for large vectors, thereby achieving an 80% reduction in the CMV peak-to-peak amplitude. In [23], the same performance is obtained by implementing their second carrier-based CMV reduction modulation technique (RCMV-CBM2), which uses two carrier signals to generate the switching sequence. Also, in [24], an improved predictive model of current control (IMPCC) is implemented in conjunction with the use of virtual voltage vectors (V^3). The technique, called IMPCC2, uses a symmetrical switching pattern to also decrease the peak-to-peak amplitude of the CMV by 80%. Although the three modulation techniques mentioned above, succeed in reducing the CMV, their THD is worse than a standard five-phase modulation technique. In addition, the number of CMV transitions is not reduced.

In [24], the authors propose the IMPCC1 technique, which uses an asymmetric switching pattern to decrease the CMV amplitude and reduce the number of CMV transitions. PWM techniques based on sawtooth carriers 1 and 2 (SCPWM-1 and SCPWM-2, respectively) are proposed in [25]. These techniques achieve the same performance as in [24], by using sawtooth carrier signals with inverse slopes. In [26], a modulation technique called CMVR-3 is proposed for reducing the CMV. This technique implements a scalar approach using two carriers with opposite phases and a modified zero sequence injection, thus achieving an operation that performs similarly to a space vector modulation technique based on five large vectors. The switching sequence achieves a lower number of CMV transitions. However, this performance is possible only for modulation indices (m) greater than 0.882. The work in [24]–[26] achieve an 80% decrease in CMV and reduce the number of CMV transitions by reducing switching operations. However, their THD is worse compared to that of a standard modulation technique.

It is also possible to eliminate the CMV transitions and generate a constant or 0 V CMV. This performance has been achieved by using five-phase three-level converters [27], [28] and control techniques that require feedback [29].

The work presented here proposes modulation strategies based on sigma-delta ($\Sigma\Delta$) modulations to achieve: 80% reduction in the CMV peak-to-peak amplitude; reduced number of CMV transitions; low-THD output voltage; and high-efficiency operation of the converter compared to convetional modulation techniques [21].

Low EMI's have been achieved in power converters by implementing $\Sigma\Delta$ modulation [30], [31], which is recommended for high sampling frequencies. Using low sampling frequencies will affect the modulation resolution, thus increasing the modulator error and producing an output signal with low-order harmonics [32]. Another method for improving the system resolution is to increase the number of integrator loops. However, adding integrators could destabilize the system [33], [34].

In [35], the authors discuss applying hexagonal $\Sigma\Delta$ modulation to a three-phase converter and demonstrate that using this technique at high switching frequencies together with a double-loop $\Sigma\Delta$ modulator mitigates the amplitude of low-order harmonics, while confirming high-efficiency operation of the converter.

The performance of $\Sigma\Delta$ modulation in a three-phase multilevel converter is shown in [36], [37]. A reduction of the switching losses is observed, due to a decrease in the number of switching operations. In addition, $\Sigma\Delta$ modulation spreads the harmonic content over the frequency spectrum, which in turn decreases the amplitude of high-frequency components.

In [38], two modulation techniques based on $\Sigma\Delta$ modulators are proposed for a five-phase VSI. These techniques combined the use of $\Sigma\Delta$ modulators with the nearest vector algorithm to choose the vector to be applied during each sampling period. The converter operates at high efficiency and low THD when implementing the double-loop five-phase all-vector $\Sigma\Delta$ (DL-5P-AV-$\Sigma\Delta$) modulation technique. In addition, the number of CMV transitions during a switching period is reduced, which decreases the amplitude of conducted EMIs. The performance is significantly better than that of the two-large and two-medium SVM (2L+2M SVM) modulation technique.

Applying $\Sigma\Delta$ modulation to five-phase converters in order to reduce CMV effects has not been addressed yet. In this work, the use of $\Sigma\Delta$ modulation in order to generate modulation strategies that reduce both the CMV amplitude and its number of level changes is proposed. All the modulation strategies are applied to a five-phase converter based on SiC devices, as shown in Fig. 1. Six $\Sigma\Delta$ common-mode voltage reduction ($\Sigma\Delta$-CMVR) modulation strategies are proposed and studied. These strategies are named $\Sigma\Delta$-CMVR1, $\Sigma\Delta$-CMVR2, $\Sigma\Delta$-CMVR3, $\Sigma\Delta$-CMVR4, $\Sigma\Delta$-CMVR5 and $\Sigma\Delta$-CMVR6. Each modulation strategy is based on the use of $\Sigma\Delta$ modulators in conjunction with the nearest vector algorithm and the choice of a specific set of vectors (switching states) that meet the necessary criteria to obtain the desired CMV waveform. In [38], the reduction of the number of level transitions is also achieved. However, the size of these level transitions is variable due to the use of all the voltage vectors, whereas in the proposed modulation strategies, all the level transitions are equal and they are limited to a value of $0.2V_{dc}$, thus achieving an 80% reduction in the maximum CMV peak-to-peak amplitude. These two features allow for improving the performance of the proposed modulation strategies in terms of conducted EMI and CMC. Despite the reduction in the number of voltage vectors used, high converter efficiency and low output voltage THD are achieved. To summarize, the proposed modulation strategies allow:

- Output voltage with low THD.
- High efficiency converter operation.
- An 80% decrease in CMV peak-to-peak amplitude.
- A reduction in CMV transitions, thereby reducing the CMCs.
- A restriction in the CMV level transition amplitude ($0.2V_{dc}$).
- A decrease in the conducted EMI amplitude.

Simulation results were used to analyze the average number of switching operations per switch by means of single-loop and double-loop ΣΔ modulators. The experimental results were used to analyze the converter's THD, efficiency, CMV waveform, CMCs, and conducted EMI performance and, then, compared with those of the AZSPWM [22], the SCPWM-2 [25], and the RCMV-CB2 [23].

The rest of this paper is organized as follows. Section II introduces the basis of the decision algorithm and describes the set of chosen vectors in each one of the modulation strategies. Section III presents the simulation and experimental results obtained from a five-phase VSI. Finally, Section IV summarizes the conclusion of this paper.

II. Five-phase ΣΔ common-mode voltage reduction modulations

Like SVM techniques, three-phase ΣΔ modulation techniques operate in α-β space [34], [35]. In the case of five-phase SVM, they operate in two 2-D subspaces: α-β and x-y. These subspaces can be obtained by applying Clarke's transformation (1).

$$C_{T5} = \frac{2}{5}\begin{bmatrix} 1 & \cos(\varphi) & \cos(2\varphi) & \cos(3\varphi) & \cos(4\varphi) \\ 0 & \sin(\varphi) & \sin(2\varphi) & \sin(3\varphi) & \sin(4\varphi) \\ 1 & \cos(3\varphi) & \cos(\varphi) & \cos(4\varphi) & \cos(2\varphi) \\ 0 & \sin(3\varphi) & \sin(\varphi) & \sin(4\varphi) & \sin(2\varphi) \\ 1/2 & 1/2 & 1/2 & 1/2 & 1/2 \end{bmatrix} \quad (1)$$

where $\varphi = 2\pi/5$.

Fig. 2 shows the α-β and x-y subspaces. Both subspaces comprise 32 vectors (switching states), which are divided into 10 large, 10 medium, 10 small, and 2 zero vectors. The α-β subspace contains the harmonics on the order of $10k \pm 1$ $(k = 0, 1, 2, 3, \ldots)$. The x-y subspace contains the harmonics on the order of $10k \pm 3$ $(k = 0, 1, 2, 3, \ldots)$. Each vector can be considered a five-digit binary code. The leftmost bit corresponds to the switching state of inverter leg a while the rightmost bit corresponds to the switching state of inverter leg e. Each leg's switching state is represented by a 0 or 1, which indicates, respectively, the output voltage levels that correspond to the DC bus midpoint, namely, $\frac{-V_{dc}}{2}$ and $\frac{V_{dc}}{2}$.

The CMV value can be calculated based on the switching states of each VSI leg, as follows [22]:

$$V_{CM} = \frac{V_{dc}}{5}(S_a + S_b + S_c + S_d + S_e) - \frac{V_{dc}}{2} \quad (2)$$

where V_{CM} is the CMV value; S_i are the inverter leg's switching states, with $i = \{a, b, c, d, e\}$; and V_{dc} is the DC bus voltage. Table I summarizes the CMV values according to the applied switching state. Thus, by choosing and applying specific vectors, modulation strategies can be implemented in order to obtain the desired CMV waveform. Therefore, the CMV transitions and the maximum CMV amplitude can be defined.

A. Five-phase ΣΔ algorithm operation

The ΣΔ modulation strategies applied in this paper are based on the ΣΔ modulation technique proposed in [38]. Four ΣΔ modulator loops are implemented in order to follow the reference vector in both the α-β and x-y subspaces, as shown

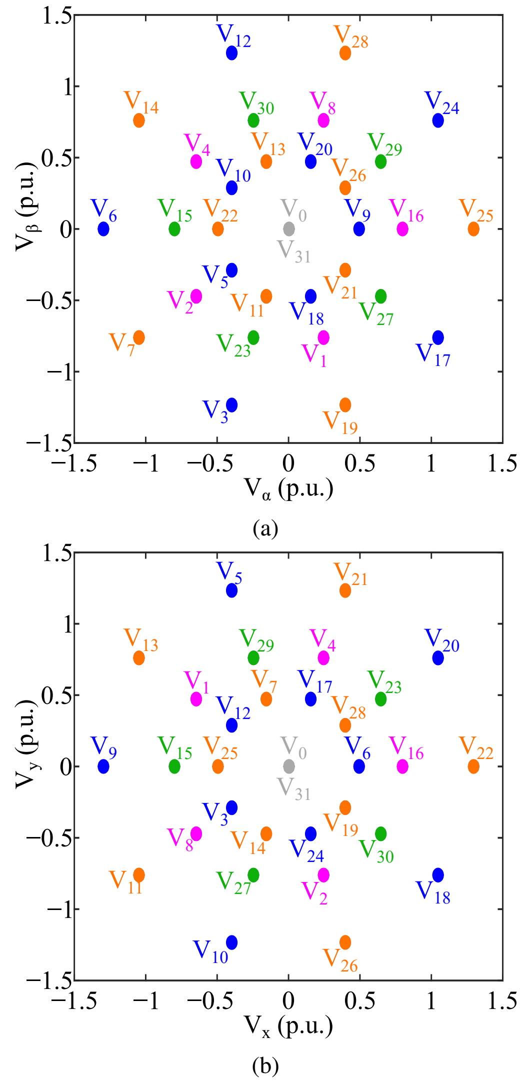


Fig. 2: Five-phase 2-D subspaces: (a) α-β, and (b) x-y subspace. Orange switching states generate CMV of $0.1V_{dc}$, green switching states generate CMV of $0.3V_{dc}$, purple switching states generate CMV of –$0.3V_{dc}$, and blue switching states generate CMV of –$0.1V_{dc}$.

in Fig. 3. The outputs of the ΣΔ modulator loop go into a CMV quantizer, which implements a set of vectors and the nearest-vector algorithm in order to choose the vector that is closest to the reference input.

First, the ΣΔ modulator loops compare the position of the reference vector in the α-β and x-y subspaces (V_α, V_β, V_x, and V_y) with the current CMV quantizer output, which is the applied vector position (V'_α, V'_β, V'_x, and V'_y). Since the applied vector varies depending on which set of vectors is implemented, the feedback values of the ΣΔ modulator loops also vary. As the applied vector, which depends on the modulation strategy, is always the one closest to the reference vector, the errors of the modulating loops are minimized. These errors are integrated, or doubly integrated, and become the input signals of the CMV quantizer (V^*_α, V^*_β, V^*_x, and V^*_y), as shown in Fig. 3.

Second, in accordance with the selected set of vectors,

TABLE I: CMV value according to the applied vector.

Vectors, V_j (switching states)	CMV value
V_{31}(11111)	$+0.5V_{dc}$
V_{15}(01111), V_{23}(10111), V_{27}(11011), V_{29}(11101), V_{30}(11110)	$+0.3V_{dc}$
V_7(00111), V_{11}(01011), V_{13}(01101), V_{14}(01110), V_{19}(10011), V_{21}(10101), V_{22}(10110), V_{25}(11001), V_{26}(11010), V_{28}(11100)	$+0.1V_{dc}$
V_3(00011), V_5(00101), V_6(00110), V_9(01001), V_{10}(01010), V_{12}(01100), V_{17}(10001), V_{18}(10010), V_{20}(10100), V_{24}(11000)	$-0.1V_{dc}$
V_1(00001), V_2(00010), V_4(00100), V_8(01000), V_{16}(10000)	$-0.3V_{dc}$
V_0(00000)	$-0.5V_{dc}$

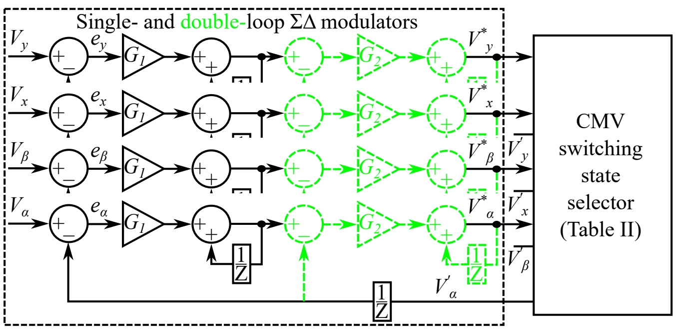


Fig. 3: Single- and double-loop ΣΔ modulators. The green line shows the second integrator-loop for the double-loop ΣΔ modulator. The value of the G_1 and G_2 is 0.9.

the nearest-vector algorithm of the CMV quantizer calculates the distances between the inputs (V^*_α, V^*_β, V^*_x, V^*_y) and the positions of the selected vectors (V'_α, V'_β, V'_x, V'_y) in both subspaces as follows:

$$D^2_{\alpha\beta j} = (V'_{\alpha j} - V^*_\alpha)^2 + (V'_{\beta j} - V^*_\beta)^2 \quad (3)$$

$$D^2_{xyj} = (V'_{xj} - V^*_x)^2 + (V'_{yj} - V^*_y)^2 \quad (4)$$

where $D^2_{\alpha\beta j}$ and D^2_{xyj} are the square distances from the ΣΔ modulator loops outputs (V^*_α, V^*_β, V^*_x, V^*_y) to each j vector position ($V'_{\alpha j}$, $V'_{\beta j}$, V'_{xj}, V'_{yj}). $D^2_{\alpha\beta j}$ and D^2_{xyj} are calculated instead of $D_{\alpha\beta j}$ and D_{xyj} in order to simplify the nearest-vector algorithm by avoiding the square root operation.

Third, the CMV quantizer calculates the total distance to each vector, as follows:

$$D_j = D^2_{\alpha\beta j} + D^2_{xyj} \quad (5)$$

where D_j is the sum of the squared distances for each vector.

Finally, the CMV quantizer chooses the vector with the lowest total distance by applying (6):

$$V_j = min\{\hat{D}_j\} \quad (6)$$

where V_j is the vector with the minimum distance value. In addition, the algorithm feeds back the ΣΔ modulator loops with the coordinates of the chosen vector (V'_α, V'_β, V'_x, and V'_y).

Notably, the switching frequency is variable in ΣΔ modulation techniques, whereas it remains constant in SVM and PWM techniques. Therefore, in order to compare the performance of ΣΔ modulation techniques with those of SVM and PWM techniques, it is necessary to set a maximum switching frequency value (f_{max}), as follows:

$$f_{max} = \begin{cases} f_{sw} & \text{for 2L+2M SVM} \\ f_s/2 & \text{for } \Sigma\Delta \text{ modulations} \end{cases} \quad (7)$$

where f_{sw} is the switching frequency and f_s is the sampling frequency.

B. Five-phase CMV mitigation ΣΔ modulation strategies

These proposed ΣΔ modulation strategies are based on choosing sets of vectors that reduce the maximum peak-to-peak CMV amplitude by 80%. In addition, the CMV transitions are limited to $0.2V_{dc}$ steps. In order to accomplish this, six modulation strategies were implemented. The ΣΔ-CMVR1 and ΣΔ-CMVR2 modulation strategies limit the CMV amplitude between –$0.1V_{dc}$ and $0.1V_{dc}$; ΣΔ-CMVR3 and ΣΔ-CMVR4 modulation strategies limit it to between $0.1V_{dc}$ and $0.3V_{dc}$; and ΣΔ-CMVR5 and ΣΔ-CMVR6 modulation strategies limit it to between –$0.3V_{dc}$ and –$0.1V_{dc}$. Table II summarizes the main characteristics of these modulation strategies.

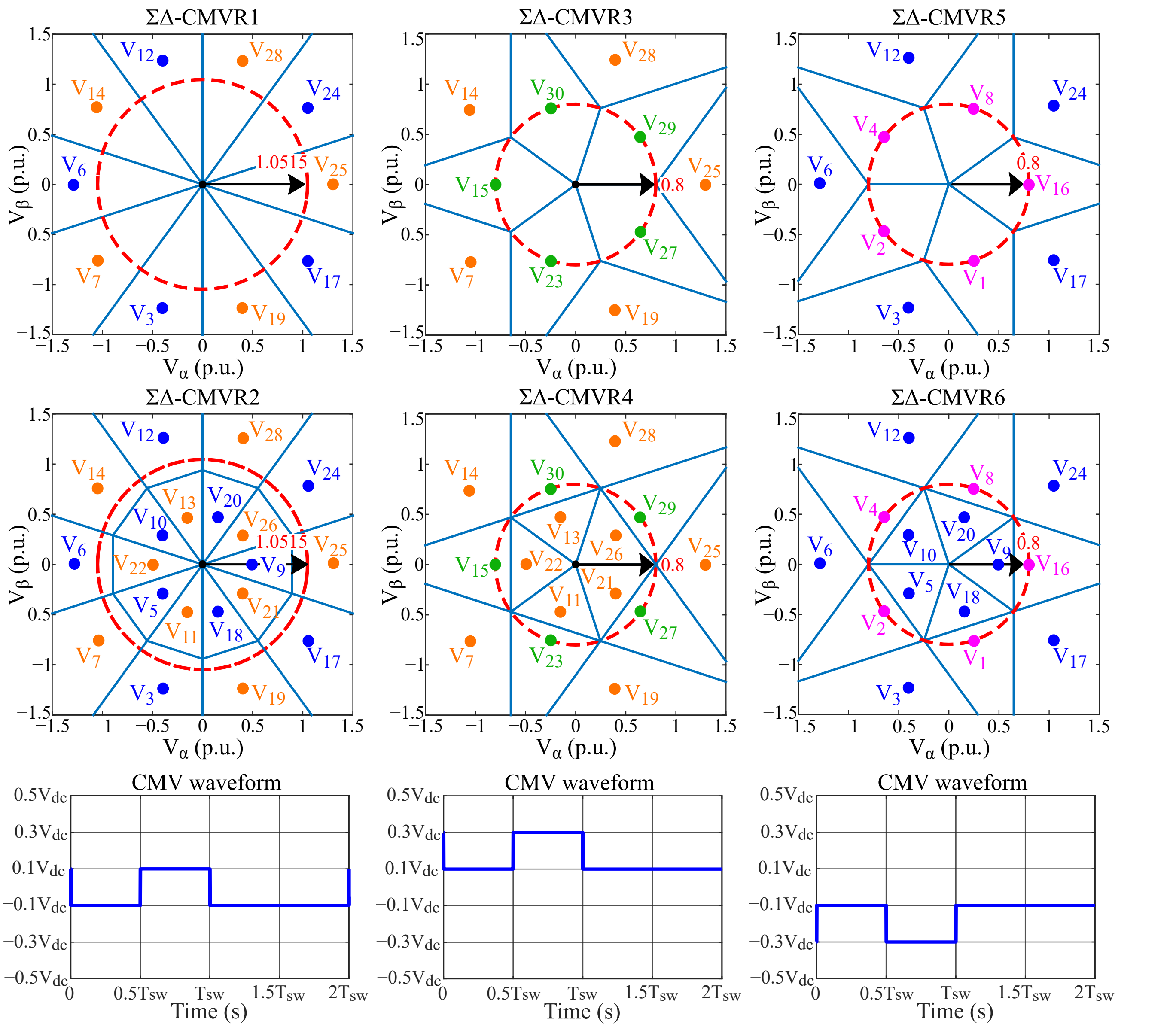
TABLE II: Summary of the proposed ΣΔ modulation techniques characteristics.

Modulation techniques	Vectors	CMV levels	CMV dv/dt Max. trans.[1]	Linear region
ΣΔ-CMVR1	V_3, V_6, V_7, V_{12}, V_{14}, V_{17}, V_{19}, V_{24}, V_{25}, V_{28}	$0.1V_{dc}$ –$0.1V_{dc}$	2	m ≤ 1.015
ΣΔ-CMVR2	V_3, V_5, V_6, V_7, V_9, V_{10}, V_{11}, V_{12}, V_{13}, V_{14}, V_{17}, V_{18}, V_{19}, V_{20}, V_{21}, V_{22}, V_{24}, V_{25}, V_{26}, V_{28}	$0.1V_{dc}$ –$0.1V_{dc}$	2	m ≤ 1.015
ΣΔ-CMVR3	V_7, V_{14}, V_{15}, V_{19}, V_{23}, V_{25}, V_{27}, V_{28}, V_{29}, V_{30}	$0.3V_{dc}$ $0.1V_{dc}$	2	m ≤ 0.8
ΣΔ-CMVR4	V_7, V_{11}, V_{13}, V_{14}, V_{15}, V_{19}, V_{21}, V_{22}, V_{23}, V_{25}, V_{26}, V_{27}, V_{28}, V_{29}, V_{30}	$0.3V_{dc}$ $0.1V_{dc}$	2	m ≤ 0.8
ΣΔ-CMVR5	V_1, V_2, V_3, V_4, V_6, V_8, V_{12}, V_{16}, V_{17}, V_{24}	–$0.1V_{dc}$ –$0.3V_{dc}$	2	m ≤ 0.8
ΣΔ-CMVR6	V_1, V_2, V_3, V_4, V_5, V_6, V_8, V_9, V_{10}, V_{12}, V_{16}, V_{17}, V_{18}, V_{20}, V_{24}	–$0.1V_{dc}$ –$0.3V_{dc}$	2	m ≤ 0.8

[1] Per switching period (f_{max}).

Fig. 4 shows the Voronoi diagram and theoretical CMV waveforms. The Voronoi diagram offers a graphical view of the vectors used by the proposed ΣΔ modulation strategies.

The ΣΔ-CMVR1 strategy is based on using only large vectors. Its maximum value of m in the linear region is 1.0515, the same as with DL-5P-AV-ΣΔ [38]. The proposed modulation ΣΔ-CMVR3 strategy implements a vector group composed of large and medium vectors, as shown in Fig. 4b.Due to the use of large vectors, the maximum value of m can be geometrically determined as $m = (4/5)\cdot 2\cdot cos^2(\pi/5) = 1.047$. However, due to the performance of the ΣΔ modulation, it is not possible to reach this value of m. The red dashed line in the Voronoi diagram in Fig, 4b shows the linear operation region of the ΣΔ-CMVR3 modulation strategy (m = 0.8). Working outside



(a) (b) (c)

Fig. 4: Voronoi diagram and CMV waveform of the proposed modulation techniques: (a) ΣΔ-CMVR1 and ΣΔ-CMVR2, (b) ΣΔ-CMVR3 and ΣΔ-CMVR4, (c) ΣΔ-CMVR5 and ΣΔ-CMVR6.

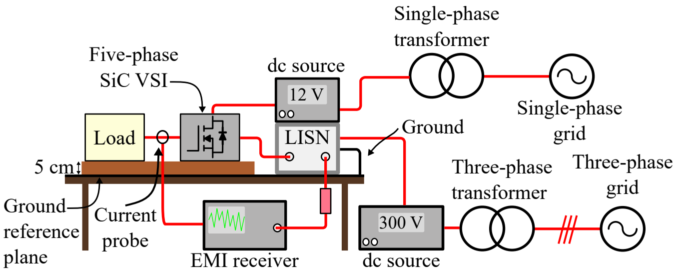
this area would distort the output current. On the other hand, ΣΔ-CMVR5 uses a group of large and medium vectors that limit the CMV waveform to values between –0.3V_{dc} and –0.1V_{dc}, as shown in Fig. 4c. Just as with the ΣΔ-CMVR3 modulation strategy, the maximum value of m in the linear region is 0.8, as shown by the dashed red line in Fig. 4c.

In the ΣΔ-CMVR2, ΣΔ-CMVR4, and ΣΔ-CMVR6 modulation techniques, and depending on the operating point, the implementation of small vectors improves the output waveform quality due to the increase in the number of the available switching states, thus improving the ΣΔ modulator loop resolution. However, the use of small vectors slightly decreases the efficiency of the proposed modulation techniques, as it implies additional switching operations among small neighboring vectors.

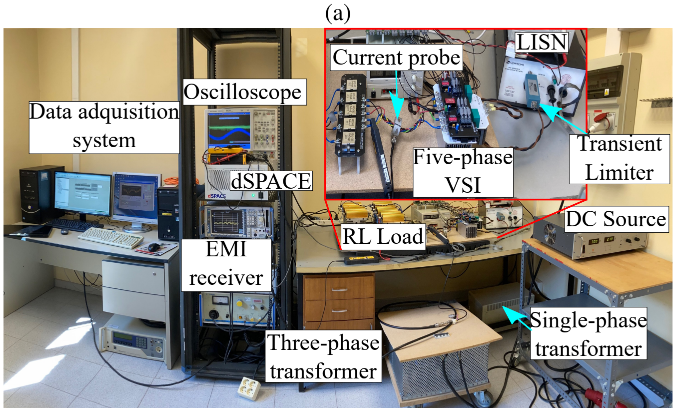
III. Results

Simulation and experimental results were obtained to evaluate the performance of the proposed modulation strategies. The simulations, performed in Matlab/Simulink and PLECS Blockset, analyzed the effects of using single-loop (SL) and double-loop (DL) ΣΔ modulators on the average switching operations per MOSFET.

The experimental results for THD, efficiency, CMV, and EMIs generated by the proposed modulation strategies were obtained on a five-phase VSI prototype. Fig. 5 shows the schematic and experimental setup. This prototype consists of SiC modules FS45MR12W1M1_B1. The VSI was fed by a 300 V_{dc} source connected through a Line Impedance Stabilization Network (LISN) (10 kHz to 30 MHz frequency range). An R-L load with R = 34 Ω and L = 470 μH were connected at the



(a)



(b)

Fig. 5: Experimental setup: (a) setup schematic, and (b) implemented setup.

VSI output. The modulation techniques were implemented on a dSPACE platform (DS1006 board and DS5203 FPGA). The voltages and currents were measured with a high-resolution oscilloscope (1 GHz bandwidth and 4 GS/s sampling rate); a high voltage differential probe (400 MHz bandwidth); and a current probe (100 MHz bandwidth). VSI efficiency was measured using a digital power meter (1 MHz bandwidth). CMC and conducted EMI were measured using an RF current probe (9 kHz to 30 MHz range) and an EMI receiver (9 kHz to 3 GHz range) complying with the standard CISPR-16-1-1 [40]. The performance of the proposed modulation techniques was compared with that of the AZSPWM [22], the RCMV-CBM2 [23], and the SCPWM-2 [25] modulation techniques.

A. Analysis of the number of switching operations under single- and double-loop ΣΔ modulators.

Both resolution and output voltage THD in ΣΔ modulation improve with the number of integrator loops. However, the number of integrator loops also affects the number of transistor switching operations. Fig. 6 shows the number of switching operations per transistor during a fundamental period using single- and double-loop ΣΔ modulators in the proposed modulation techniques.

In ΣΔ-CMVR1 and ΣΔ-CMVR2, using double-loop ΣΔ modulators allows for reducing the number of switching operations from 10.2% to 30.2%. On the other hand, the single-loop ΣΔ modulators used in ΣΔ-CMVR3 and ΣΔ-CMVR5 lower the number of switching operations when compared to those obtained with double-loop ΣΔ modulators, but only for

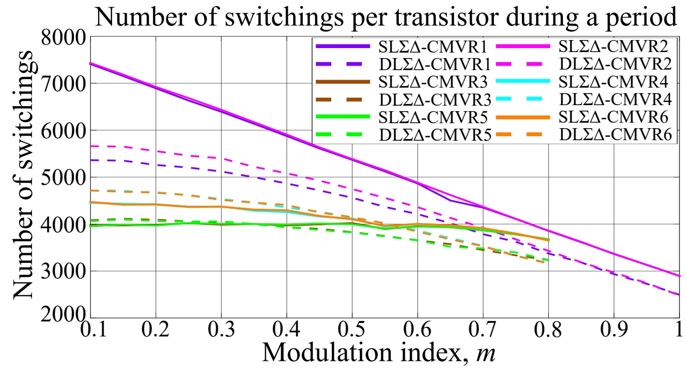


Fig. 6: Comparison of transistor switching operations during a fundamental period using single-loop and double-loop ΣΔ modulators at f_{max} of 200 kHz.

$m < 0.35$. Similar performance is observed in ΣΔ-CMVR4 and ΣΔ-CMVR6: single-loop ΣΔ modulators generate fewer switching operations for values of $m < 0.6$. Furthermore, despite the number of implemented integrator loops, ΣΔ-CMVR3, ΣΔ-CMVR4, ΣΔ-CMVR5, and ΣΔ-CMVR6 show a lower number of switching operations compared to those of ΣΔ-CMVR1 and ΣΔ-CMVR2.

B. THD and efficiency analysis

Table III shows the experimental results from testing the line voltage THD and the VSI efficiency under the proposed modulation techniques. The experimental results were also obtained for the AZSPWM, RCMV-CB2, and SCPWM-2 strategies in order to compare the results of the proposed modulation techniques with those of others that similarly mitigate CMV. The THDs of the first forty harmonics were measured as specified in the EN 50160 standard [39]. The modulation techniques have a lower THD than those of the other compared PWM techniques; a difference that is evident for values of $m < 0.7$. The THDs of the DLΣΔ-CMVR3 and DLΣΔ-CMVR5 modulation techniques increase when operating at a modulation index of $0.7 < m < 0.8$, because they approach the limit of their linear region of operation ($m = 0.8$). However, in DLΣΔ-CMVR4 and DLΣΔ-CMVR6, using small vectors helps overcome this drawback and allows having a low THD output voltage. In addition, the proposed modulation strategies have a THD that is similar to that of the DL-5P-AV-ΣΔ modulation strategy despite having fewer vectors available. Regarding current THD, the ΣΔ modulation strategies present a lower THD in comparison with those of the PWM techniques, as shown in Fig. 7. Thus, despite the reduction in the number of switching operations and the number of available vectors, the proposed modulation strategies achieve output voltages and currents with low THD.

On the other hand, VSI efficiency improves with the proposed modulation techniques as compared to the others, mainly by reducing the number of VSI switching operations and thereby decreasing the switching losses. When the proposed modulation techniques are implemented, the VSI efficiency improves between 3.06% and 35.13% when com-

TABLE III: Experimental THD and efficiency performance.

Switching frequency (f_{max})	Modulation technique	Line voltage THD (%) Modulation index, m				Efficiency (%) Modulation index, m							
		0.3	0.5	0.7	0.9	0.2	0.3	0.4	0.5	0.6	0.7	0.8	0.9
200 kHz	AZSPWM [22]	1.95	1.18	0.65	0.55	50.69	67.93	78.69	84.99	88.66	90.78	92.39	93.57
	SCPWM-2 [25]	2.30	1.01	0.70	0.52	47.21	67.60	78.08	84.22	88.29	90.61	92.49	93.81
	RCMV-CBM2 [23]	2.12	1.66	1.03	0.70	50.80	67.18	78.49	84.93	88.83	91.02	92.69	93.87
	DLΣΔ-CMVR1	0.97	0.64	0.30	0.22	73.83	83.87	88.70	92.78	94.82	96.22	96.80	96.93
	DLΣΔ-CMVR2	**0.90**	**0.31**	**0.28**	**0.25**	**70.16**	**82.29**	**87.81**	**92.06**	**94.49**	**96.01**	**96.15**	**97.26**
	DLΣΔ-CMVR3	1.07	0.49	0.64	–	82.34	88.17	92.65	94.96	96.28	97.29	97.10	–
	DLΣΔ-CMVR4	0.48	0.75	0.36	–	80.15	87.09	91.11	94.18	95.19	96.99	97.12	–
	DLΣΔ-CMVR5	1.13	0.55	0.60	–	81.69	87.69	92.26	94.80	95.99	97.15	97.03	–
	DLΣΔ-CMVR6	0.49	0.65	0.32	–	79.13	86.36	90.54	93.93	94.92	96.82	97.08	–
	DL-5P-AV-ΣΔ [38]	0.90	0.44	0.43	0.30	83.40	86.53	89.44	92.60	94.78	95.96	96.59	97.26

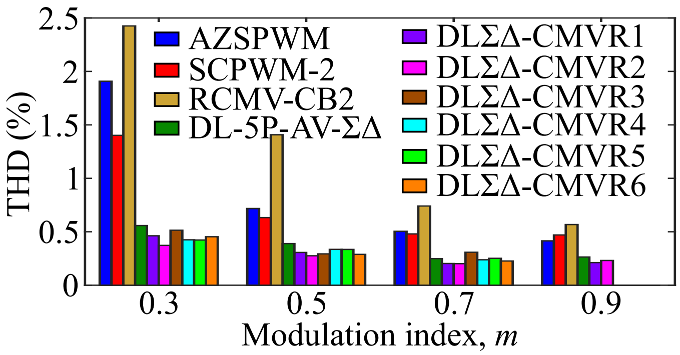


Fig. 7: Experimental current THD at f_{max} of 200 kHz.

pared to the effiency of the VSI under the other modulation techniques.

This trend in efficiency is linked to the number of switching operations per fundamental period, as observed in Fig. 6. Therefore, the DLΣΔ-CMVR3 and the DLΣΔ-CMVR5 modulation techniques provide higher efficiency than the DLΣΔ-CMVR1. This is because the use of medium vectors reduces simultaneous switching operation. In contrast, using only large vectors results in at least two simultaneous switching operations per sampling period. The use of small vectors slightly decreases the efficiency of the VSI because of the fact that the change of state between small neighboring vectors involves three simultaneous switching operations. Although the DLΣΔ-CMVR2 modulation technique provides the inverter with the lowest efficiency compared to the other proposed modulations, its linear region of operation is the same ($m = 1.0515$) as those of AZSPWM, SCPWM-2, and RCMV-CB2. In addition, its output voltage has the lowest THD compared to the other proposed modulation techniques. For these reasons, the remaining results were obtained using only the DLΣΔ-CMVR2 modulation strategy. The proposed modulation strategies provide the VSI with an efficiency which is similar to that obtained with the DL-5P-AV-ΣΔ modulation strategy, sometimes even slightly better, depending on the working point and the modulation strategy used.

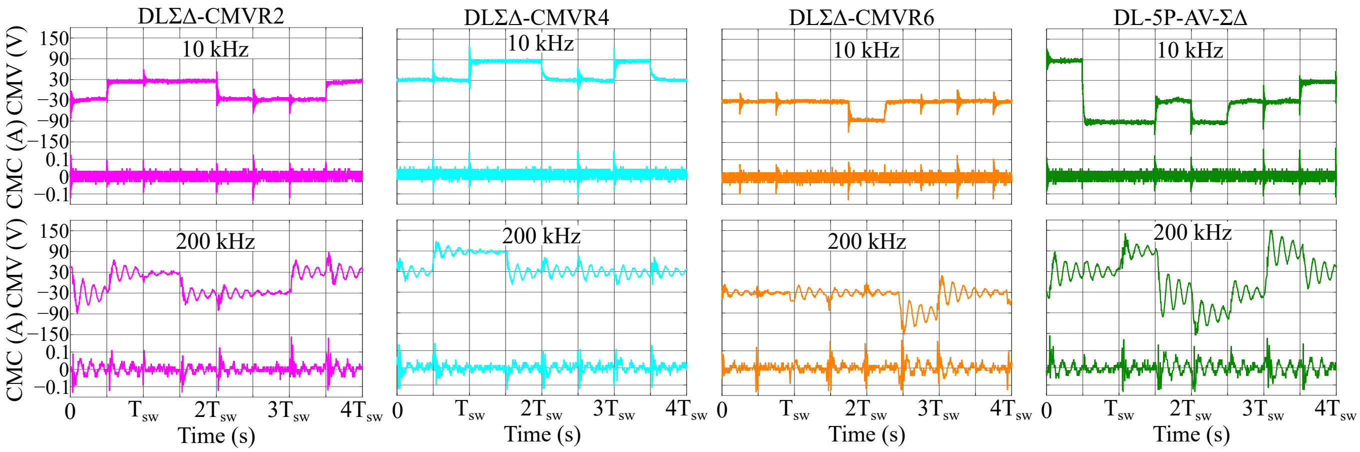
C. Performance comparison between DLΣΔ-CMVR and DL-5P-AV-ΣΔ.

Figure 8 shows the CMV and CMC waveforms at f_{max} of 10 and 200 kHz for the DLΣΔ-CMVR2, DLΣΔ-CMVR4, DLΣΔ-CMVR6, and DL-5P-AV-ΣΔ strategies. Fig. 8 corroborates the simulation results by showing the different CMV levels and their corresponding CMCs. A change in the vector to be applied does not imply a CMV level change, but it can generate a CMC glitch, as can be observed in Fig. 8. Besides, a clear difference in the CMV ringing when working at high or low switching frequencies can be observed.

Figure 9 shows the frequency spectra analysis of the CMV, CMC, and conducted EMIs at f_{max} = 200 kHz. In Fig. 9a can be seen how the maximum amplitudes of the CMV components get reduced when the proposed modulation strategies are implemented in comparison with those obtained with the DL-5P-AV-ΣΔ [38]. This performance is due to the limitation in the values of the CMV level transitions achieved by the proposed modulation strategies. The CMC spectra is shown in Fig. 9b. In a similar way to what happens with the CMV spectra, the proposed modulation strategies also manage to reduce the maximum amplitude of the CMC components. The reduction in the CMC components is due to the fact that the proposed modulation strategies have fewer available vectors than the DL-5P-AV-ΣΔ strategy, thus increasing the odds of applying the same vector in consecutive sampling steps. The fact that the proposed modulation strategies also manage to reduce the amplitude of conducted EMI with respect to those produced by the use of DL-5P-AV-ΣΔ modulation can be seen in Fig. 9c. DLΣΔ-CMVR4 and DLΣΔ-CMVR6 strategies always exhibit a better performance, however their linear operation range is limited to m = 0.8. Nevertheless, the DLΣΔ-CMVR2 strategy still has better performance when compared to that of the DL-5P-AV-ΣΔ without such a restriction in its linear output voltage operating range.

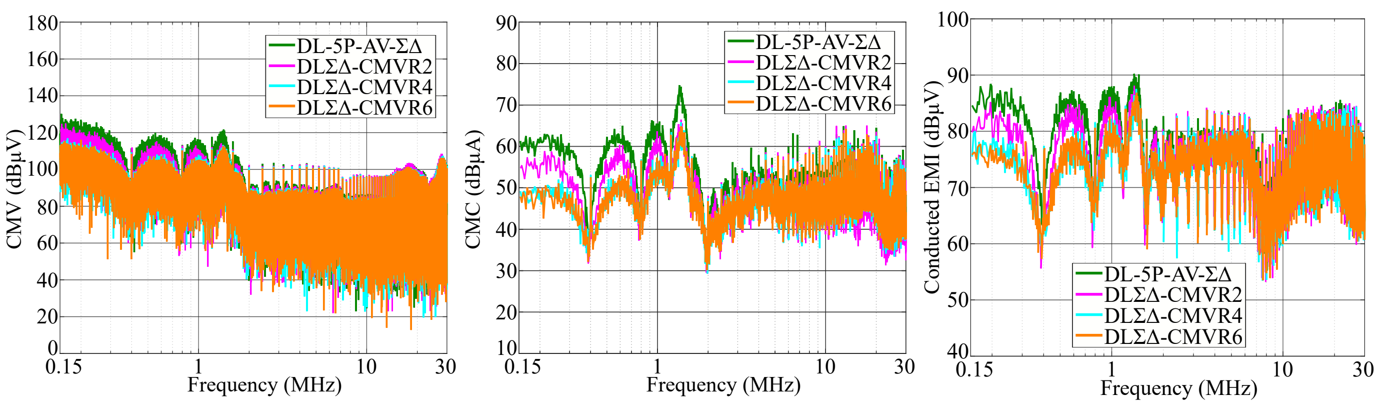
D. Comparison of CMV, CMC and conducted EMI performance of the CMV reduction techniques

The DLΣΔ-CMVR2 modulation technique provides the inverter with the lowest efficiency compared to the other proposed modulations. However, its linear region of operation is the same ($m = 1.0515$) as those of AZSPWM, SCPWM-2, and RCMV-CB2. In addition, its output voltage has the lowest THD compared to the other proposed modulation techniques. For these reasons, the DLΣΔ-CMVR2 modulation is chosen to analyze its performance relative to the conducted CMV, CMC, and EMI and compare it with those of the other PWM modulation strategies.



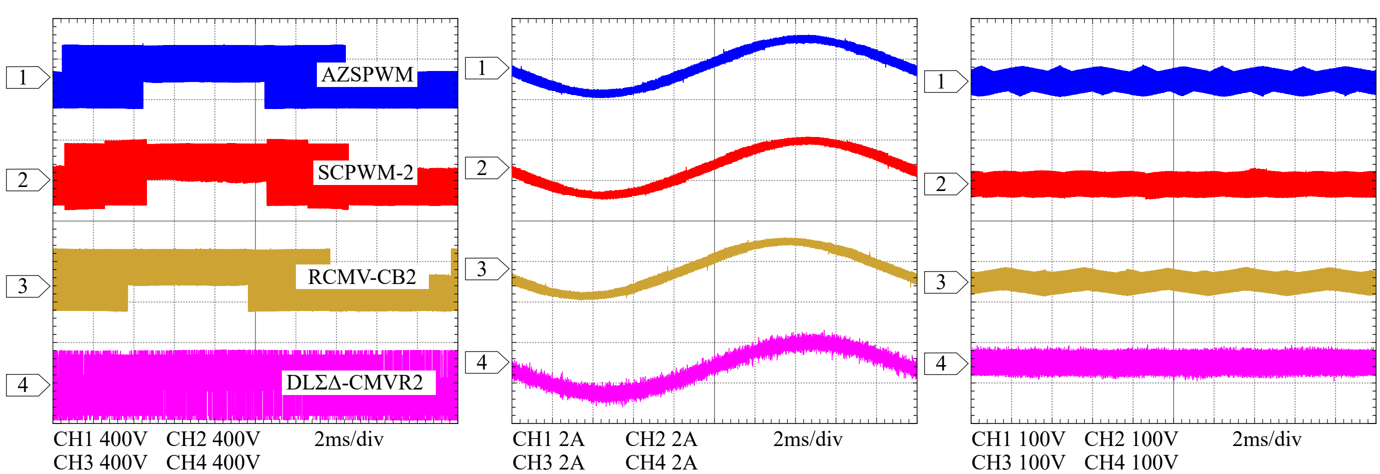
(a) (b) (c) (d)

Fig. 8: Experimental CMV and CMC waveforms at m=0.7 and f_{max} of 10 and 200 kHz: (a) DLΣΔ-CMVR2, (b) DLΣΔ-CMVR4, (c) DLΣΔ-CMVR6, and (d) DL-5P-AV-ΣΔ.



(a) (b) (c)

Fig. 9: Experimental frequency spectra f_{max} of 200 kHz and m=0.7: (a) CMV, (b) CMC, and (c) conducted EMI.



(a) (b) (c)

Fig. 10: Experimental output waveforms at f_{max} of 200 kHz and m=0.7 for AZSPWM (CH1), SCPWM-2 (CH2), RCMV-CB2 (CH3), and DLΣΔ-CMVR2 (CH4): (a) line voltage, (b) current, and (c) CMV waveform.

Fig. 10 shows the line voltage, current, and CMV generated by AZSPWM, SCPWM-2, RCMV-CB2, and DLΣΔ-CMVR2. Although the line voltage is different for each modulation technique, all of them generate a sinusoidal current at the VSI output, as shown in Figs. 10a and 10b. Furthermore, Fig. 10c shows the CMV generated by each modulation technique. The

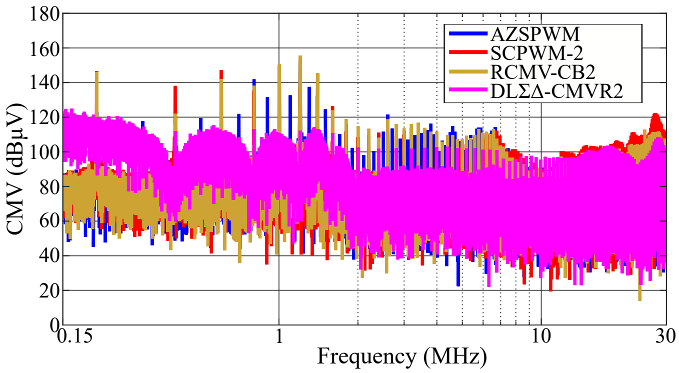


Fig. 11: Experimental CMV spectrum at f_{max} of 200 kHz and m=0.7.

four modulation techniques reduce the CMV peak amplitude by 80%, thus obtaining a $0.2V_{dc}$ peak-to-peak amplitude.

The spectrum of the experimental CMV is shown in Fig. 11. The DLΣΔ-CMVR2 modulation technique has a maximum amplitude of 125.02 dBμV, which is lower than those of AZSPWM, SCPWM-2, and RCMV-CB2, whose maximum amplitudes are 153.06, 147.16, and 155.64 dBμV, respectively. This is because the DLΣΔ-CMVR2 technique spreads the CMV frequency components over the entire frequency spectrum, thereby allowing a decrease in the amplitude of the CMV components.

The reduction in switching operations not only improves the efficiency of the VSI but also has an impact on the number of CMV transitions. The DLΣΔ-CMVR2 modulation technique considerably reduces the number of transitions to 1 or 2 per switching period. On the other hand, AZSPWM and RCMV-CB2 have the same number of CMV transitions as a conventional five-phase modulation technique. The SCPWM-2 has a slightly smaller number of CMV transitions than AZSPWM and RCMV-CB2. This performance can be seen in Fig. 12a. The maximum CMC amplitude of DLΣΔ-CMVR2 (65.2 dBμA) is 16.9 to 19.3 dBμA lower than those of AZSPWM (83 dBμA), SCPWM- 2 (82.1 dBμA), and RCMV-CB2 (84.5 dBμA).

Fig. 12b shows the results of the conducted EMI analysis. The maximum amplitudes of conducted EMIs for AZSPWM, SCPWM-2, RCMV-CB2, and DLΣΔ-CMVR2 are 95.6, 94, 95.4, and 87.9 dBμV, respectively. Therefore, DLΣΔ-CMVR2 modulation reduces the conducted EMI maximum amplitude by 6.1 to 7.7 dBμV when compared with the other modulation techniques. Table IV summarizes the experimental results obtained from the analysis of the CMV, CMC, and conducted EMI frequency spectra.

TABLE IV: Maximum frequency component amplitude of CMV, CMC, and conducted EMI at f_{max} = 200 kHz and m = 0.7.

Modulation technique	CMV (Fig. 11) dBμV	CMC (Fig. 12a) dBμA	Conducted EMIs (Fig. 12b) dBμV
DLΣΔ-CMVR2	125.02	65.2	87.9
AZSPWM [22]	153.06	83.0	95.6
SCPWM-2 [25]	147.16	82.1	94.0
RCMV-CB2 [23]	155.64	84.5	95.4

IV. Conclusion

In this paper several modulation techniques based on ΣΔ modulators that provide an 80% reduction in the maximum peak-to-peak amplitude of CMV by choosing a set of vectors are proposed. The proposed modulation techniques are applied to a high-frequency five-phase VSI converter. Depending on the vector-set chosen, the CMV is limited to values of between –$0.3V_{dc}$ and –$0.1V_{dc}$, –$0.1V_{dc}$ and $0.1V_{dc}$, and $0.1V_{dc}$ and $0.3V_{dc}$. The DLΣΔ-CMVR3, DLΣΔ-CMVR4, DLΣΔ-CMVR5, and DLΣΔ-CMVR6 modulation techniques, have the best efficiency. However, the limited maximum linear region of operation is limited ($0 \leq m \leq 0.8$) on account of their vector-sets. In contrast, the linear region of operation of DLΣΔ-CMVR1 and DLΣΔ-CMVR2 is the same as that of AZSPWM, SCPWM-2, and RCMV-CB2 ($0 \leq m \leq 1.0515$).

The performance of the proposed modulation strategies was compared with those of the DL-5P-AV-ΣΔ modulation. The proposed modulation strategies have a similar performance in THD and efficiency when DL-5P-AV-ΣΔ modulation is implemented. However, the performance is improved concerning CMV, CMC, and conducted EMI when using the proposed modulation strategies.

The feasibility of the proposed modulation techniques was evaluated through experimental results and compared with other PWM modulation techniques that similarly mitigate the CMV amplitude. However, the proposed modulation techniques demonstrate superior performance over the AZSPWM, SCPWM-2, and RCMV-CB2 modulation techniques in the following ways:

- The converter operation is between 3.06% and 35.13% more efficient, depending on the operating point.
- The output voltage has the lowest THD.
- The maximum amplitude of the CMV frequency components is reduced (22.14 to 30.62 dBμV reduction).
- The number of CMV transitions per switching period (f_{max}) is reduced, thereby also reducing the maximum amplitude of the CMC frequency components (16.9 to 19.3 dBμA reduction).
- The conducted EMI amplitude decreases.

On the other hand, the proposed modulation techniques require to be implemented at high switching frequencies in order not to lose resolution and to obtain a low voltage THD. Unlike the AZSPWM, SCPWM-2, and RCMV-CBM2 techniques that perform well at low switching frequencies, the proposed modulation techniques present an increase in their voltage THD. However, taking into account that the current trend in converters is to obtain high efficiency and high power density designs, the implementation of the proposed modulation techniques in conjunction with the use WBG devices does not represent a relevant drawback.

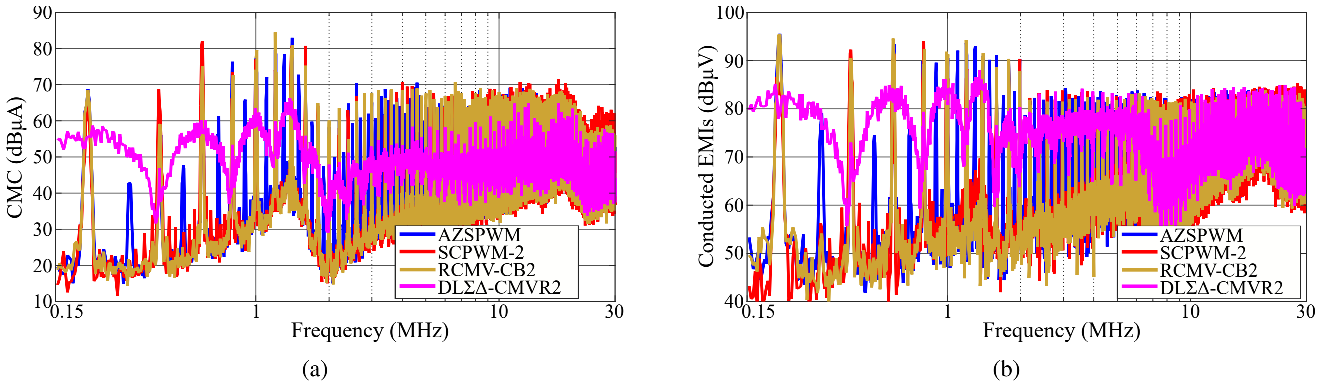


Fig. 12: Experimental EMIs analysis at f_{max} of 200 kHz and m=0.7: (a) CMC spectrum, and (b) conducted EMIs.

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Fernando Acosta-Cambranis (Student Member, IEEE) received the B.S. degree in Mechatronics engineering from the Universidad Autónoma de Yucatán (UADY), Yucatan, Mexico, in 2012 and the M.S. degree in automatic systems and industrial electronics in 2018 from the Universitat Politécnica de Catalunya (UPC), Barcelona, Spain, where he is currently working toward the Ph.D. degree in electronic engineering with the Motion and Industrial Control Group (MCIA), Department of Electronic Engineering, UPC, Terrassa, Spain. From 2014 to 2016, he was the supervisor of communications and control in the peninsular division of the Federal Electricity Commission (CFE) of Mexico. His research interests include modeling and control of power converters, multiphase converters, renewable energy, modulation techniques, and electromagnetic compatibility.

Jordi Zaragoza (Member, IEEE) received the B.S. degree in electronic engineering, the M.S. degree in automatic and electronic industrial engineering, and the Ph.D. degree from the Technical University of Catalonia (UPC), Catalonia, Spain, in 2001, 2004, and 2011 respectively. In 2003, he joined as an Assistant Professor with the Faculty of UPC, where he became an Associate Professor in 2012. From 2006 to 2007, he was a Researcher with the Energy Unit of ROBOTIKER-TECNALIA Technologic Corporation, Basque Country, Spain. Since 2017, he has been the Director of the Terrassa Industrial Electronics Group, UPC. He is the author of more than 70 published technical papers and has been involved in several projects in the fields of power electronics and systems. His research interests include modeling and control of power converters, multilevel converters, wind energy, power quality, and HVdc transmission systems.

Néstor Berbel (Member, IEEE) received the B.S., M.S., and Ph.D. degrees from the Technical University of Catalonia (UPC), Barcelona, Spain, in 2002, 2004, and 2015, respectively, all in electronic engineering. In 2003, he joined as an Assistant Professor with the Faculty of UPC, where he became an Associate Professor in 2012. His scientific research has been developed at the Terrassa Industrial Electronics Group, Department of Electronic Engineering, UPC, Terrassa, Spain. His research interests include microelectronic reliability, power converters, efficiency on power converters, modulations, and control loops applied on power converters.

Gabriel J. Capella received the B.S, M.S. and Ph.D. degrees in electrical engineering from the Technical University of Catalonia (UPC), Spain, in 1985, 2001 and 2015, respectively. Since 1986 he has been with the UPC where he is currently an Associate Professor. His research interests include parallel-connected converters, power quality, renewable energy systems and fault tolerant power electronics systems.

Luis Romeral (Member,IEEE) received the M.S. degree in electrical engineering and the Ph.D. degree from the Universitat Politècnica de Catalunya (UPC), Barcelona, Spain, in 1985 and 1995, respectively. In 1988, he joined the Electronic Engineering Department, UPC, where he is currently a Professor and the Director of the Motion and Industrial Control Group (MCIA), whose major research activities concern induction and permanent magnet motor drives, enhanced efficiency drives, fault detection and diagnosis of electrical motor drives, and improvement of educational tools. He has developed and taught post-graduate courses on programmable logic controllers, electrical drives and motion control, and sensors and actuators.