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# Compact and Wideband MMIC Phase Shifters Using Tunable Active Inductor Loaded All-Pass Networks

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# Compact and Wideband MMIC Phase Shifters Using Tunable Active Inductor Loaded All-Pass Networks

by

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## Dedication

To my family and friends especially my wife Jesusita and my boys, Antonio, Adiel, Athan and Alzan. I couldn't have done this without your love, support and understanding. Baba did this for you guys!

To my brother for laying down the footprints that I could follow and my Mom for refusing to give up on me.

To my "Comprade" Catarino for always being there for me especially during those difficult times. Thanks for all the advice and encouragement.

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To Mama Lina, Papa Tono, Tia Awi, Tia Blankie and Bito, seems like just yesterday you were here with me. Time goes by so fast and only the best memories of you remain. You made my childhood one that I would never trade for anything else. Love and miss you.

Dabito

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There are so many more people like me, with the desire to go to school and get an educationand hopefully have a positive impact on this world. With people like the ones mentionedabove it becomes a lot easier to turn those dreams into reality. Thanks!

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## Abstract

This dissertation addresses the design of monolithically integrated phase shifters at S- and L-frequency bands using a commercially available GaAs process from Triquint. The focus of the design is to operate over a wide bandwidth with full 360° phase shift capability, 50 Ω input/output impedance match and low RMS phase and gain errors. The first version of the design is based on passive all-pass phase shifters integrated with wideband amplifiers to compensate for insertion loss. This design uses a 4-bit system to achieve the required phase shift and each bit consists of 3 sections of all-pass filters designed at separate frequencies within the 0.8 – 3 GHz band. Simulation results show a complete 360° phase shift with RMS gain error of less than 0.6 dB and RMS phase error of less than 2.5°. The system is also shown to achieve good input and output impedance matching characteristics. However, the fabricated prototype fails to perform with full functionality due to the excessive number of passive inductors in the design and the resulting mutual coupling. The mutual coupling issue could be solved by spacing out the layout to allow more separation among the inductors. Unfortunately, in the S- and L-bands, this is not an option for this research work as the fabricated design already uses the maximum allowed chip size as determined by the foundry. In addition, larger chip sizes considerably increase the cost in practical applications. To address the challenging needs of small size, wide bandwidth and low frequency applicability, the second design introduced in this dissertation proposes a novel phase shifter implementation that utilizes tunable active differential inductors within all-pass networks. The inductor tuning is used to achieve phase shifts up to $180^0$. A switchable active balanced to unbalanced transition circuit (balun) is included in front of the all-pass network to complement its phase shift capability by

another 180°. In addition, the all-pass network is followed by a variable gain amplifier (VGA) to correct for gain variations among the phase shifting states and act as an output buffer. Although active inductors have been previously used in the design of various components, to the best of our knowledge, this is the first time that they have been used in an all-pass phase shifter. The approach is demonstrated with an on-chip design and implementation exhibiting wideband performance for S and L band applications by utilizing the 0.5 μm TriQuint pHEMT GaAs MMIC process. Specifically, the presented phase shifter exhibits $1 \times 3.95$ mm$^2$ die area and operates within the 1.5 GHz to 3 GHz band (i.e. 2:1 bandwidth) with 10 dB gain, less than 1.5 dB RMS gain error and less than 9° RMS phase error. Comparison with the state-of-the-art MMIC phase shifters operating in S and L bands demonstrates that the presented phase shifter exhibits a remarkable bandwidth performance from a very compact footprint with low power consumption. Consequently, it presents an important alternative for implementation of wideband phase shifters where all-passive implementations will consume expensive die real estate.

# Chapter 1:

# Introduction

## 1.1 Overview

A phased array is a group of antennas which act as a single antenna unit and allow the transmission or reception of an electronic signal in a specific direction (Beam-steering) by adjusting its effective radiation pattern while suppressing signals from undesired directions. The shape of the radiated pattern (Beam- Forming) can also be achieved by changing the signal amplitude in each antenna [1.1]. Combining the signals coherently also improves the signal to beam steering methods, the first being the mechanically rotating reflectors shown in Figure 1(a)

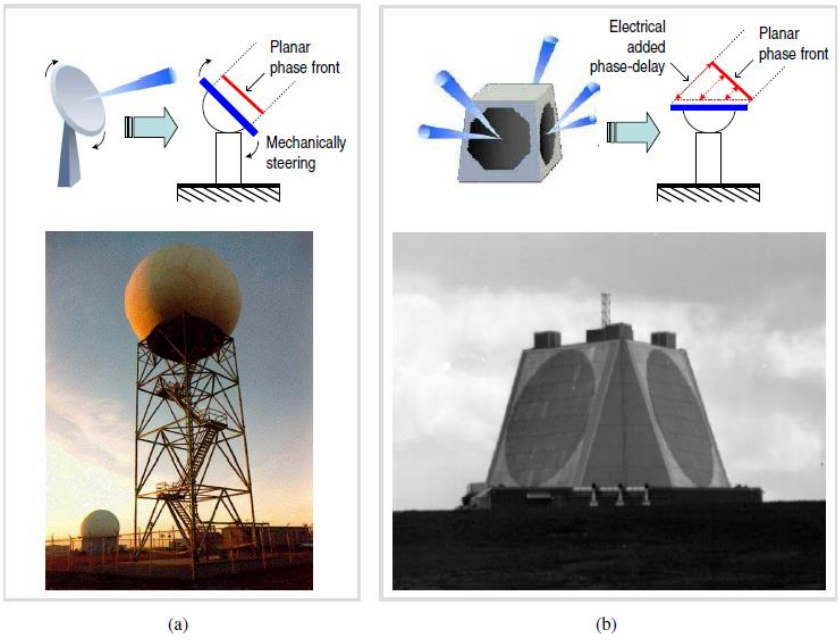


Figure 1-1. Array antenna systems: (a) mechanically steered, rotating reflector array and (b) electrically steered, fixed phased-array

noise ratio (SNR) of the system compared to a single antenna element. There exist two main beam steering methods, the first being the mechanically rotating reflectors shown in Figure 1(a) [1.2, 1.3] where the reflective surface is moved to change the angle of the beam and the second being the electronically beam steering phased array where beam steering is achieved by changing the phase of the signal on each antenna in the array as shown in Figure 1(b) [1.2, 1.3].

Phased array systems provide several advantages over mechanical radars since phased arrays can transmit multiple beams simultaneously while place a null in the direction of undesired signals such as jammers. These array systems can be one, two or three dimensional, and have a planar or conformal surface. In the case of a passive phased array (does not include any active devices providing gain to the system), the individual antenna elements consist of a T/R module which is a cascade of a phase-shifter and an attenuator where each element is individually adjusted to steer the beam. For the best performance of the phase array it is necessary to improve system noise figure as well as transmitter output power which can be achieved by using an active T/R module which has both a low noise and high power amplifier located inside it and can be used to compensate the losses of the feed network.

In the past, phased array systems were mainly used for military and government applications such as Search and Detection, Target Tracking, Missile Guidance, Air Mapping Systems and Ground and Battle field Surveillance [1.4]. Recently, phased array systems are being introduced for mobile cellular communications, automotive radar, Wi-Fi/Wimax networks as well as navigation and air traffic control [1.5, 1.6]. Figure 1-2 shows an example of implementation of phased array systems in mobile cellular networks which allows for an increase number of users to share the same available network [1.6]. It works by focusing energy in the desired direction thus minimizing energy toward other directions and satisfying transmit power requirements.

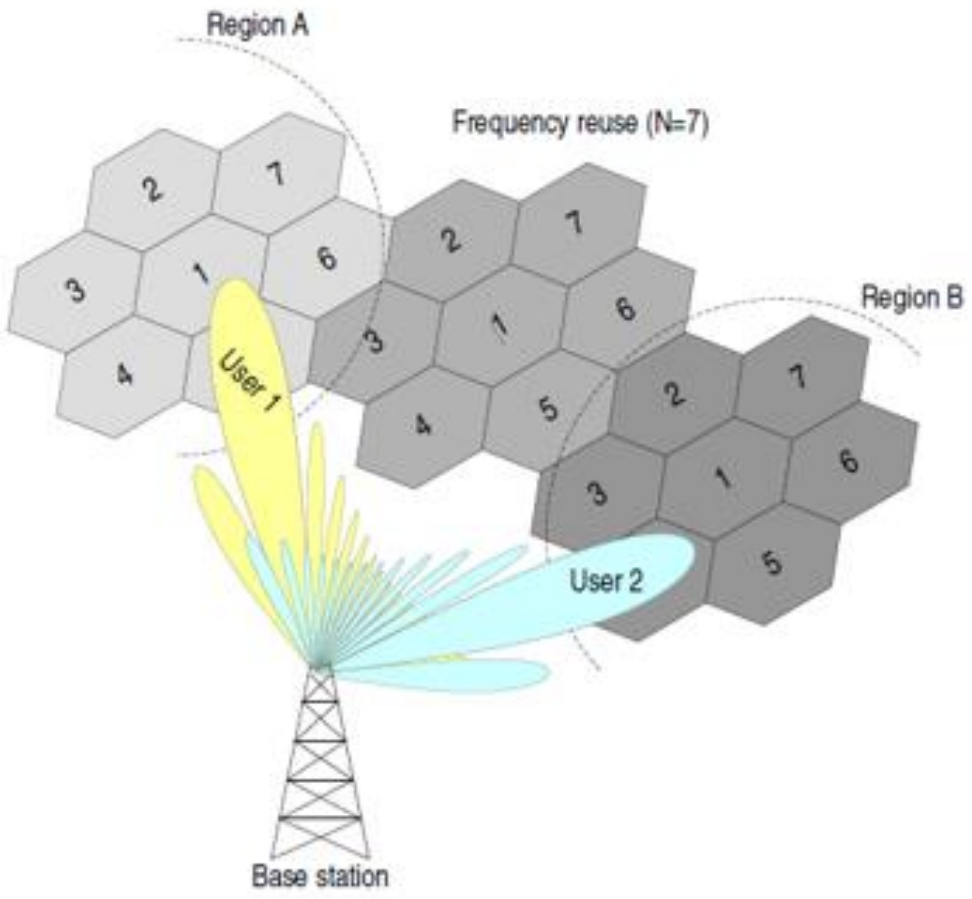


Figure 1-2. Beamforming in cellular wireless communication network

Some examples for civilian use of phased array systems is shown in Figure 1-3 [1.6]. Significant improvement in lead time for severe weather is made possible by rapid scan capabilities of phased arrays decrease warning times associated with extreme weather events. Phased-arrays also make it possible to more quickly accomplish aircraft surveillance tasks leading to more efficient air traffic controls. Phased-arrays systems can also be used to diagnose air quality at a level needed to track airborne biological, radiological, chemical and nuclear contaminants in the atmosphere.

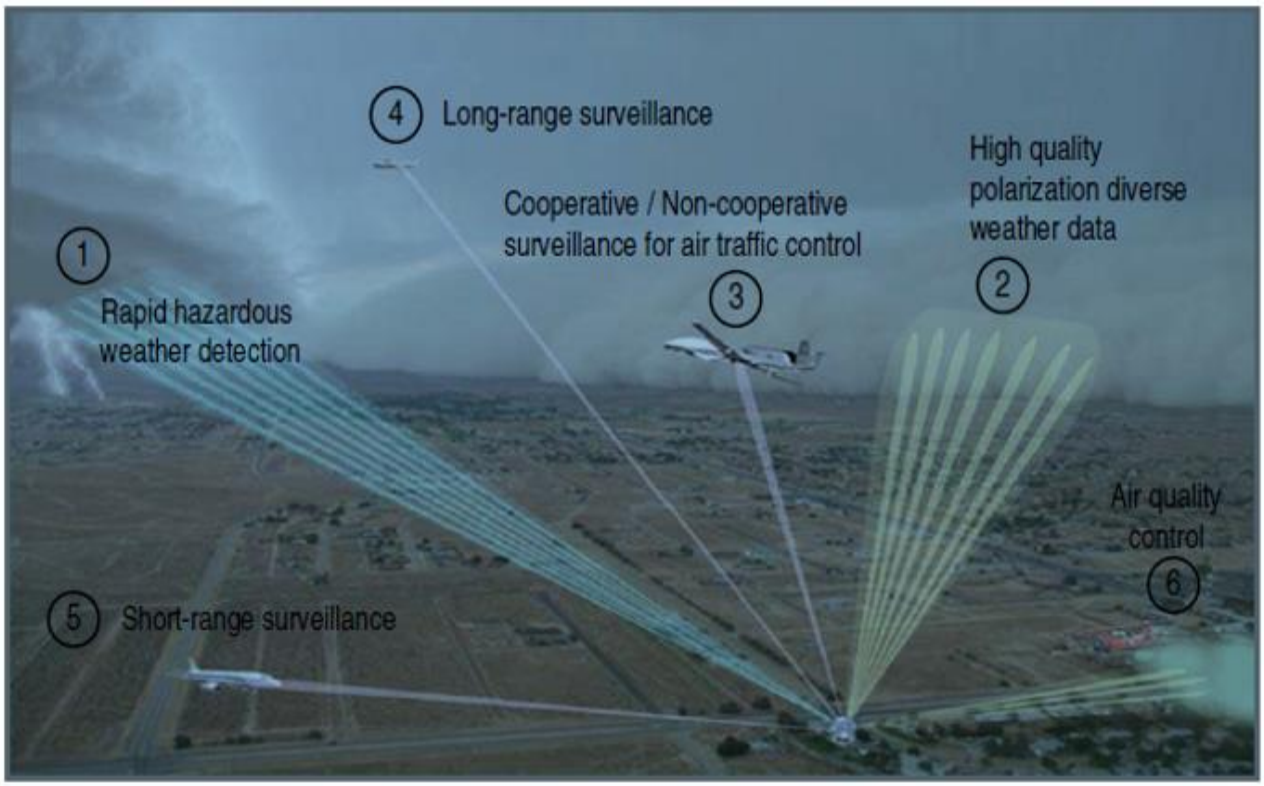


Figure 1-3. Phased-array applications in civilian sectors

Early phased array systems were developed exclusively using off the shelf components with a hybrid-design concept that includes printed circuit board components such as microstrip traces and strip lines as well as passive components combined with microwave integrated circuits resulting in not only high cost but also resulted in large bulky systems that consumed a lot of power [1.7]. Recently, commercial applications have become more feasible from a cost standpoint due to the maturity of technology of integrated circuits. This makes it possible to integrate the entire RF T/R chain into a single monolithic microwave integrated circuit or module thereby reducing the cost as well as size weight and power (SWaP) of the phased array system [1.8]. Leveraging the maturity of integrated circuits, low cost, highly reliable phase array systems can now be designed and implemented for both military as well as commercial applications.

In the design of phased array systems, the phase shifter is the most essential element and is also the most difficult to design, especially when integrated on a single chip. Considering chip integration, the phase shifter represents a considerable portion of the overall system cost [1.3] and while the demand for phased array systems has been dominated by military applications that can absorb this cost, many commercial applications have recently emerged as discussed previously. In the case of on-chip integration, small circuits are favorable concerning costs and depending on the frequency of operation, different design techniques for the phase shifter should be considered. At lower Rf frequencies such as S- and L- band applications, some passive phase shifters require large inductors which consume a lot of chip real estate requiring alternative design approach. Some of the performance constraints and requirements for robust phase shifter design are 360° phase shift, adequate bandwidth, small size, low power consumption, low RMS phase and gain error, adequate linearity and unconditional stability. To meet these specifications at different frequencies, both active (provides gain to system) and passive phase shifters have been designed including reflective type phase shifter, tuned transmission lines, vector modulator type and switch filter. These types of phase shifters and more are briefly discussed in the next section.

**1.2 Brief Review of Previous Work**

Using coupled transmission-line elements, B.M. Schiffman [1.9], in the 1950's demonstrated the concept of broadband microwave phase shifters by designing a matched differential phase shifter. Several improvements based on the Schiffman method were subsequently reported during the years [1.10] – [1.18]. The Schiffman method consists of the use of parallel coupled transmission lines with one being the reference path and the other providing the required phase shift, determined by the length of the transmission line. In [1.10], improvements to the Schiffman original approach was obtained by using new forms of multi-section coupled lines. The

requirement of very narrow gaps between the lines provided to be troublesome using printed circuit board (PCB) technology. Reference [1.11] used a multi-section Schiffman phase shifter to achieve more than 90% bandwidth with very small phase ripple and good return loss. Again here, PCB fabrication technology limited the applicability of the design since it also required very narrow gaps as well as high impedance lines. The approach in [1.15] used a Schiffman phase shifter together with a network of switches implemented as transmission lines, to achieve broadband performance for 90° and 180° phase shifters at 3 GHz. A similar approach was used in [1.16] where a broadband 180° phase shifter was designed. This design used a different approach for the design of the switching network and included the use of coupled lines and parallel open and short circuit stubs. Measured performance showed a return loss of 14 dB with maximum phase deviation of 5° from 1.5 to 4.5 GHz. In [1.18] the use of open circuit and short circuit multi-section stubs presented a new approach to the design of a 45° phase shifter. The proposed design was much smaller in size with better bandwidth performance than its predecessors. Despite this smaller size, the use of passive components makes in impractical for chip integrations as the size would be excessively large.

The design of switched line, reflection type, loaded line and high-pass low-pass phase shifters using PIN diodes as switches was reported in [1.20]. In [1.21], improved bandwidth and larger phase shifts of these types of phase shifters was reported. Here, both constant phase shift as well as constant time delay performance was improved by eliminating resonance effects which negatively affect both amplitude and phase response. A reflection type 180° phase shifter was proposed in [1-24] that used both series and parallel LC circuits as well as a 3 dB Lange coupler. The design was implemented as a MMIC with a 180° phase shift from 0.5 to 30 GHz. The work reported in [1.25] used lumped element all-pass filters to design a C-band 5 bit MMIC. In [1.26],

a series cascade of all-pass filters is used to develop a full 360° MMIC phase shifter by implementing thin film BST varactors, resulting in a low cost compact phase shifter. The authors in [1.28] presented a unique method of designing broadband phase shifters using networks of unbalanced all-pass filters in combination with single-pole double-throw switches (SPDT). Cascading two or more of these networks provided phase shifts with single- and multi- octave bandwidth. All-pass networks are suitable for RF applications at lower frequency bands since the transition frequency of the all-pass network can be at a higher frequency of operation. This in turn, results in smaller passive components especially for inductors which for MMIC applications translated into small chip area. The initial design in this dissertation is based on this design technique while the second part uses the initial design criteria to establish a baseline for the final active phase shifter design. More details on the design of passive all-pass phase shifter is presented in Chapter 3.

Various analog techniques using vector summation have recently been reported [1.29] – [1.35]. This technique achieves the desired phase shift by varying the amplitude of I/Q signals using variable gain amplifiers or attenuators. This approach lends itself quite suitable to integrated circuit applications because of its limited use of bulky passive components. At lower RF frequencies such as S- and L- band the necessary requirement for the generation of I/Q signals results in bulky R-C based lumped passive quadrature networks using either RC-CR or R-C polyphase filters which also have very limited bandwidth [1.29].

### 1.3 Motivation and Organization of the Dissertation

Studies and research on phase shifters generally focus on achieving high phase shift resolution with minimal phase error as well as low gain variation between the different phase states in as

wide a bandwidth as possible all while being as small as possible to minimize cost (chip real estate).

The purpose of this research is to improve on the design of broadband all pass phase shifters in the L- and S- frequency range and implement this in integrated circuit form in an effort to decrease the size of the phase shifters while providing minimal phase and amplitude errors for phase shifts from 0° to 360°. All design will be implemented in a 0.5 µm GaAs pHEMT process with both enhancement and depletion mode transistors. The challenge here is to realize a phase shifter capable of providing 360° phase shift with good performance metrics while occupying a small chip size which can be a problem at the lower S- and L- band frequencies. Using techniques implemented in both board level and integrated circuit designs two design approaches are introduced. The first consists of the design of passive all-pass phase shifters and wideband amplifiers implemented in a 4-bit system with each bit consisting of 3 separate sections of all-pass filters to achieve a full 360° phase shift. The second design technique uses a different approach to the first. Here, an active tunable inductor together with a broadband active balun and variable gain amplifier is designed to achieve a similar function to the passive all-pass network of the first design resulting in a very compact and tunable phase shifter capable of achieving 360° phase shift with good input and output match and low RMS gain and phase error and occupying ¼ chip size of first design.

The main achievements of this work include:

- A 1.5 GHz to 3 GHz wideband active balun/180° phase shifter with switchable outputs and stable input match. It has a gain error of less than 0.3 dB and phase error of less than 2° across the entire frequency range. Design implemented in 0.5 µm GaAs process.

- Wideband 1.5 GHz to 3 GHz two stage variable gain amplifier/buffer using switchable resistor network for gain variation from 10 dB to 15 dB at mid-band with stable output match. Design also implemented in 0.5 µm GaAs process.
- Novel all-pass phase shifter using active tunable inductor to achieve tunable phase shift up to 180° with a single stage at s- and L- band and occupying ¼ chip size of a similar phase shifter using passive components to achieve similar functions. Design was also implemented in 0.5 µm GaAs process.
- A complete S- and L- band phase shifter capable of achieving full 360° phase shift using components listed above with a chip size 0f 2.7 x 4.5 $mm^2$ including all bias lines and bondpads. Measured results show a gain of 10 dB, RMS phase error < 9, RMS gain error < 1.5, power consumption of 78 mW, P1dB of 12 dBm at mid-band and fractional bandwidth of 67%.
- All designs described about use techniques that can easily be implemented in cheaper silicon process.

The dissertation consists of 6 chapters. Chapter 2 covers phase shifter fundamentals that include a basic explanation of phase shifter, phase shifter architectures and performance requirements. Having discussed the different phase shifter architectures, the passive all-pass architecture was selected as the best choice for the current application because of its inherent match to 50 Ω and wideband performance. Chapter 3 then goes into more details about broad-band all-pass phase shifter design, discussing the all-pass filter design theory and its implementation in the design of phase shifters. It then details the design of a broadband all-pass passive phase shifter implemented in 0.5 µm GaAs process. However, the fabricated prototype fails to perform with full functionality due to the excessive number of passive inductors in the design and the resulting mutual coupling.

The mutual coupling issue could be solved by spacing out the layout to allow more separation among the inductors. Unfortunately, in the S- and L-bands, this is not an option for this research work as the fabricated design already uses the maximum allowed chip size as determined by the foundry. Chapter 4 details a different approach to the problem and goes into details on the design of active inductors using gyrator networks. Detailed design techniques are presented into the design of a floating active inductor. Chapter 5 implements the active inductor designed in the previous chapter into an active all-pass phase shifter using the same knowledge presented in chapter 3 for the design of broadband phase shifters. The conclusions and recommendations are then discussed in Chapter 6.

### 1.4 Technology Overview

The technology utilized for the circuits developed in this work was provided by Triquint (Qorvo). The TQPED GaAs process is a 150mm, 0.5 μm, pHEMT process with both depletion and enhancement mode pHEMTs. This process is targeted for high efficiency and linearity in power amplifier, high linearity and low loss in RF switch, low noise in low-noise amplifier applications.

The standard TQPED process offers a D-Mode pHEMT with a –0.8 V pinch off and an E-Mode pHEMT with a Vp of +350 mV. The three metal interconnecting layers are encapsulated in a high performance dielectric that allows wiring flexibility, optimized die size and plastic packaging simplicity. Precision NiCr resistors and high value MIM capacitors are included allowing higher levels of integration, while maintaining smaller, cost effective die sizes.

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## Chapter 2:

## Phase Shifter Fundamentals

### 2.1 Introduction

Phase shifters, in a simple way, can be described as a two-port device that changes the phase of the input signal with minimal amount of attenuation. In reality, phase shifters will have some amount of attenuation associated with the phase shift. This will depend on the type of phase shifter used, being either active or passive. Figure 1 shows a general two port network functioning as a phase shifter [2.1]. The output signal at port 2 is a combination of the input signal $V_1$ with the additional phase shift denoted by $e^{-j\theta}$ with the phase shift being $\theta$. In this ideal case, the signal does not experience any gain attenuation.

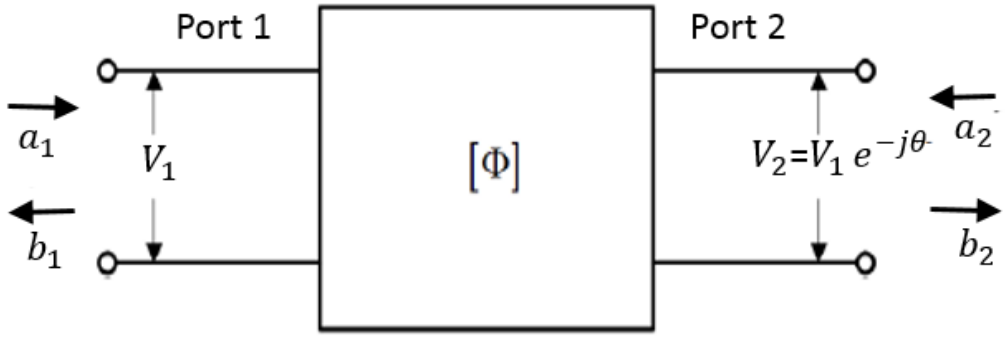



Figure 2-1. Block diagram of a phase shifter

The scattering matrix for the ideal two port phase shifter is given by:

$$\begin{pmatrix} b_1 \\ b_2 \end{pmatrix} = \begin{pmatrix} 0 & e^{-j\theta} \\ e^{-j\theta} & 0 \end{pmatrix} \cdot \begin{pmatrix} a_1 \\ a_2 \end{pmatrix} \tag{2.1}$$

The insertion phase of the signal is the phase of $S_{21}$ and the phase shift always has to be referenced to an initial state or it is meaningless and the phase shift of the signal will always be in comparison to the reference state. The phase shift ranges from $0^0$ to $360^0$ for complete rotation.

In practical applications insertion loss (or gain) will be experienced by the signal. The loss in dB is again derived from the scattering parameters as:

$$IL(dB) = 20\log_{10}|S_{21}| \tag{2.2}$$

In the design of phase shifters, phase performance is generally related to the insertion loss and used as a figure of merit when describing the performance. Insertion loss can be overcome with additional amplification in applications such as military radar where both phase and gain error are very important but comes at the cost of increased power consumption. In other systems such as automotive radar, a trade-off with power consumption can be made. In general, some of the most critical parameters of phase shifters are $360^0$ phase shifting capability, insertion loss, amplitude variation, third-order intercept point (IP3), return loss, linearity of control function, power consumption and chip size for IC applications. Insertion loss is largely driven by the number of stages necessary to achieve a certain bandwidth as well as the topology used. Amplitude variation relates to phase shift and is the variation in insertion loss for different phase shift values. IP3 is a measure of linearity for the phase shifter while return loss shows how good of a match the input/output of the phase shifter is, typically in reference to 50Ω. Return loss plays a less important role for phase shifters implemented on chip as part of a system where its input/output are not directly interfacing with the 50 Ω outside world. Linearity of control function is the relationship between the control voltage and the corresponding phase shift values. Ideally this would be a linear relationship for passive phase shifters but is usually non-linear for active devices as transistor change states from cutoff to saturation.

## 2.2 Types of Phase Shifters

Phase shifter may be analog or digital depending on the type of control that sets the different phase states. These can be either electric or mechanical control, based on the tuning mechanism used. Electronic phase shifters use electronic components to control the phase response. These include voltages and currents and have a much faster response than mechanical methods [2.1]. Mechanical phase shifters on the other hand are generally constructed using transmission lines structures in combination with some means of manual tuning to achieve the desired phase shift response.

Electronic phase shifters can be put into two major categories based on how they are controlled. Digital phase shifters are only able to achieve discreet phase shift values that depend on the resolution or number of bits and are controlled by set voltages. The idea behind digital phase shifters is to switch the signal between some reference path and some desired phase shift path with the phase shift being the difference. These require only digital voltages to control the switching paths which are usually done using electronic switches such as transistors or diodes. There are several ways of creating a phase shift bit using this approach. Continuous phase shifters vary the phase in a continuous manner and are capable of achieving any desired phase shift value within the tuning range with the appropriate applied tuning voltage. Continuous phase shifters are very popular especially for on-chip applications and are capable of achieving $360^0$ phase shift. The control voltages for these types of phase shifters are usually implemented using multibit DAC for greater accuracy and ease of calibration. The discussion from this point onward will only include electronic phase shifters, both digital and continuous.

### 2.2.1 Switched Line Phase Shifter

The Switch Line Phase Shifter uses different line lengths as alternate the signal paths controlled by switches as shown in Figure 2 [2.2]. The difference in time delay between the two paths accounts for the phase shift where the time delay (in seconds) for a given line of length $L_o$ is $\tau_D = \frac{2\pi L_o}{v_p}$. The phase shift (in degrees) can be derived from the line length difference between the reference and modified lines. Given a difference in length $\Delta L$, the time delay becomes $\Delta\tau_D = \frac{2\pi\Delta L}{v_p}$ where $v_p$ is the phase velocity.

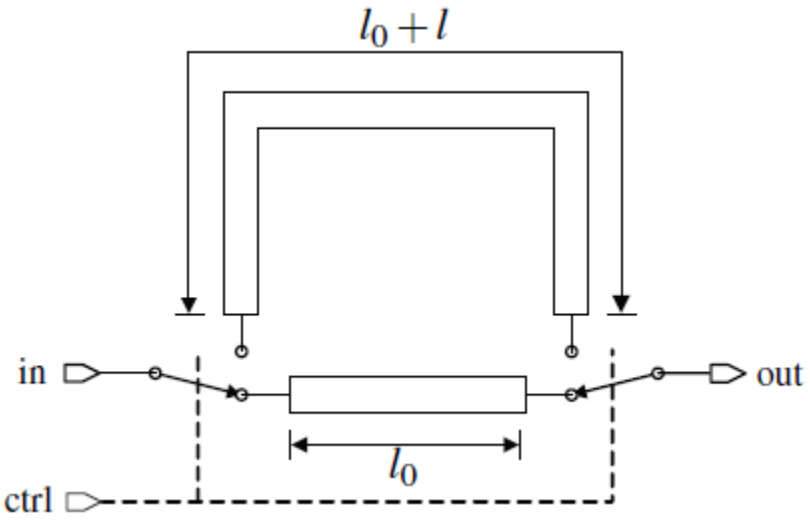



Figure 2-2. Switch-line phase shifter

One of the major advantages of switched line phase shifters is that the phase shift is wideband which avoids or minimizes bean squinting in wideband arrays. For low GHz applications, this architecture is quite bulky and suffers from variations in attenuation between the two paths because of the varying line lengths. Loss can become significant and therefore not ideal for applications that require SWaP (size, weight and power) performance.

### 2.2.2 Reflection Type Phase Shifter

Reflection type phase shifter use the directional properties of a 3-dB hybrid coupler (Fig 2-3a) or of a circulator (Figure 2-3b) [2.3]. In the 3dB 90º hybrid coupler the power incident at the excitation port gets divided evenly to thru port and coupled port with 90° phase difference. Based on the state of the switch, the two parts are either reflected back and recombine at the output port or travel on the *l*/2 transmission line and are reflected back having travelled an additional *l*/2 length before being recombined. Since the total traveled length is *l*, the time delay that the signal is subject to is provided by $\tau_D = \frac{2\pi L_o}{v_p}$. Either PIN diode or FET switching may be used for digital phase shift operation. A reflection type phase shifter with a very compact termination circuit is reported in [2.4].

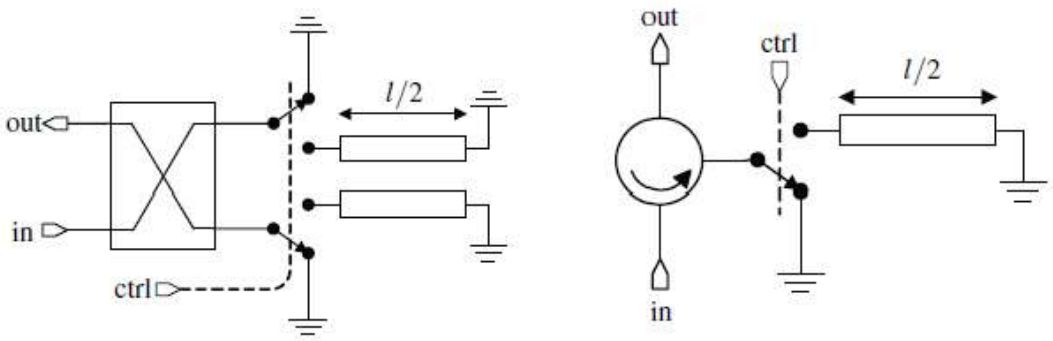



Figure 2-3. Reflection type phase shifter (a) hybrid, (b) circulator

### 2.2.3 Loaded Line Phase Shifter

In loaded line phase shifters, instead of using varying line lengths to achieve the phase shift as in the previous two techniques, phase difference is created by changing the propagation characteristics of the transmission line by switching between shunt susceptance or series reactance as it is seen in Figures 2-4.a and 2-4.b [2.1]. This is done by manipulating the characteristics of the transmission line which are composed of a quarter wavelength transmission line with both ends terminated by either an inductive or capacitive load. The drawback with the use of quarter

wavelength lines is that it limits the useful bandwidth of this design. As the phase shift values increase, quality of the input match degrades so it is not applicable for requirements that call for large phase shifts or large bandwidth.

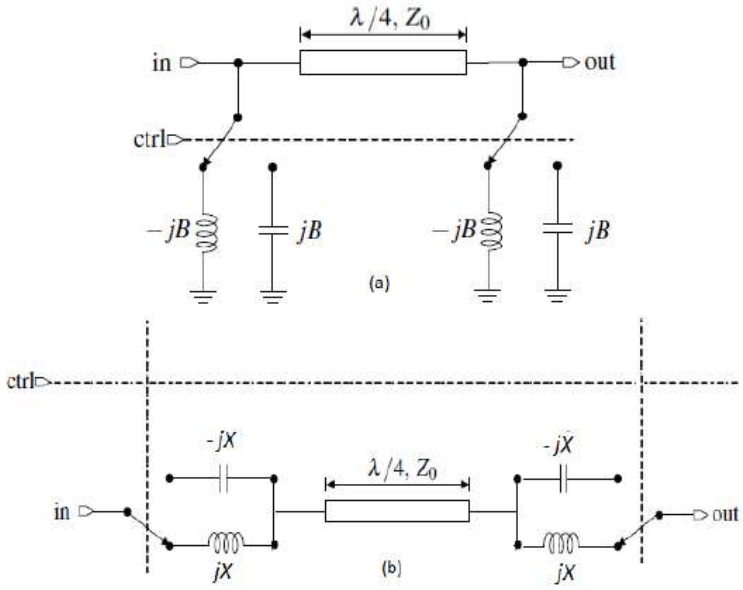



Figure 2-4. Loaded-line phase shifter

### 2.2.4 High/Low Pass and All Pass Phase Shifter

A high pass passive network in parallel with low pass network (HPF-LPF) (Fig. 2-6)[2.4] as well as two parallel all pass filter networks (APF) (Fig 2-7) [2.5] can be used to design phase shifters which are based on filter networks and are popular switching phase shifter topologies with similar operation principles. This type of phase shifter uses circuits which only require "digital" control voltages used to control SPDT switches to switch between two paths, these being the high pass path and the low pass path or between all pass filters path as shown in Figure 2-5. One path becomes the reference path and the other the phase shift path. The desired phase shift is the phase difference between the reference and phase path. High pass filters provide a phase advance, while the opposite can be said for the low pass filter, giving a phase delay. Both HPF-LPF and APF

topologies exhibit good return loss characteristic which allows for easy tuning over the desired phase shift performance. Overall insertion loss and chip size increase with increasing phase shift resolution as these require more networks in cascade. This architecture has been implemented on chip because of its small size and flat phase response at high frequencies (> 5 GHz) but become bulky at lower frequencies which require higher values of inductors in implementing the filters.

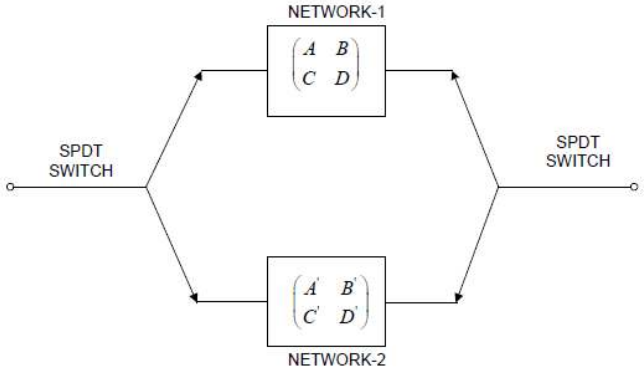



Figure 2-5. Phase shifter with switching elements

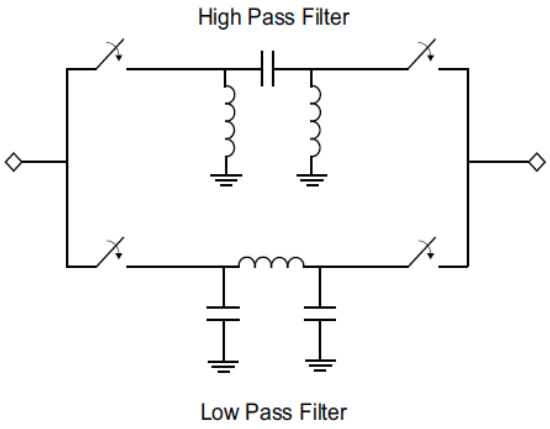
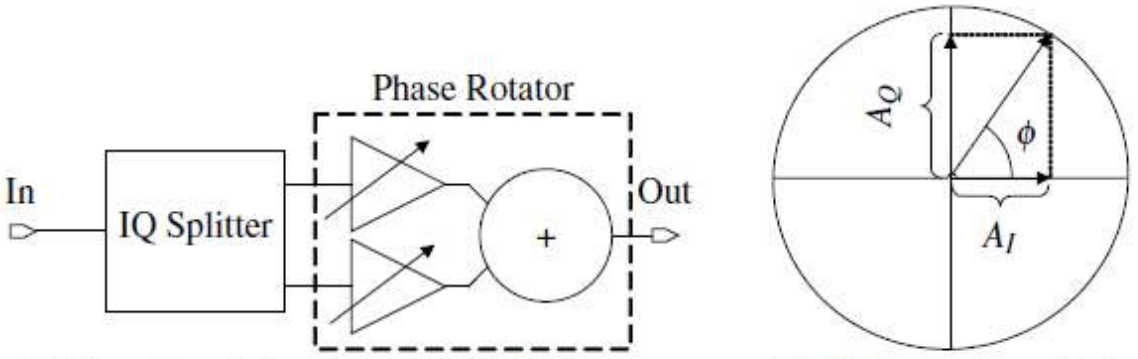



Figure 2-6. High pass/low-pass network

### 2.2.5 Vector Modulators

All the phase shifters described previously can be classified as digital since these only provide discrete phase states. Continuous phase shifters may be attractive for on-chip applications that

require a full $360^0$ phase shift with high resolution. The control voltages for these types of phase shifters are usually implemented using multibit DAC for greater accuracy and ease of calibration. Vector Modulators (Fig. 2-7a) form a continuous type of phase shifter capable of achieving $360^0$ phase shift [2.6] – [2.7]. Also called a phase interpolation phase shifter, it functions by splitting the input signal into two equal amplitude signals that are ideally 90° apart in phase. The two signals are then amplified by two variable gain amplifiers (VGAs) and then summed, forming the output signal. The phase shift is determined by the gain of the two VGAs which are independent of each other. Using this approach, phase between 0° and 360° can be achieved. The weighted summation of the I and Q components used to form the resultant phase shift is shown in Figure 2-7b. This type of architecture is quite common for integrated circuit implementation because of it's extensive use of active components. One major drawback of this approach is the exceptional accuracy and complexity required of the amplitude control components to minimize the RMS phase errors which in turn requires complex control circuitry to ensure precision of the phase shift. Apart from this, operation at lower RF frequencies results in bulky passive I/Q splitters that may not be able to be integrated on chip.




(a) Phase interpolation phase shifter block diagram. (b) I-Q phase vector synthesis.

Figure 2-7. Vector modulator phase shifter

### 2.2.6 Periodically Loaded Transmission Line

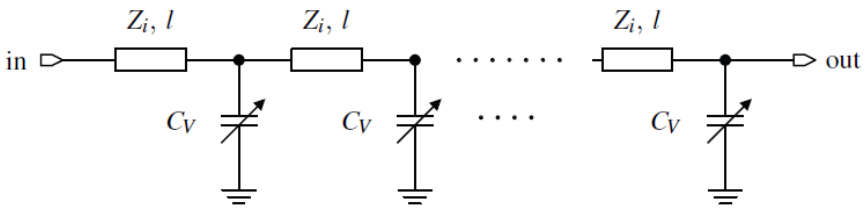



Figure 2-8. Periodically loaded line phase shifter

Tunable transmission lines can be used as phase shifters. The lumped element equivalent circuit of the periodically loaded line phase shifter is depicted in figure 2-8 [2.8] and is composed of series transmission lines and shunt varactors. Tuning the varactors causes the characteristics of the transmission line can also be varied. If a unit cell of the artificial transmission line is assumed to have characteristic impedance *Zi* with a corresponding phase velocity *vi* and length *l*, then the equivalent inductance and capacitance of each section is given as:

$$L_t = \frac{lZ_i}{v_i} \tag{2.3}$$

$$C_t = \frac{l}{Z_i v_i} \tag{2.4}$$

By varying the capacitance of the line using the varactors, the characteristics of the artificial line change and the phase shift becomes a function of the varying capacitance as:

$$\Delta\emptyset = 2\pi f \frac{i}{v_p}\left(\sqrt{1+x} - \sqrt{1+xy}\right) \tag{2.5}$$

$$x = \frac{C_{v\_max}}{C_t}$$

$$y = \frac{C_{v\_min}}{C_{v\_max}}$$

The lumped element equivalent circuit implementation is preferred as it is smaller than the transmission line and this can be implemented as low-pass or high-pass structures using lumped inductors and varactors. Cascading several sections can increase the phase resolution at the cost of higher insertion loss but can achieve 360° phase shift.

### 2.2.7 Integrated Switches

The use of switches in the realization of phase shifters such as those described previously in sections 2.2.1-2.2.4 becomes very important for phase shifter performance in particular that associated with insertion loss. Most switches used in these examples rely on FET technology to achieve the switching function. By means of gate voltage, the channel conductivity of the FET can be controlled while consuming no DC power. Varying the channel resistance $R_{DS}$ the FET as a switch, can either be turned OFF or ON. In other words, the channel resistance behaves as a voltage variable resistor. Figure 2-9 below shows the equivalent circuit of a FET used as a switch. Typical performance metrics of a switch are it ON resistance and OFF capacitance which are determined by the process used and the size of the FET. These have a direct impact on the undesired insertion loss in ON state and high frequency isolation in the OFF state.

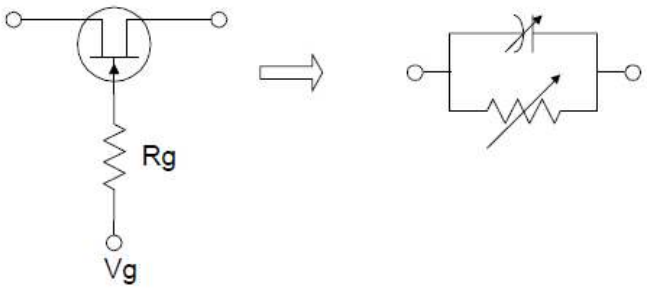



Figure 2-9. Equivalent circuit of a FET operating as a switch

Several different circuit topologies exist for switch implementation with the two most common being the single-pole-double-throw (SPDT) series switch and the SPDT series-shunt switch. The simplest of these is the series switch as shown in figure 2-10 which uses only a single series FET

in each arm with complimentary voltages V1 and V2 controlling each switch. When the switch in one arm turns ON, the other arm turns OFF. As mentioned before, switch performance is determined by FET size used in the switch. Figure 2-11 shows a another variation of the SPDT switch where instead of just a series switch in each arm, it used a combined series and shunt switch. The additional shunt switch improves the isolation in the OFF state but also makes the insertion loss in the ON state worse. Depending on the application, one or the other could be used.

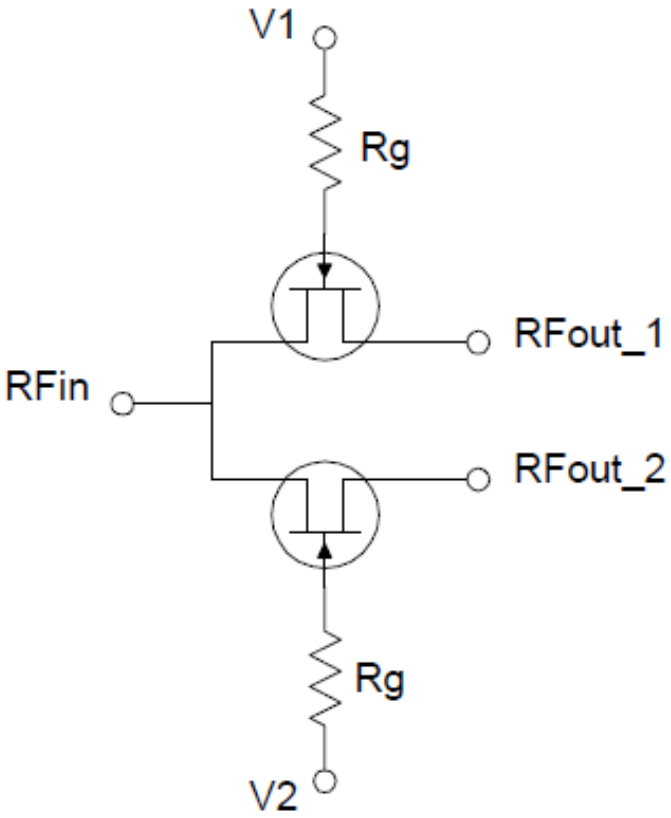



Figure 2-10. SPDT switch using series FETs

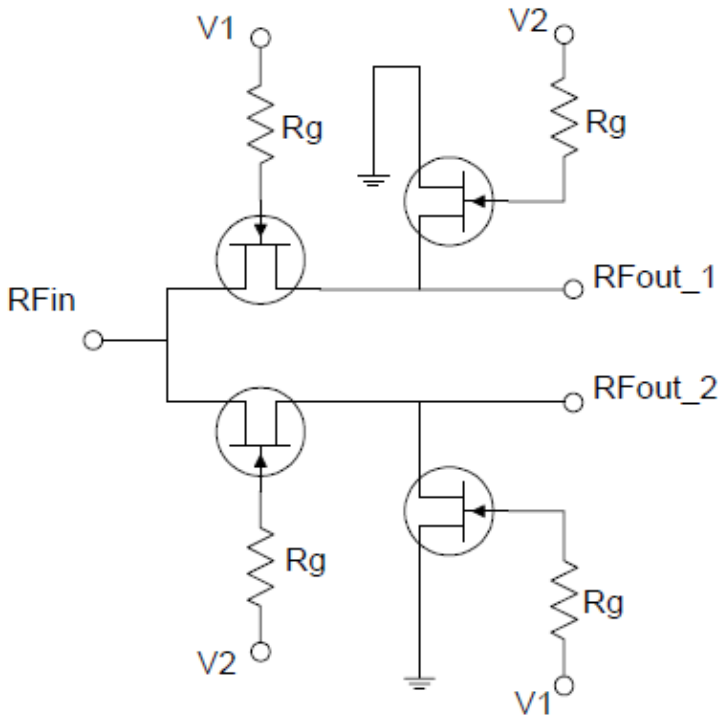



Figure 2-11. SPDT switch using series-shunt FETs

### 2.3 Phase Shifter Requirements

The main technical requirements used to describe the electrical performance of phase shifters are listed below and each is briefly explained. Different applications will have different emphasis on certain aspects of these requirements enforcing some more than others. These include Phase shift error, amplitude imbalance, return loss, insertion loss, number of bits, operating frequency band and design size.

#### 2.3.1 Phase Shift Error

Phase shift is the phase difference between insertion phases of reference and difference paths and is desired to be constant over the operating bandwidth. Design efforts always have to deal with a certain amount of phase error in the operating bandwidth with the limits set at the system level and depend on the type of application with military being less tolerant than commercial.

In the performance of digital phase shifter, the phase error cannot be larger than the phase resolution and the intersection of two adjacent phase states is usually unacceptable. This occurs when either or both adjacent phase states have too much variation in the operating bandwidth.

Sources of phase error may originate from input power variation, temperature variation, transistor or device mismatch etc. RMS phase error definition is the most common way of reporting or documenting phase error even though peak to peak phase error is also used.

### 2.3.2 Amplitude Imbalance

In ideal conditions, the magnitude of the phase shifted signal should remain constant and not be affected by the phase shifter. In reality, the effect that the phase shifter has on amplitude will vary between the reference state and the phase shift state. This difference is what is referred to as amplitude imbalance and is desired to be as small as possible. RMS gain error definition is the most common way of reporting or documenting gain error between the reference state and phase shift state.

### 2.3.3 Insertion Loss

The magnitude of insertion loss depends on the requirements of the system and is not a desired property which in reality is quite difficult to avoid especially in passive phase shifters. It is a measure of transmission losses (signal loss) that are created by component loss, impedance mismatches and conductor losses, etc. which causes a decrease in system signal-to-noise ratio (SNR) and may increase amplification requirement leading to added power consumption. In digital phase shifters, higher resolution systems require more bits leading to higher insertion loss since phase shifter bits are usually implemented in a cascaded form. Amplifiers can be used to compensate for insertion loss in passive phase shifters.

### 2.3.4 Return Loss

Phase shifters are usually implemented as part of more complicated RF systems and return loss is a type of loss that is caused by the impedance mismatches at the input and output ports where the phase shifter connects to other components in the system. Bad return loss usually makes the insertion loss worse since it causes some amount of applied power to be reflected back to the source, decreasing both components as well as system gain and decreasing SNR. Both input and output return loss result in amplitude and phase distortions in the system response and negatively affects cascaded system performance. The return loss of the phase shifter should be kept as low as possible so as not to cause any disorder in system level performance as well as increases in insertion loss.

### 2.3.5 Number of Bits

The minimum phase shift angle that can be performed with a phase shifters is referred to as the phase resolution and is determined by the number of bits in the system. Sensitive analog phase shifters on the other hand can scan all angles in small phase shift steps determined by the accuracy of voltage leveling circuitry within the system. For digital phase shifters, it is meaningless to design a phase shifter that has more phase error than its phase resolution although, in theory, it is possible to increase the phase resolution infinitely. In phased array applications, high phase resolution plays a dominant role in good beam steering resolution and the ability to achieve small side-lobe levels. The limiting factor on this on the other hand is that increasing the phase resolution may increase the insertion loss, cost, size and complexity of the circuit.

### 2.3.6 Operating Frequency Band and Device Size

Operating frequency band defines the bandwidth of the system and plays an important role in the decision as to what type of phase shifter is needed. It is the initial design parameter that defines lower and upper frequencies of operation with all other performance requirements tailored to be satisfied within the operating frequency band. At MHz and low GHz frequencies, passive components tend to be larger and therefore a preference for active phase shifters, while at higher frequencies, passive design of phase shifters are more common. Size, weight and power (Swap) play an important role in phase shifter design especially for those used in military applications. Phase shifters should be designed to be compact and able to be integrated in applications like expandable jammers where there is little room for every RF component.

## 2.4 Summary

There are numerous other types of phase shifter, but the most common and widely used types have been presented above. A general description of each type was given, listing both advantages and disadvantages. Depending on the application and the specifications, one of these architectures could be used. Furthermore, some of the most important design parameters were listed with a brief description of each. The initial choice of type of phase shifter needed for a specific design is crucial to satisfy the design specifications or to, at a minimum, reach a satisfactory tradeoff between specifications. Some of the most critical design requirements for phase shifters are accurate phase variation up to 360°, low RMS phase and gain error, low loss, size (die form), good input/output match and low control complexity all over required bandwidth. Based on the information presented above, the all-pass phase shifter was chosen as the work horse for the design of the phase shifter detailed in this dissertation. The advantages of the all-pass phase shifter include ability of achieving large phase shift, excellent return loss and low loss variation between

states over a wide bandwidth. Ability of cascade multiple stages for wider bandwidth makes it architecture a good choice for broadband phase shifters. Achieving 360° of phase shift is possible as phase shift of individual stages can be summed directly.

## 2.5 References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# Chapter 3:

# All-Pass Phase Shifter Design

## 3.1 Introduction

Phase shifter topologies such as those using switched networks [3.1], [3.2], reflection types [3.3], [3.4] and vector summation networks [3.5], [3.6] aim to achieve broad bandwidth performance with minimal phase error and return loss. In these conventional designs, the value of the phase shift is dependent on the return loss of the system [3.2] which therefore sets a limit on the operational bandwidth of the phase shifter. The design requirements in this chapter call for wide bandwidth (0.8 GHz to 3 GHz) with good input and output match and low phase and gain error. All pass networks are matched naturally over large bandwidths which makes the synthesis of its phase response much simpler to achieve. For wider bandwidths, the all-pass networks can be cascaded which makes it relatively easier to combine single and multi-octave responses [3.7]. In designing the phase shifter both the phase response and the return loss should be considered simultaneously. In cascaded systems, the matching conditions between the cascaded stages plays an important role in the performance of the phase shifter since this plays a role in the overall return loss. When properly designed to have large return loss this allows individual stages to be summed directly. The total phase of the cascaded system of bits becomes the sum of the individual bits and the design requirement may be simplified to that of simple phase summation [3.8]. The good match between stages also makes it more feasible to integrate amplifiers between the stages to provide gain to the system and compensate for losses incurred in the all-pass network.

### 3.2 All-Pass Filter Design Theory

The all-pass filter forms the core of the all-pass phase shifter design and will be described briefly. The two most common types of all pass filters (passive) are the series-L and series-C networks as shown in Figure 3-1. These networks are said to be matched naturally, if the following condition is met;

$$Z_o = \sqrt{\frac{L}{C}} \tag{3.1}$$

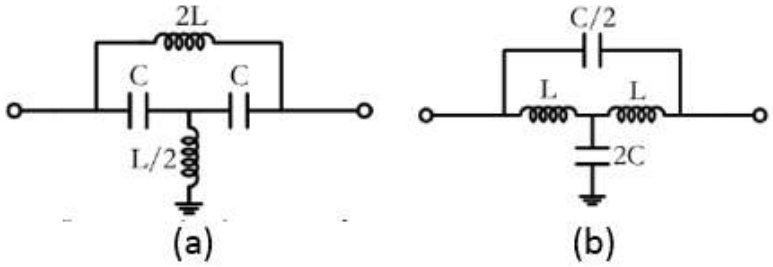



Figure 3-1. All pass filter in series L (a) and series C (b) configuration

where, C and L are the values of the passive component used in the design of the filter. Both networks have equivalent phase responses.

In the following analysis of the all pass filter, the associated reactance is expressed as $x = {\omega L}/{Z_0}$ and susceptance as $b = \omega C Z_0$. The normalized impedance z and normalized frequency Ω are expressed as:

$$z = \frac{1}{Z_0}\sqrt{\frac{L}{C}}\,, \quad \Omega = \frac{\omega}{\omega_0}\,, \ where\ \omega_0 = \frac{1}{\sqrt{LC}} \tag{3.2}$$

The single section all-pass phase shifter network is shown in Figure 3-2. To achieve a phase difference, the first network shifts the transition frequency from $\omega 0$ to $\omega 1$, and the second network from $\omega 0$ to $\omega 2$ with the relation

$$\frac{\omega_1}{\omega_0} = \frac{\omega_0}{\omega_2}$$

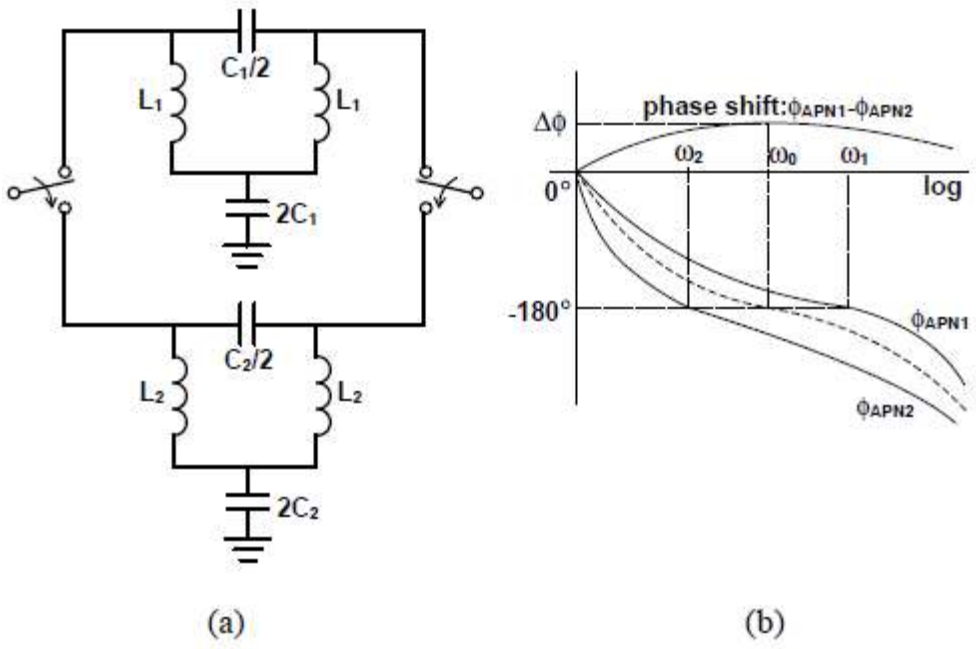



Figure 3-2. Single section all pass phase shifter [3-1]

At frequencies below $\omega_0$ the phase response of the network is similar to that of a low-pass filter (LPF) while for frequencies above $\omega_0$ it approximates that of a high=pass filter (HPF). Redefining the reactance and susceptance as:

$$x = \Omega z \; and \; b = \frac{\Omega}{z} \tag{3.3}$$

It can be shown that $S_{11}$ and $S_{21}$ of the network in terms of reflection coefficients can be described by the equations:

$$S_{11} = \frac{1}{2}(\Gamma_e + \Gamma_o) \; and \; S_{21} = \frac{1}{2}(\Gamma_e - \Gamma_o) \tag{3.4}$$

where $\Gamma_e$ and $\Gamma_o$ are the even and odd mode reflection coefficients.

For the network to be matched at all frequencies, $S_{11} = 0$ which occurs when z = 1 which means that ${}^{L}/_{C} = {Z_0}^2$. The transmission coefficient $S_{21}$ under this condition, has a unity magnitude and a phase response gives as:

$$\psi = \pi - 2\tan^{-1}\left(\Omega - \frac{1}{\Omega}\right) \tag{3.5}$$

Given the choice of the two different configurations, these being the series-C and series-L, the series-C is preferred since this option reduces the use of additional inductor values. The inductor used in this configuration also has a smaller value than that of the series-L configuration which lends itself favorable for IC design since larger inductors occupy more die space.

**3.3 All-Pass Phase Shifter Design**

For a switch bit network consisting of all pass networks (APNs) as shown in Figure 3-3 with corresponding transition frequencies $\omega_A$ and $\omega_B$, the insertion phase as described in equation 3 of each network is gives as:

$$\psi_A = \pi - 2\tan^{-1}\left(\Omega_P - \frac{1}{\Omega_P}\right), \;\; \psi_B = \pi - 2\,tan^{-1}\left(\frac{\Omega}{P} - \frac{P}{\Omega}\right) \tag{3.6}$$

where $\omega_m^2 = \omega_A\,\omega_B$ is the geometric mean of the two frequencies and $\Omega$ is redefined as $\omega/\omega_m$ and the new design parameter $p = \sqrt{\frac{\omega A}{\omega B}}$. The phase difference between the two branches then becomes the difference between $\psi_A$ and $\psi_B$.

$$\psi_B - \psi_A = \; \emptyset = 2\left\{\tan^{-1}\left(\Omega_P - \frac{1}{\Omega_P}\right) - \tan^{-1}\left(\frac{\Omega}{P} - \frac{P}{\Omega}\right)\right\} \tag{3.7}$$

The parameter p in the above equation is associated with the differential phase at the center frequency $\emptyset_m$. The parameter p for a phase shift $\emptyset_m = \emptyset\ (\Omega = 1)$ is given as [3.7]:

$$p = \frac{1}{2}\tan\left(\frac{\emptyset_m}{4}\right) + \sqrt{1 + \frac{1}{4}tan^2\left(\frac{\emptyset_m}{4}\right)} \tag{3.8}$$

Given the equations above, the value of the reactive elements that form the two branches of the APN can be calculated using the following equations where the center frequency of operation is given as $\omega_m$. The values correspond to those shown in Figure 3-3 for a single section all pass phase shifter.

$$L_1 = \frac{pZ_0}{\omega_m} \tag{3.9}$$

$$L_2 = \frac{Z_0}{p\omega_m} \tag{3.10}$$

$$C_1 = \frac{p}{Z_0\omega_m} \tag{3.11}$$

$$C_2 = \frac{1}{pZ_0\omega_m} \tag{3.12}$$

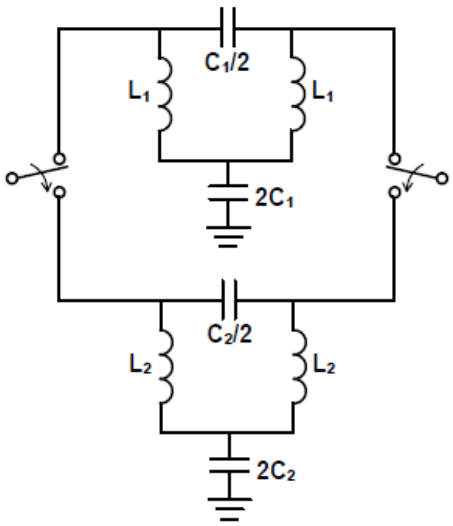



Figure 3-3. Topology of a single stage all-pass phase shifter

Using the above equations, a 4 bit phase shifter using the APN topology was designed for a frequency from 0.8 GHz to 3 GHz for a 3.75:1 bandwidth. Each bit in the sequence consists of three stages as shown in figure 3-4 below. Three stages per bit was found to be necessary in system

simulation to provide required phase shift over frequency from 0.8 GHz – 3 GHz. Figure 3-5 shows an example of the 90° phase shifter simulation setup. This was used to determine the number of stages necessary to achieve the phase shift across the frequency band of interest. Figure 3-6 is the schematic of a single section all-pass phase shifter centered at 1.9 GHz. Simulation results of this section and those of two more sections centered at 1 GHz and 3 GHz is shown in figure 3-7. Observing the response of each section separately, shows that it is insufficient to meet the requirements for the desired phase shift from 0.8 GHz to 3 GHz and therefore the necessity of three sections. Simulation results of the three combined sections is also shown in figure 3-7 and found to be an optimum tradeoff between bandwidth, insertion loss and chip size.

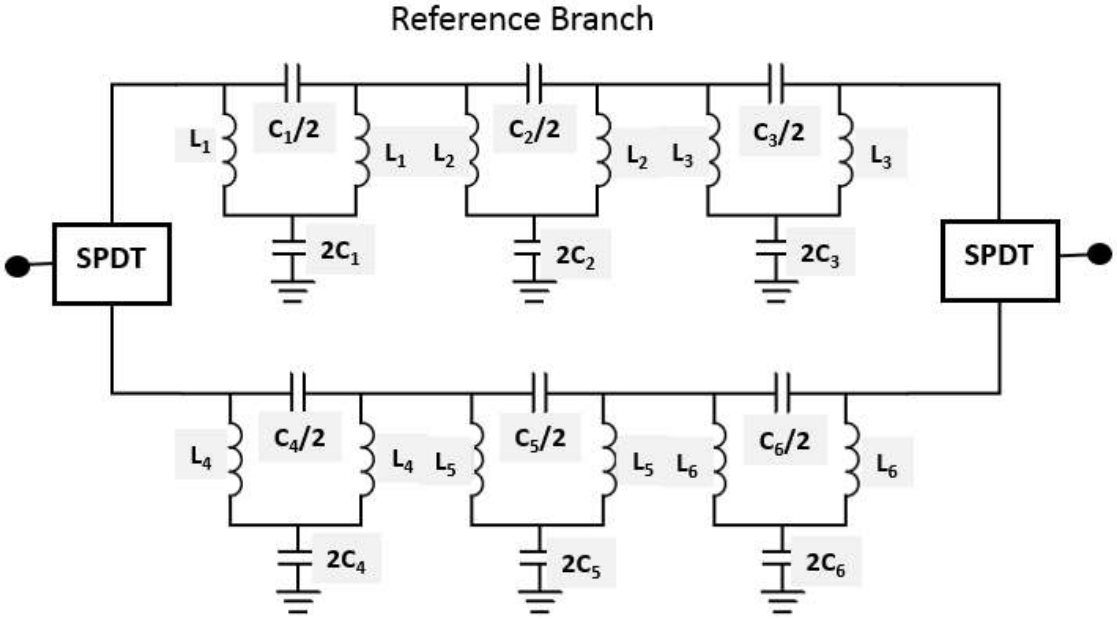



Figure 3-4. Topology of a single bit

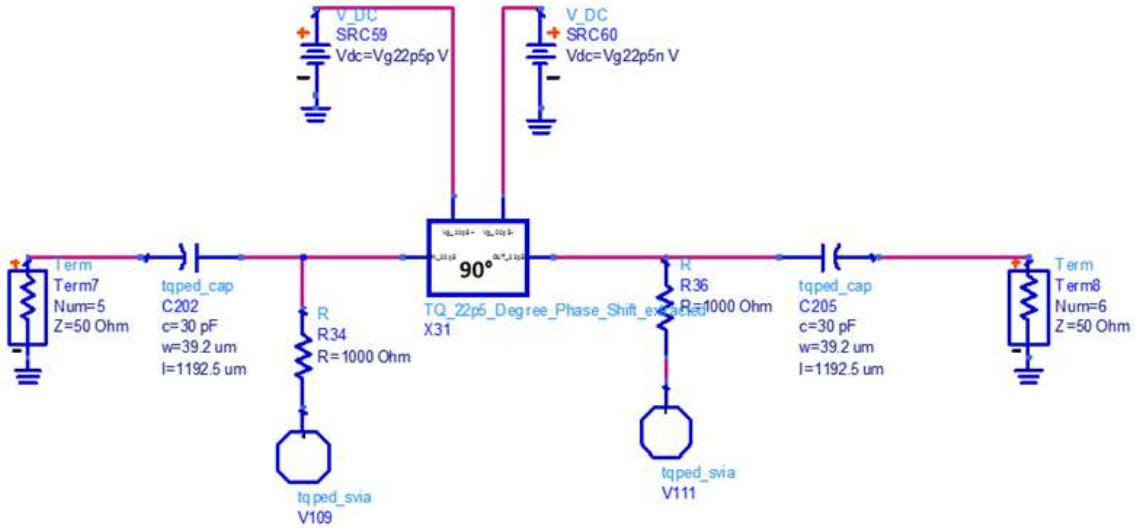



Figure 3-5. Simulation setup for 90° phase shifter

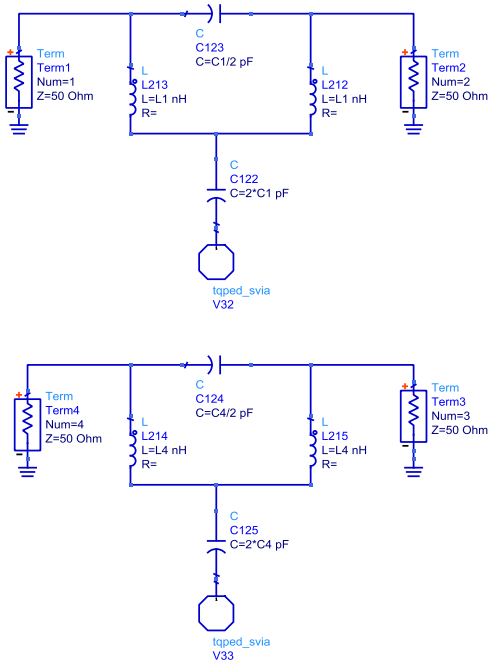



Figure 3-6. Single section 90° phase shifter at 1.9 GHz

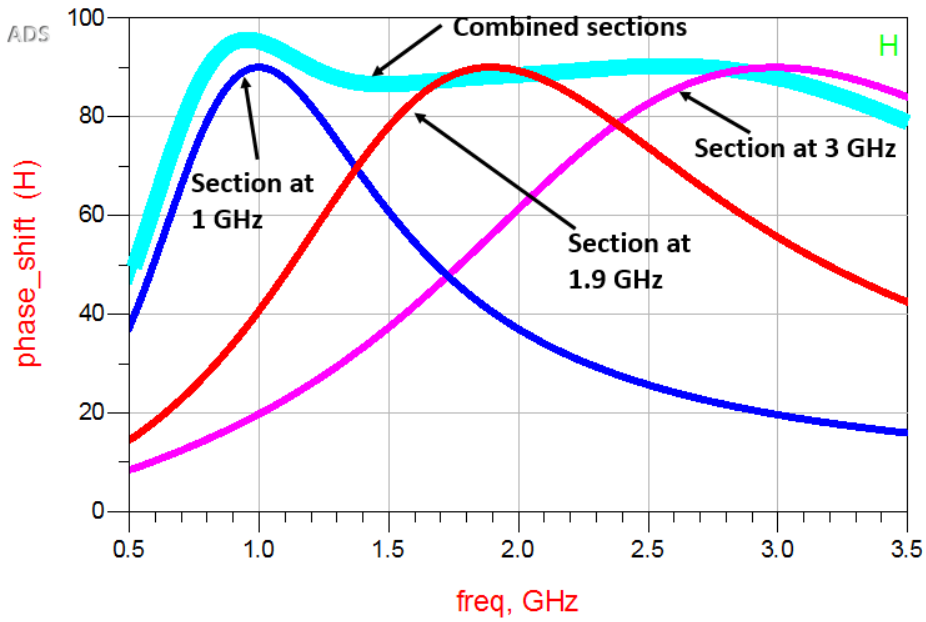



Figure 3-7. Simulation results of 90° phase shifter

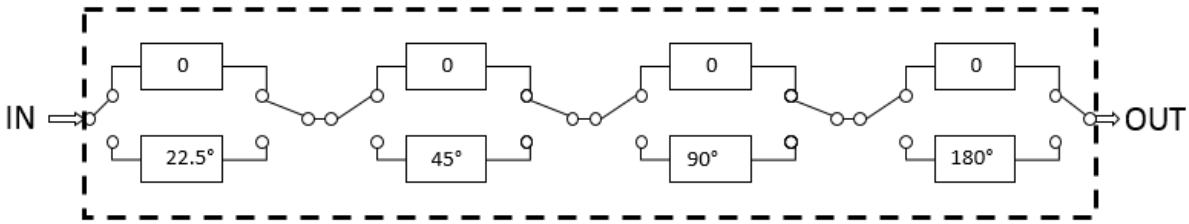



Figure 3-8. Block diagram of 4-bit phase shifter

The phase shift is the difference between the insertion phase of the reference branch and second branch. The signal is routed through the appropriate branch using single-pole double throw switches. After determining the center frequency for each section as shown in figure 3-7 to achieve a smooth phase shift across band from 0.8 GHz to 3 GHz, the component values are calculated using equations 3.8 to 3.12 and shown in Table 3.1. Table 3.1 list the values for the reactive components calculated for the necessary phase shifts of $22.5^0$, $45^0$, $90^0$ and $180^0$ as shown in figure above.

Table 3.1 Calculated LC Values (C in pF, L in nH)

| Components | Branch 1 (Reference) | | | |
|---|---|---|---|---|
| | $22.5^0$ | $45^0$ | $90^0$ | $180^0$ |
| L1 (nH) | **10.45** | **10.1** | **12.2** | **16.09** |
| C1 (pF) | **8.4** | **8.78** | **9.78** | **12.88** |
| L2 (nH) | **4.4** | **4.63** | **5.14** | **6.78** |
| C2 (pF) | **3.52** | **3.7** | **4.11** | **5.42** |
| L3 (nH) | **2.78** | **2.93** | **3.26** | **4.29** |
| C3 (pF) | **2.23** | **2.34** | **2.61** | **3.43** |

| Components | Branch 2 | | | |
|---|---|---|---|---|
| | $22.5^0$ | $45^0$ | $90^0$ | $180^0$ |
| L4 (nH) | **9.5** | **9.0** | **8.10** | **6.15** |
| C4 (pF) | **7.58** | **7.21** | **6.48** | **4.92** |
| L5 (nH) | **3.4** | **3.79** | **3.41** | **2.59** |
| C5 (pF) | **3.19** | **3.03** | **2.73** | **2.07** |
| L6 (nH) | **2.52** | **2.4** | **2.16** | **1.64** |
| C6 (pF) | **2.02** | **1.92** | **1.73** | **1.31** |

The design was done using Keysight's Advanced Design System simulation software. Figure 3-6 below shows the schematic of the 4 bit phase shifter. Individual bit performance is affected by the source and load impedance it sees and is therefore degraded by the loading of the adjacent bits. As a result, optimal bit ordering determined from simulation of different combinations, becomes necessary to keep the worse matched bits isolated from each other and placing them between the

better matched bits. The optimal bit ordering for this design is shown below in Figure 3-6. A schematic of the $22.5^0$ phase shifter using component values listed in Table 3.1 is shown in Figure 3-7. The schematic includes series/shunt switches at the input and output to switch from reference state to phase shift state as previously described. Inclusion of these switches further deteriorates the insertion loss of the network.

Simulation results of the entire 4 bit system is shown in Figure 3-8. It includes the four individual phase states, those being the $22.5^0$, $45^0$, $90^0$ and $180^0$ phases. Phase errors of less than $2^0$ are attainable across the entire frequency range. The available 16 states of this 4 bit

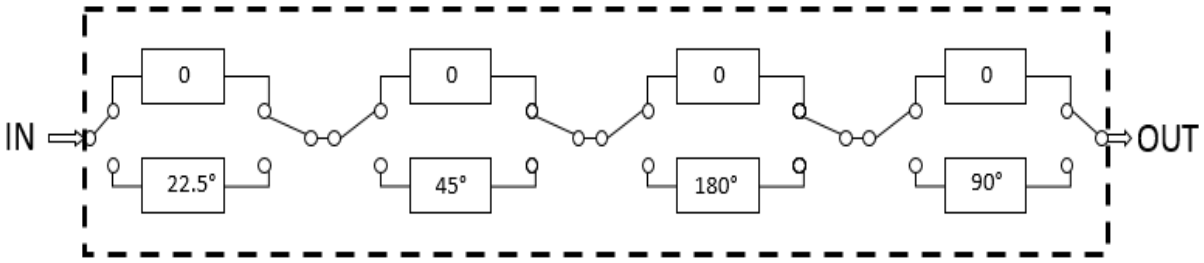



Figure 3-9. Optimal bit ordering

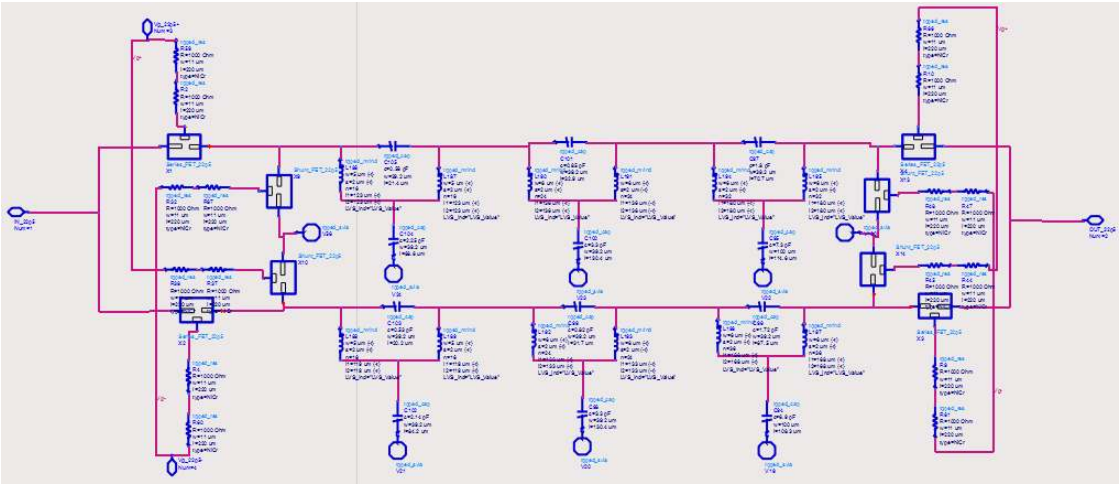


Figure 3-10. Schematic of $22.5^0$ phase shifter

system can be used to attain phase shifts of $360^0$ with a phase resolution of $22.5^0$. Figure 3-9 shows the insertion loss and return loss of the system. As discussed previously, the return loss of

this network is very good as the all-pass filter is naturally matched. Insertion loss on the other hand, with the inclusion of the switches is very high – from 9 dB to about 12 dB.

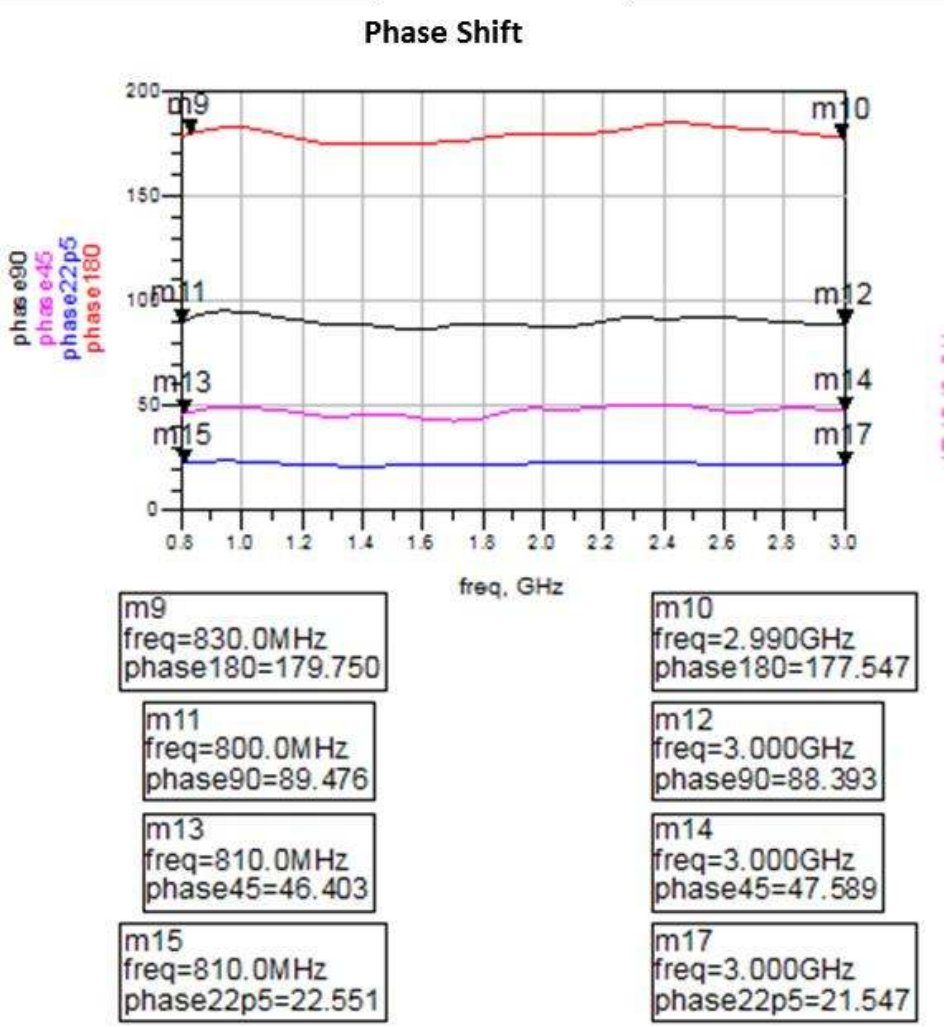



Figure 3-11. Simulated phase shift of 4 bit system

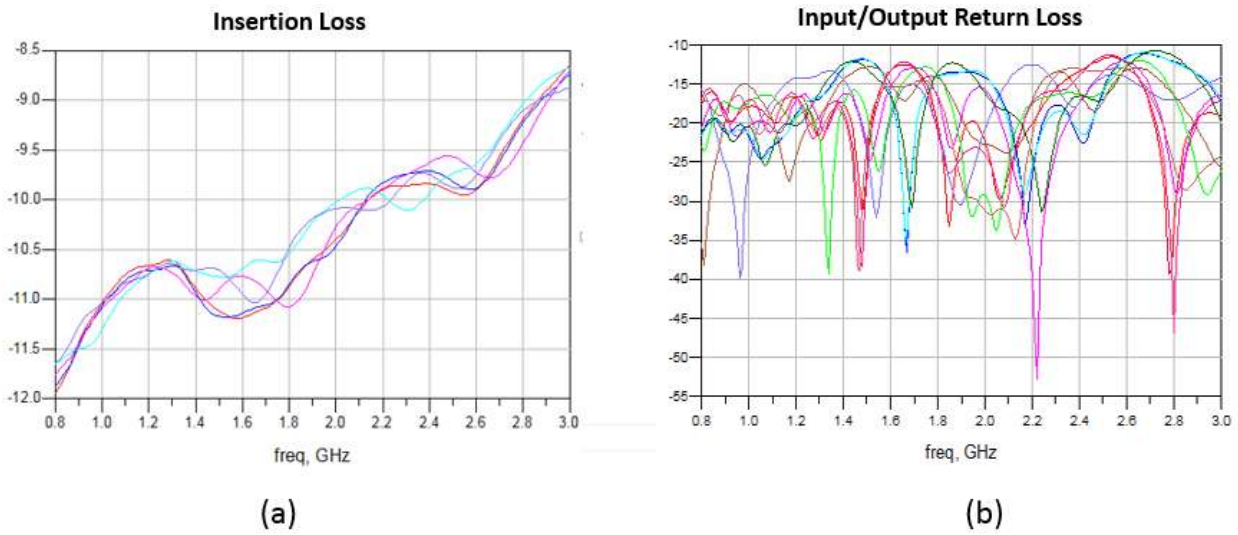



Figure 3-12. Simulated insertion loss (a) and input/output return loss (b)

To compensate for the loss in the network, wideband amplifiers were placed between the stages as shown in Figure 3-10 and 3-11. Apart from introducing gain to the network, these amplifiers provide stable source and load impedance to the phase shifters improving the individual bit performance. The amplifiers were designed as low noise wideband amplifiers using simultaneous noise and power match techniques [9]. Using noise matching by biasing the transistor using optimum noise current density for minimum noise and sizing it for power match, the transistor can operate at lowest noise possible while at the same time being matched for maximum power gain. Using this technique usually results in exceptionally large transistors but adding a small shunt capacitor between the gate and source terminals shrinks the necessary size while preserving the optimum noise match. The cascode architecture was used since it eliminates the miller feedback effect increasing the bandwidth and reverse isolation. It also increases the gain with a minor penalty in noise and linearity. Source inductors were used to match the input to the real part of the source (50 Ω) while a gate inductor was used to cancel the imaginary part of the input impedance. To increase the bandwidth of the design, RC feedback was used from the output buffer to the input. A simple schematic version of the design without biasing is shown in Figure 3-12.

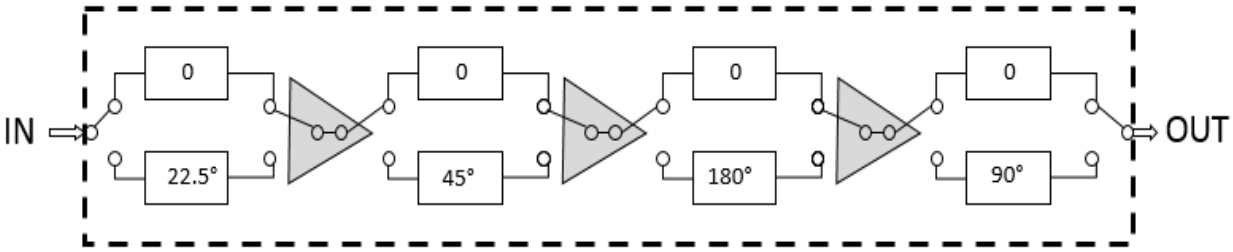



Figure 3-13. Concept of 4 bit phase shifter with amplifiers

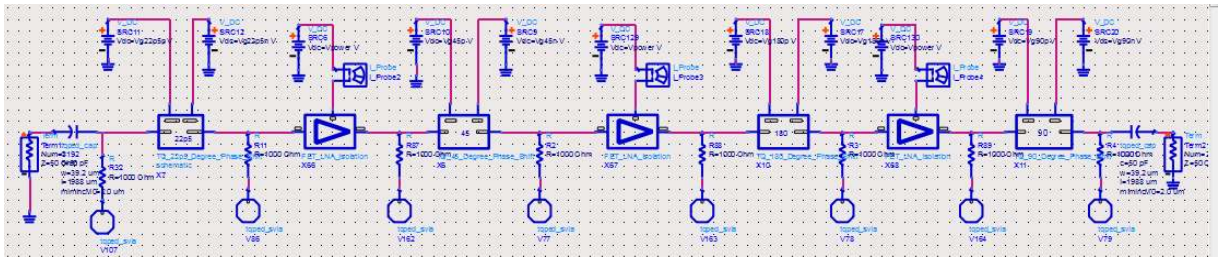


Figure 3-14. Schematic of 4 bit phase shifter with amplifiers

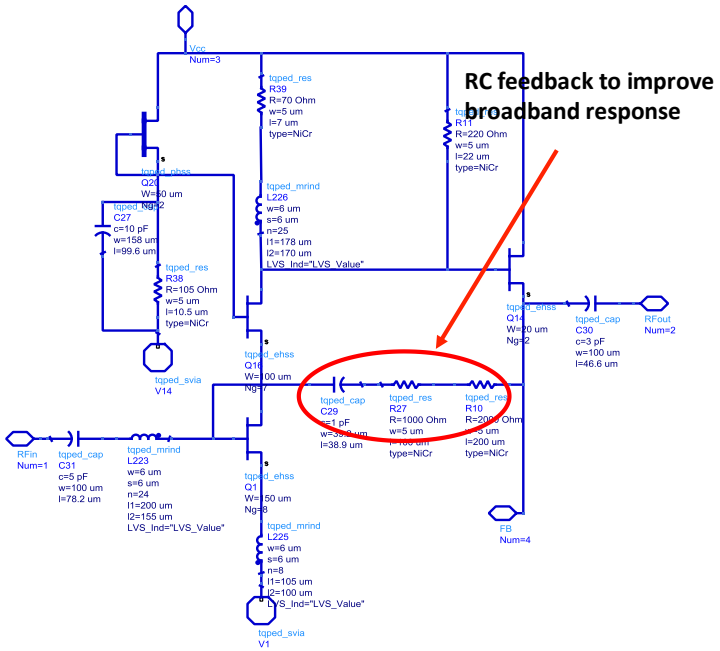



Figure 3-15. Wideband LNA Design

The entire system was designed using the Triquint TQPED GaAs process which is a 150 mm, 0.5 um pHEMT process with both depletion and enhancement mode devices. It offers three metal interconnecting layers with precision NiCr resistors and high value MIM capacitors. The individual blocks including phase shifters and amplifiers were initially designed using ideal components. Once the specifications were met, the ideal components were replaced with actual components from the design kit. This required further optimization of the design to account for device parasitics. Once the design components were re-tuned to meet the design specs, the next step was to generate the layout of the complete system. Floor planning of the entire layout is necessary to have a compromise between unnecessary coupling of the individual components and chip size. Once the layout was complete, the next step was to run electromagnetic simulation of the physical layout. ADS Momentum was used for this purpose. Additional re-tuning of the design was necessary at this point to account for coupling and the effect of interconnecting transmission lines. System level simulation of the 4 bit phase shifter is shown in Figure 3-13 to Figure 3-15 for all 16 states. Figure 3-16 shows the simulated RMS gain and phase shift error. Figure 3-17 shows the layout of the complete system with a chip size of 6800 µm x 4900 µm .

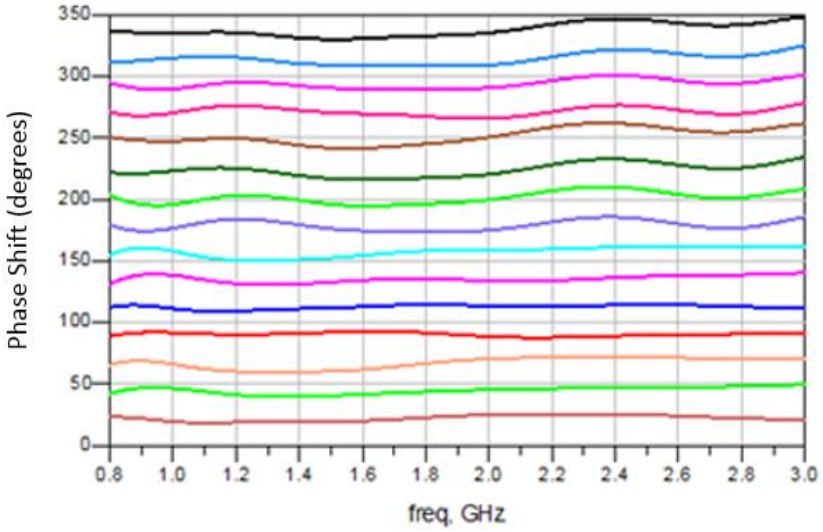



Figure 3-16. System level simulation of phase shift (degrees)

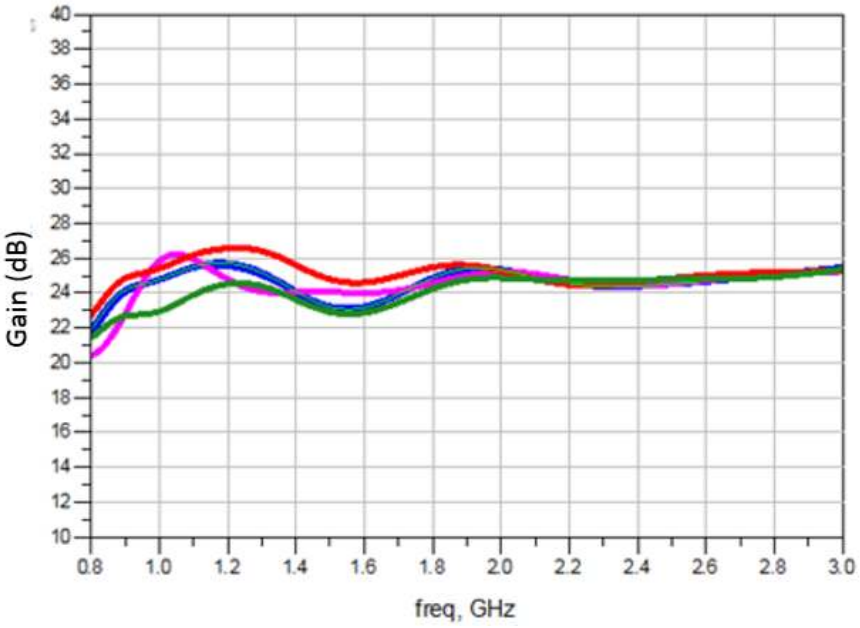



Figure 3-17. System level gain (dB)

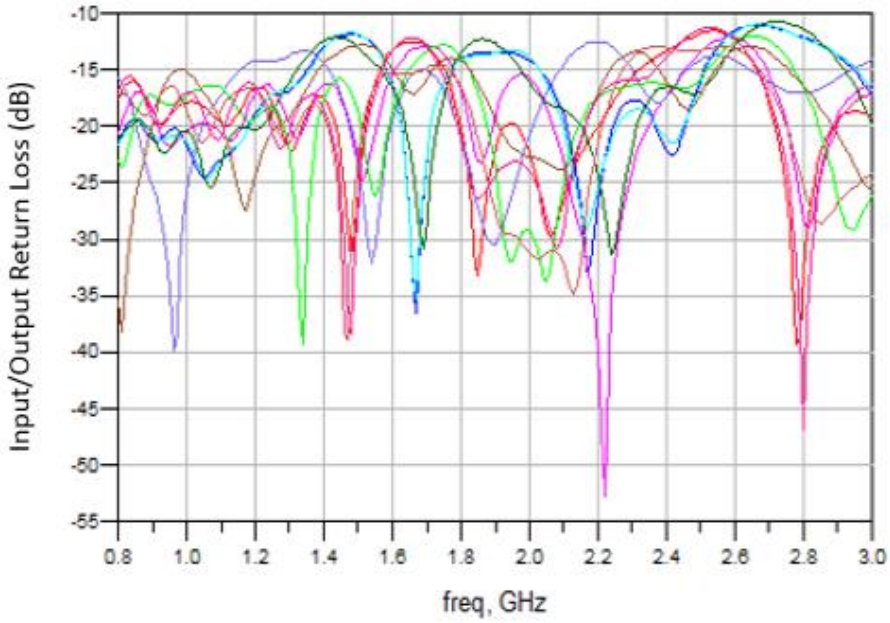



Figure 3-18. Simulation results of input/output return loss

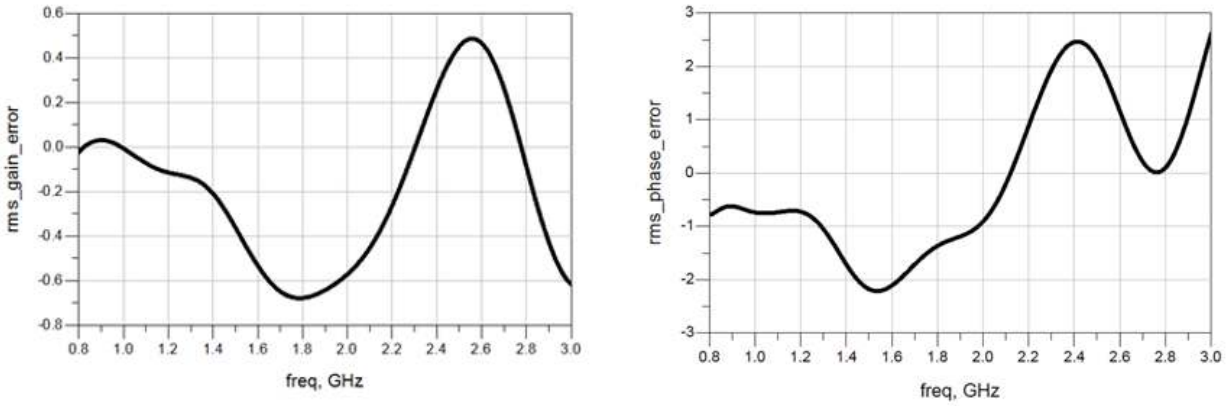



Figure 3-19. RMS gain and RMS phase error

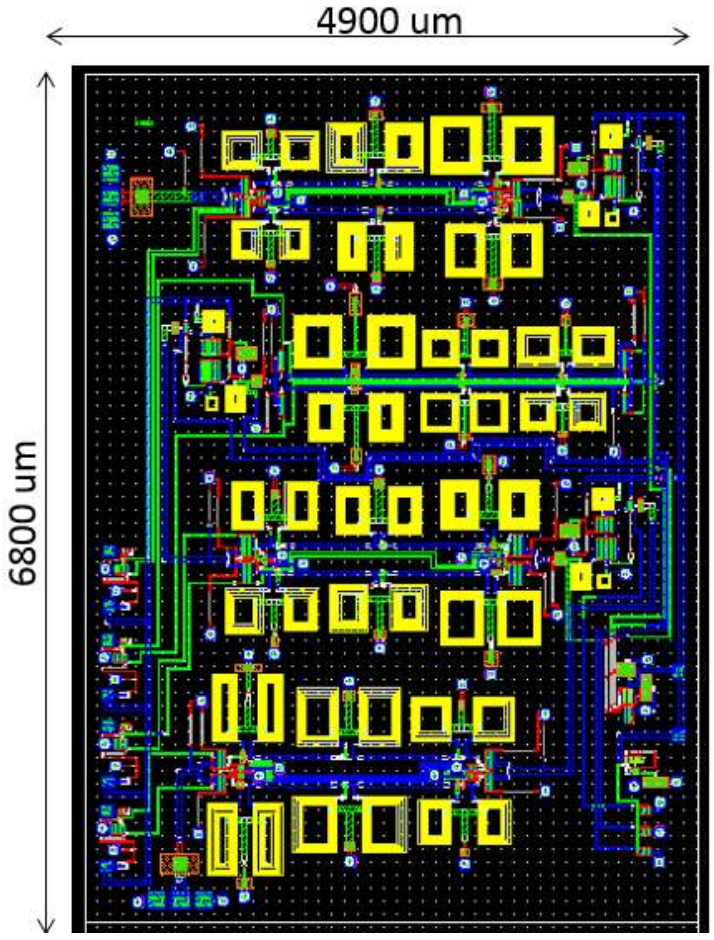



Figure 3-20. Complete chip layout

### 3.4 Fabrication and Measurement

Figure 3-18 (a) shows the fabricated chip and Figure 3-18 (b) shows the test board with the mounted chip. The 3 transmission lines on the right side of the board were used to perform TRL calibration. The test board is a 0.79 mm thick FR4 board. All traces on the test board were fabricated using 1 oz. copper with Electroless Nickel Electroless Palladium Immersion Gold (ENEPIG) surface finish to allow for the addition of wire bonds. The RF input and output pads of the chip are wedge wire bonded to the test board with two parallel 18 µm diameter gold wires to minimize the parasitic series inductance associated with the wire bonds.

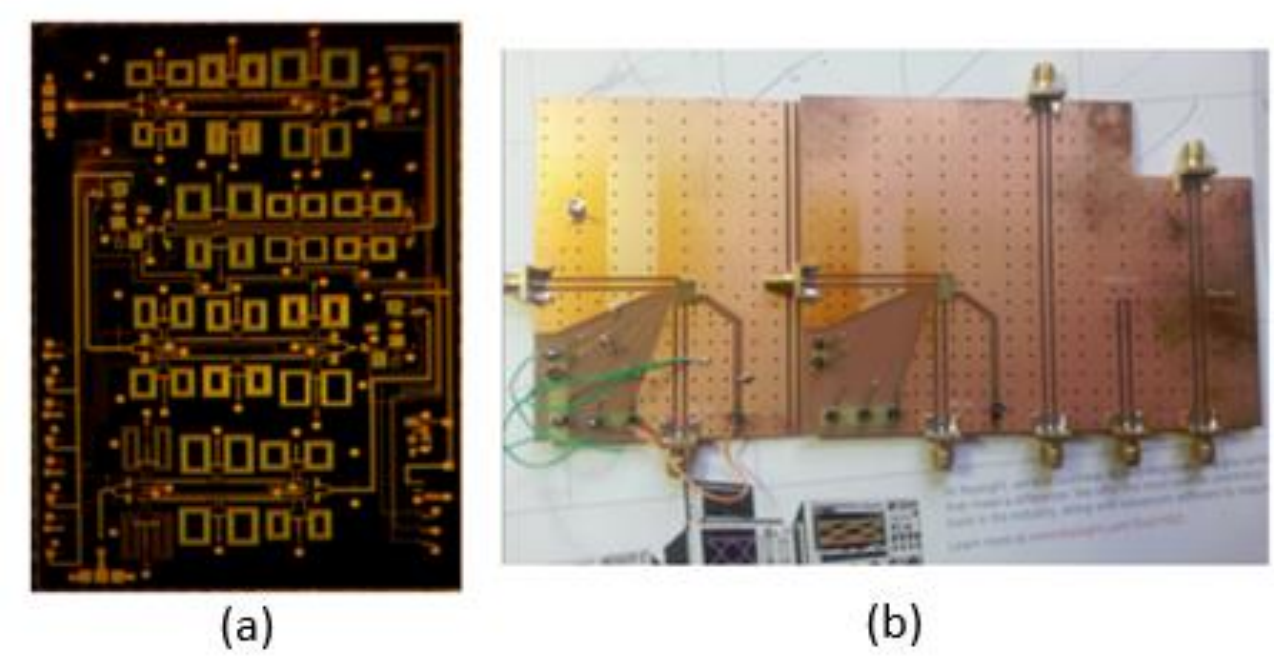



Figure 3-21. Fabricated chip and test board

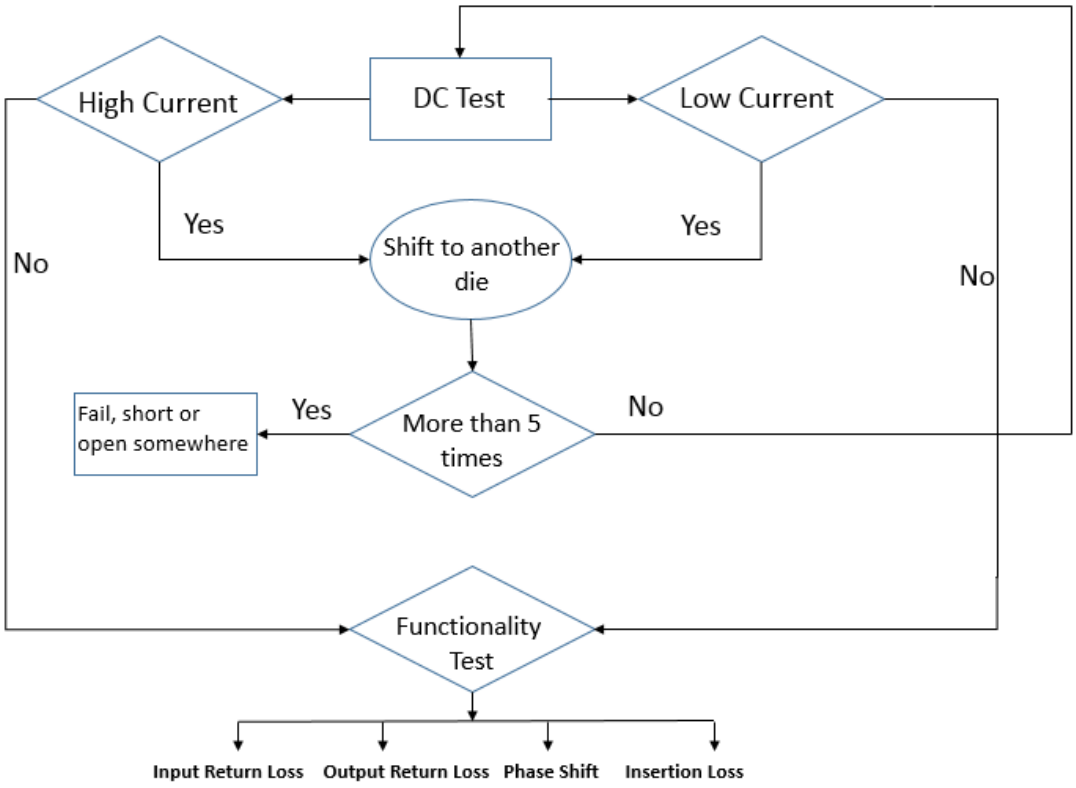
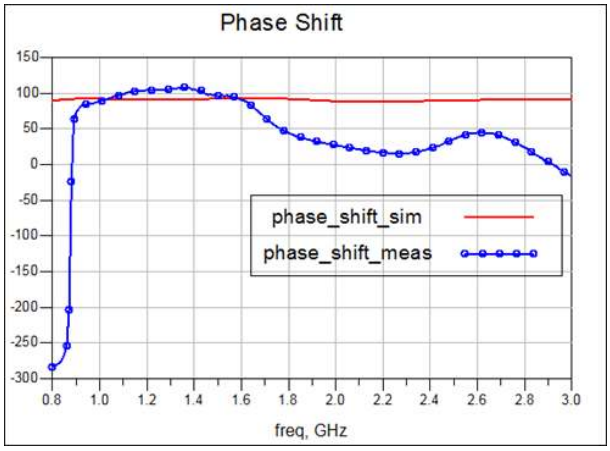



Figure 3-22. Flowchart for initial testing

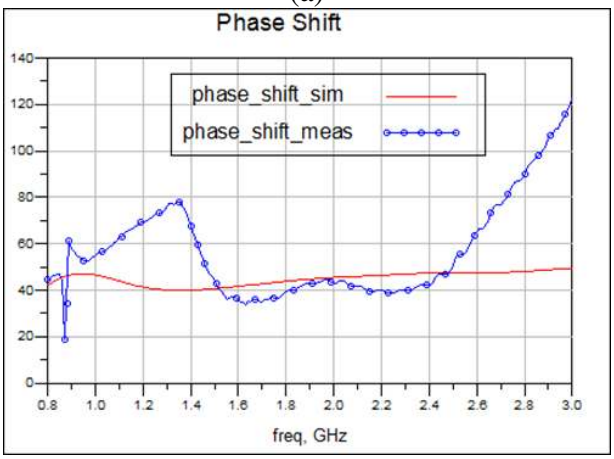
The flowchart shown in Figure 3-19 was used to carry out the measurements on the test board with each step explained below with corresponding results.

For DC Test, the design assed with logic control drawing 10 mA in the high state (5 V) and 0 mA in the low state (0 V). These are used to control the switches in the phase shifters to go from reference state to desired phase shifting state. Being a four bit phase shifter, there were four control pins. Amplifiers also passed DC test, drawing 36 mA from 5 V supply.

For the Functionality Test: The chip failed the functionality test giving acceptable results for input/output return loss but not for insertion loss and phase shift. Measured vs. simulated results did not match up. Measured vs. simulated plots shown below in figure 3-20.




(a)




(b)


(c)

Figure 3-23. Simulated vs. measured phase shift (a) 90° (b) 45° (c) 22.5° and (d) 180°


(d)

Figure 3-23. (Continued)

The root cause of functionality test failure is strongly suspected to be caused by spiral mutual inductance and coupling effects from the close proximity of the 60 inductors. The EM model inaccuracies and high coupling between the inductances which are very close to each other due to compact layout caused the difference between post layout simulation and measurement results.

A case study of this is provided below:

EM simulation done separately for each segment to simplify post EM optimization and tuning as well as simulation time. As a result, effects of mutual coupling from one segment to another was not accounted for. Maximum allowed chip size was utilized so no other option to further separate sections was possible.

The results of the experiment to find the root cause for a discrepancy between simulated and measured results is shown in Figure 3-25. The red trace is simulation of the schematic model of the inductor while the black trace is the momentum simulation result of a single

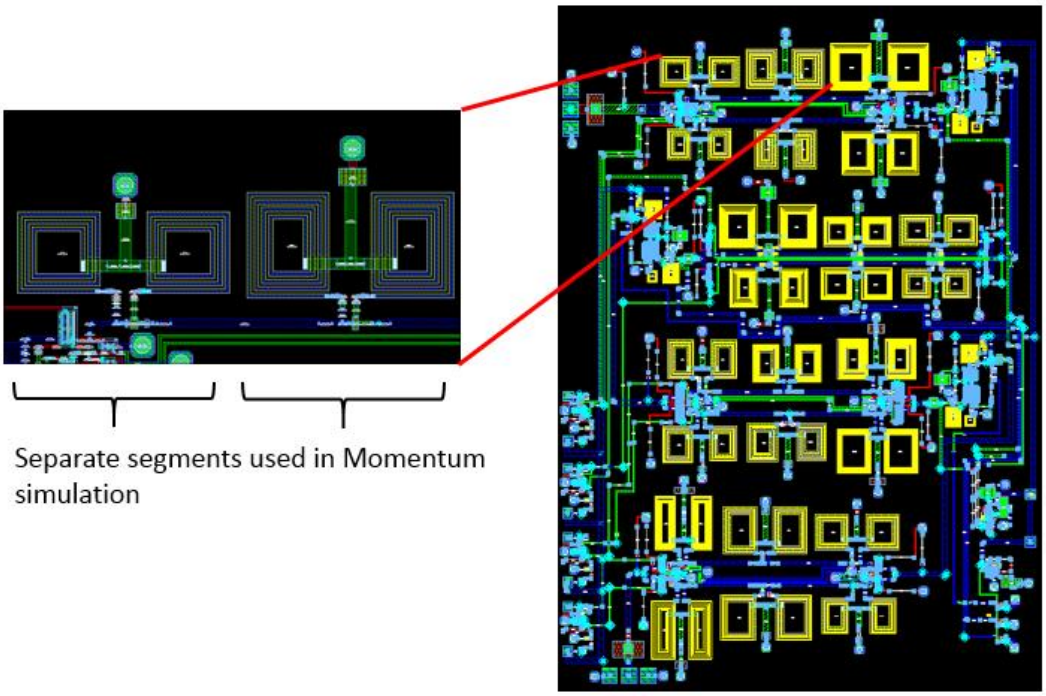



Figure 3-24. Segment of layout used for case study on mutual inductance

segment consisting of two inductors. This segment is similar to that used in optimization of the design with the entire phase shifter broken up in similar segments. The blue trace shows similar simulation of this segment but with another inductor in close proximity similar to what is actually encountered in the layout. It is clearly observed that the mutual coupling between the additional inductor and the segment does affect the net inductance. This occurs throughout the chip and is the reason for discrepancy between measured and simulated results. Adequate performance would require that these inductors be spaced further apart and therefore consuming much more die area.

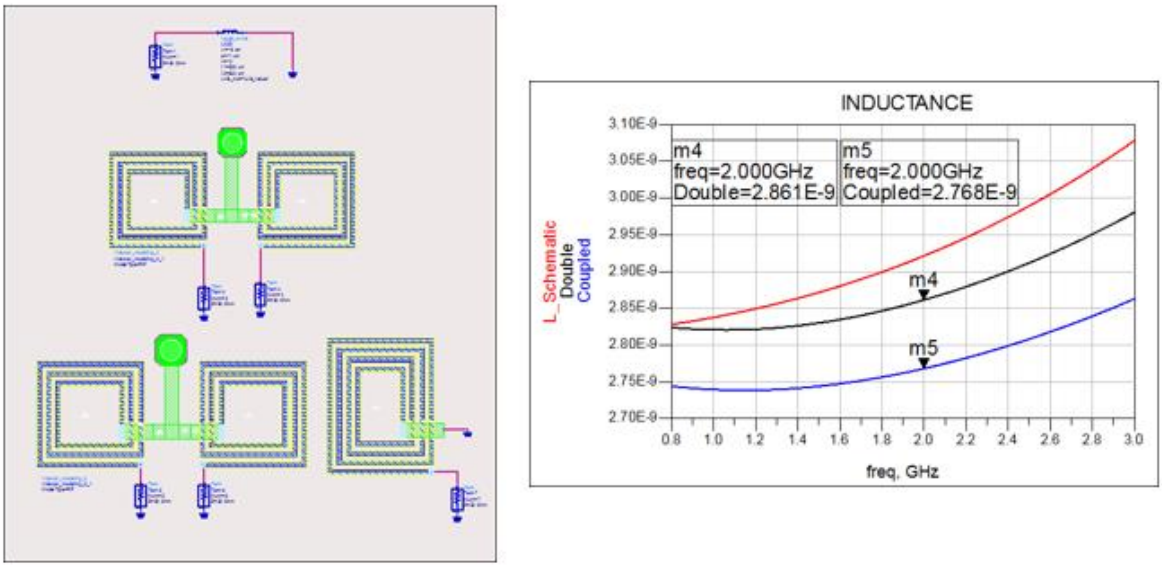



Figure 3-25. Inductor mutual inductance

### 3.5 Summary

This chapter presented the theory as well as the practical technique for the design of passive all-pass phase shifters and detailed the design of a broadband phase shifter. It first described the design techniques and equations used to design passive all-pass filters which form the core of the phase shifter. The two most common types of all-pass filters were presented with a brief description of their frequency response. Next, a broadband 4-bit phase shifter was designed for S- and L- band frequencies. To achieve a design that is operational from 0.8 GHz to 3 GHz, 3 sections of all-pass networks were necessary for each bit. The design was implemented using the Triquint TQPED GaAs pHEMT process. To compensate for loss, an LNA was also designed and implemented in the signal chain. Measured and simulation results did not match up and additional analysis of the design discover the root cause of the discrepancy was due to inductive coupling which was not accounted for in the momentum simulations. The only solution to solving this issue using the current design approach is to space out the layout to allow more separation between the inductors. This was not an option for this research as the initial design was already using the

maximum allowed chip size as determined by the foundry. To address the challenging needs of small size, wide bandwidth and low frequency applicability, the second design detailed in the next chapter proposes a novel phase shifter implementation that utilizes tunable active differential inductors within all-pass networks.

### 3.6 References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## Chapter 4:

## Active Inductor Design

### 4.1 Gyrator Based Active Inductor

Gyrator-C networks can be used to synthesize floating active inductors. A gyrator consists of two back-to-back connected transistors which function as an active inductor when one port is connected to a capacitor as shown in figure 4-1. [4.1]

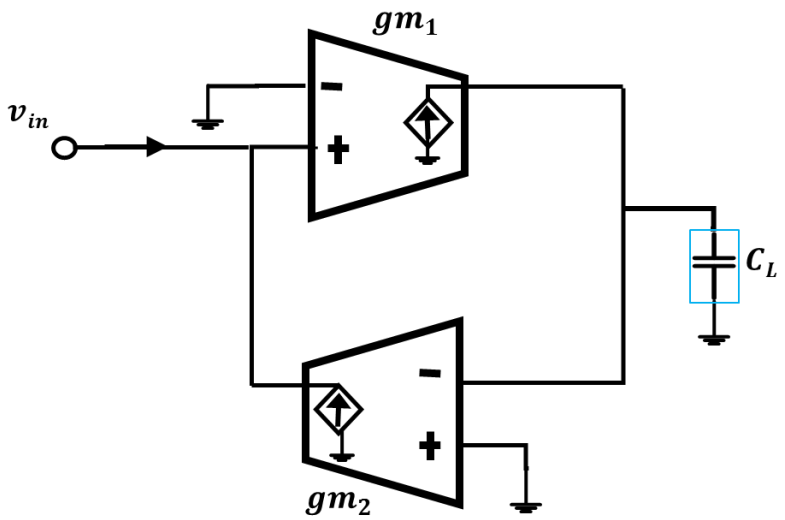


Figure 4-1. Lossless single-ended gyrator-c active inductor.

$$L = \frac{C_L}{gm_1 gm_2} \tag{4.1}$$

The inductance generated by this topology can be calculated using (4.1) which shows that the inductance is proportional to the value of the load capacitance and inversely proportional to the transconductance ($\boldsymbol{gm}$)of the transistors used.

The finite input impedance of the transconductors used in the active inductor makes the network quite lossy and limits the frequency range over which it behaves like an inductor. Figure 4-2 shows a lossy floating gyrator-c active inductor and its equivalent circuit. $\boldsymbol{G_{03}}$ and $\boldsymbol{G_{04}}$ are the total output conductance of the transconductors, $\boldsymbol{R_P}$ represents the parasitic parallel resistance, $\boldsymbol{C_p}$ the parallel capacitance and $\boldsymbol{R_S}$ the series resistance. $\boldsymbol{C_1}$ and $\boldsymbol{C_2}$ represent total parasitic capacitances at each corresponding node.

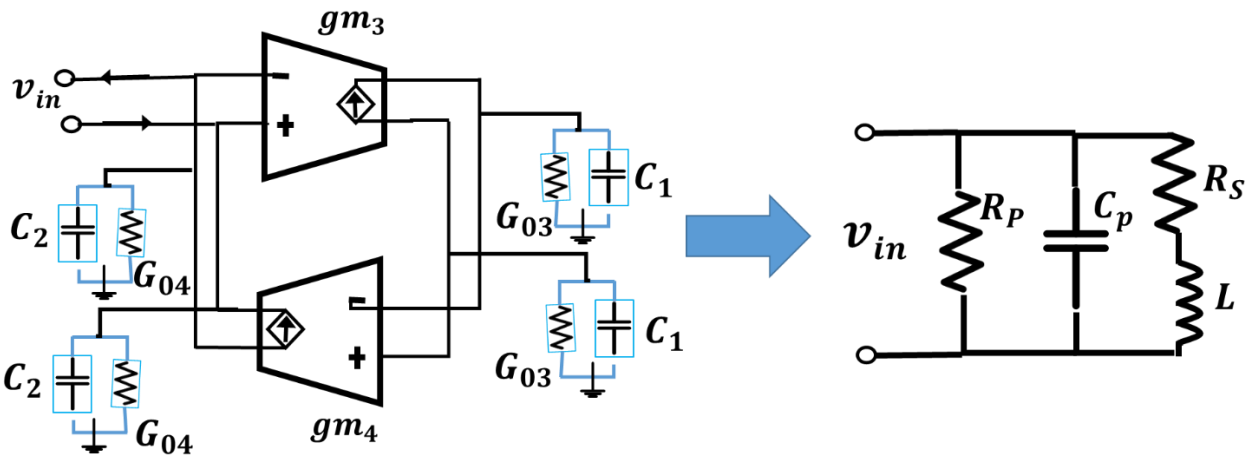


Figure 4-2. Lossy floating gyrator-c active inductor and equivalent RLC circuit

The parameters for this lossy active inductor as represented by the equivalent RLC network are given by [4.1]

$$Rp = \frac{2}{G_{04}}$$

$$Cp = \frac{C_1 + C_2}{2}$$

$$Rs = \frac{G_{03} + G_{04}}{gm_3 gm_4}$$

$$L = \frac{\frac{C_1+C_2}{2}}{gm_3 gm_4} \tag{4.2}$$

## 4.2 Frequency Response of Active Inductors

The inductive characteristics exhibited by a lossy gyrator-c active inductor are frequency limited and dictated by the parasitic resistance of the network. For the equivalent RLC network shown in figure 4-2, the input impedance is given by [4.1]

$$Z = \left(\frac{Rs}{CpL}\right)\frac{s\frac{L}{Rs}+1}{s^2+s\left(\frac{1}{RpCp}+\frac{Rs}{L}\right)+\frac{Rp+Rs}{RpCpL}} \tag{4.3}$$

The pole and zero resonant frequency of the impedance occurs at

$$\omega p = \sqrt{\frac{Rp+Rs}{RpCpL}} \quad for\ Rp \gg Rs, \quad \omega p = \sqrt{\frac{1}{CpL}} \quad = \quad \omega_o$$

$$\omega z = \frac{Rs}{L} \tag{4.4}$$

Equation (4.4) shows the dependence of the frequency response on the parasitic impedance of the system where the lower bound of the frequency range is dictated by $\omega z$ and the upper bound by $\omega p$. As shown in the bode plot in figure 4-3, $\omega z$ should be minimized and $\omega p$ should be maximized. Based on equation (4.4), $\omega z$ can be minimized by decreasing $Rs$ as given in equation (4.2). This can be done by proper sizing of transistors to control output conductance $G_{03}$ and $G_{04}$ in figure 4.2 or by using cascode transistors. Additional operational frequency range can also be obtained by using a feedback resistor [4.2]. Here, the author used a feedback resistor to introduce as additional zero to cancel the dominant pole and allowed for the use of fairly large values of integrating capacitors ($Cp$ in equation 4.4) without limiting the maximum range of frequency where the system behaves like an inductor.

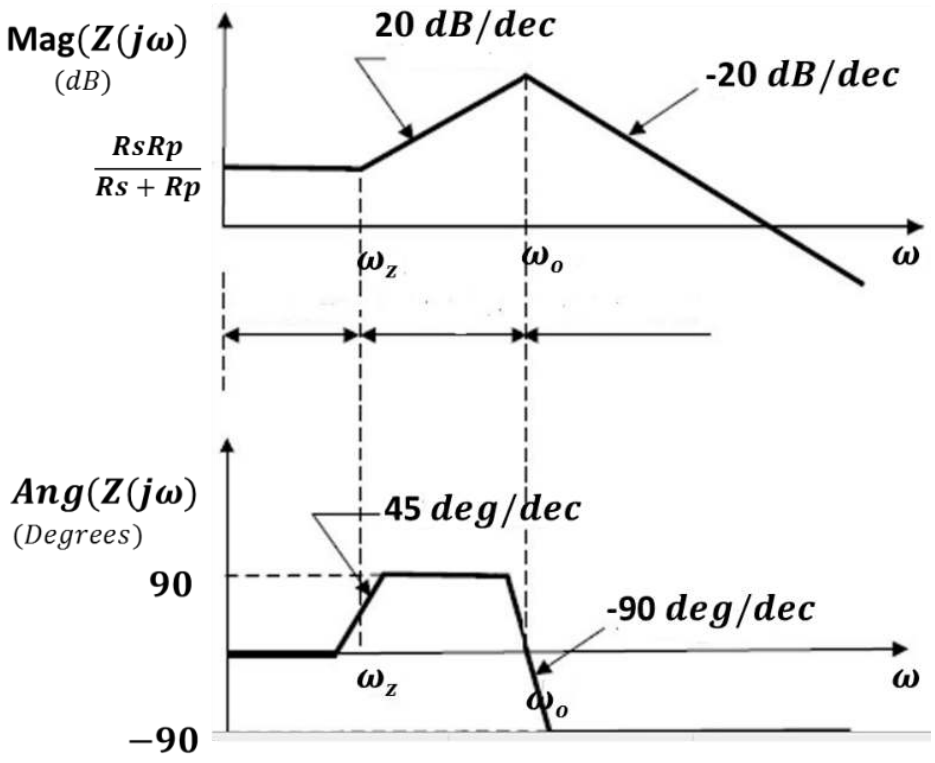


Figure 4-3. Bode plot of lossy gyrator-c active inductor

When $Rs >> Rp$ , the quality factor of the lossy gyrator-c active inductor is highly dependent on the series parasitic resistance as can be described in equation (4.5).

$$Q = \frac{\omega L}{Rs} \tag{4.5}$$

For applications, such as in oscillators where high quality factor is necessary, decreasing the value of $Rs$ to increase Q can be achieved by reducing the output conductance $G_{03}$ of the transistors according to equation (4.2). This can be done by using cascode transconductors but will have a negative effect on devices dynamic range. Proper sizing of transistor width has a direct effect on the device gm and increasing this value also decreases $Rs$ but this also influences the value of inductance $L$. The $Q$ of the active inductor can be further increased by introducing a shunt negative resistor to the input of the gyrator-c network to cancel out the parasitic resistance seen in its RF

equivalent circuit shown in Figure 4-2. This can be seen from the circuit model in Fig. 4-4 that revises the RF equivalent circuit of the gyrator-c network by replacing the series $Rs - L$ branch with parallel $\hat{R}p$ and $\hat{L}$ branches. To implement the negative $R$ that will be used to cancel $\hat{R}p$, two cross coupled equally sized transistors can be employed as shown in Fig. 4-5 [4.3]. The negative resistance and total resistance of this network is given by

$$-R = -\left(\frac{1}{gm_5} + \frac{1}{gm_6}\right)$$

$$R_{total} = \hat{R}p \| -R \tag{4.6}$$

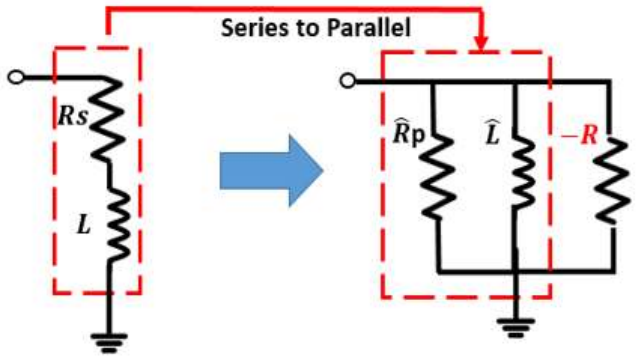


Figure 4-4. RL parallel to RL series branch transformation

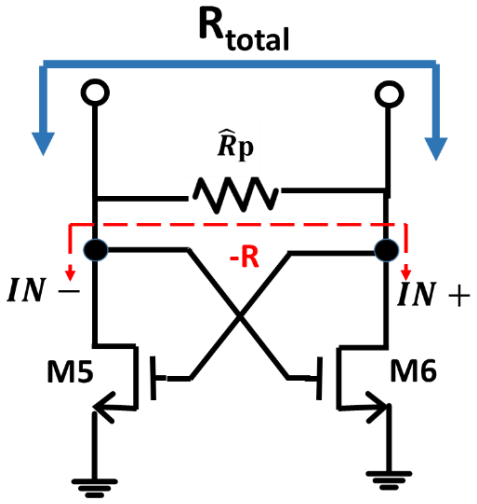


Figure 4-5. Negative resistance cross-coupled transistors

### 4.3 Differential Active Inductors

A compact source-degenerated differential active inductor (DAI) has been proposed in [4.4] that utilizes two mosfets as the gyrators in the differential gyrator-c active inductor topology as shown in figure 4-6.

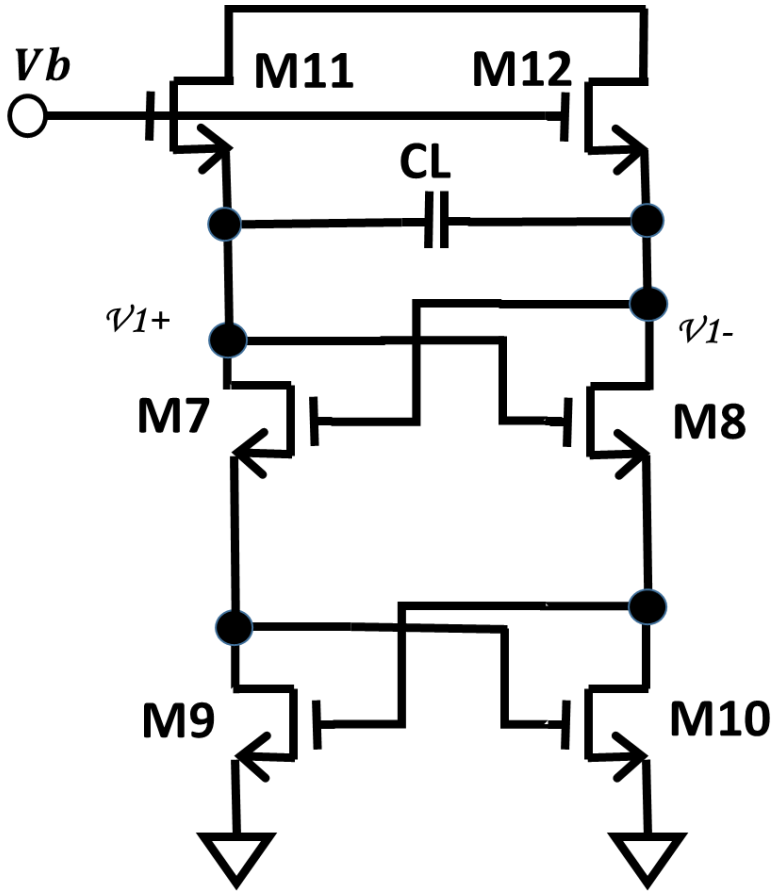


Figure 4-6. DAI based on cross-coupled transistors

The design comprises of two cross coupled transistors (M7 and M8) acting as the back to back transconductance amplifiers. Transistors M9 and M10 form the negative resistance circuit necessary to improve the quality factor. Inductance tunability is achieved by varying the *gm* values of the cross-coupled transistor pair M7 and M8 as described in equation (4.1) where CL is the load capacitance including all parasitic capacitance. Inductance tuning is done by varying the current

through these transistors by adjusting the tuning voltage *Vb* on transistors M11 and M12. The schematic in Figure 4-7 is a modified version of this design that uses feedback resistors to improve on the performance of the active inductor. Feedback resistors $R_f$ increases the frequency range of the inductor but also serves to lower the parasitic series resistance and increase the inductance as described in [4.3]. With the addition of the feedback resistors, the active inductor parameters become

$$L = \frac{CL}{\alpha(gm_{13}gm_{14})}$$

$$Rs = \frac{\frac{1}{R_T}\omega p^2 Cgs_{13,14} CL R_f}{g_{m13}g_{m14}}$$

$$R_T = R_f \| R_d \| ro_{15,16} \| ro_{13,14} \tag{4.7}$$

where $\alpha$ represents the voltage attenuation factor (between 0 and 1) introduced by the feedback resistors, $\omega p$ is the frequency in (4.4), $ro_{13,14}$ is the output resistance of transistors M13 and M14, $ro_{15,16}$ is the net negative resistance of M15 and M16 and $CL$ is the load capacitance. $Cgs_{13,14}$ is the sum of the gate to source capacitances of M13 and M14. In the case, where $Rs$ becomes negligible because of the negative resistance network, the quality factor of the active inductor is determined by the parallel resistance $Rp$ in figure 4.2 and equation (4.5) becomes

$$Q \approx \frac{Rp}{\omega L} \tag{4.8}$$

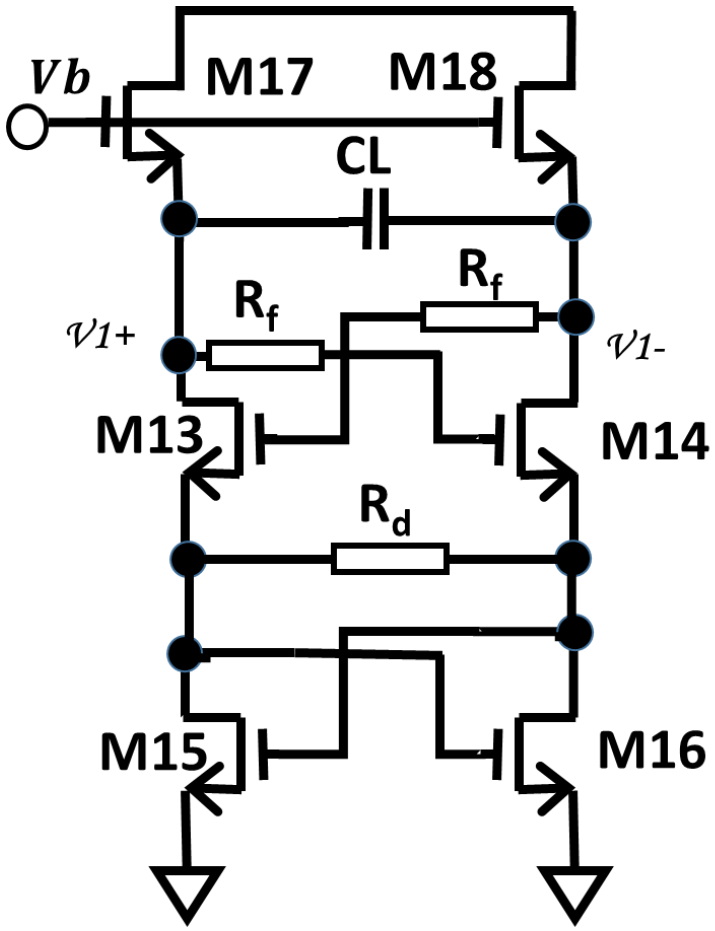


Figure 4-7. DAI based on cross-coupled transistors with feedback

Thus, the feedback resistors decrease the quality factor by increasing L. Linearity improvement is also achieved using feedback resistors in the topology described in [4.3] by decreasing the internal loop gain given in equation (4.9). This loop gain arises from an increase in $V_{GS}$ of transistors M13 and M14. For large voltage swings at the input, these transistors will go into compression and exhibit nonlinear behavior. Here, $\alpha$ represents the voltage attenuation introduced by the feedback resistors and $\omega_o$ is the resonant frequency.

$$A_L(\omega_o, \alpha) = \frac{\alpha(g_{m13}+g_{DS13})}{CL\omega_o} \tag{4.9}$$

Active inductors implemented using the gyrator-c topology are negative feedback systems and thus, stability should also be considered. Classifying the gyrator-c active inductor shown in figure 4-2 as a second order system, the damping factor is given by (4.10) [4.1].

$$\xi = \frac{1}{2\sqrt{g_{m3}\, g_{m4}}}\left(\sqrt{\frac{C_2}{C_1}} + \sqrt{\frac{C_1}{C_2}}\right) \tag{4.10}$$

Increasing $g_{m3}$ or $g_{m4}$ will lead to a decrease in the damping factor resulting in a decrease in stability. Resistor $R_d$ in figure 4-7 thus becomes mandatory for unconditional stability ensuring that the resistance of the system does not go negative.

**4.4 Circuit Implementation**

For this application, a DAI like that shown in figure 4-7 was designed as part of the active all-pass phase shifter with a tuning range from 1.6 nH to 4.3 nH at 1.5 GHz and 0.9 nH to 2.2 nH at 3 GHz. These values were obtained from values for the design of passive all-pass filters [4.5]. The proposed DAI was fabricated in a 0.5 µm GaAs pHEMT process with both enhancement and depletion mode transistors. Equations (4.2) – (4.10) were used as a guide in the proper sizing of the transistors. M13 and M14 are the most critical transistors as these form the gyrators used in implementing the active inductor. From (4.2) value of inductance in inversely related to $g_{m13}$ and $g_{m14}$ which are the transconductance of M13 and M14. Given that $g_m = \sqrt{2K\frac{W_{13,14}}{L_{13,14}}I}$ then proper sizing of these transistors is critical to set the starting value of $g_m$ and inductance to be able to achieve the desired tuning range and frequency response. When the size of M13 and M14 increase, $g_{m13}$ and $g_{m14}$ as well as parasitic capacitance $Cgs$ will increase and have a direct impact on decreasing $L$. $Rs$ will decrease which in turn will also decrease the frequency of $\omega z$ thus increasing the operational frequency range. This increase in $g_m$ will be much larger than that of $Cgs$. Decreasing the value of $L$ on the other hand will increase $Q$ as well as the self-resonant

frequency $\omega_o$. Optimization of the transistor size for M13 and M14 must be done in order to get the inductance values and frequency range mentioned previously. The feedback resistors $R_f$ add another degree of freedom as this also has a direct impact on the frequency range and inductance values [4.2]. Transistors M15 and M16 form the negative resistance network and this has a minimal impact on the inductance value and frequency range and is used to increase the $Q$ of the network. It is important to note that this circuit can be made tunable to be able to modify the $Q$ value. That was not an option implemented in this design but can be done in other versions. Transistors M17 and M18 serve as current mirrors to vary the $g_m$ of M13 and M14 to tune the inductance.

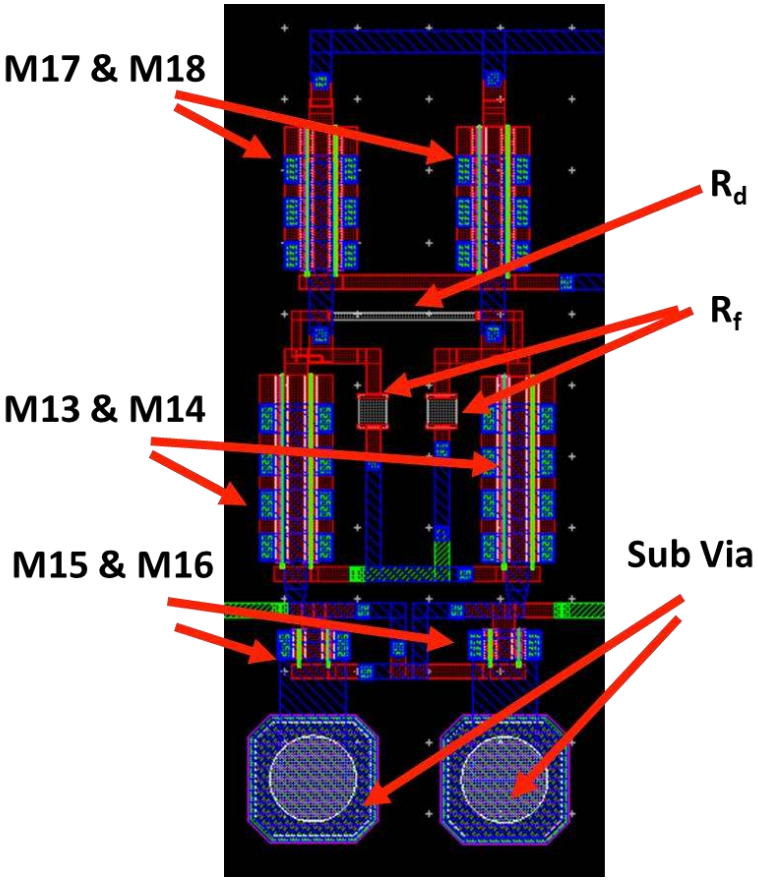


Figure 4-8. Layout of active inductor

### 4.5 Post-Layout Simulation Results

Extensive EM simulations were done using ADS Momentum as part of the post-layout simulation of the DAI to account for all parasitic effects. Optimization of the transistor size as mentioned previously resulted in achievement of the desired tuning range of inductance over a frequency range from 1.5 GHz to 3 GHz as shown in figure 4-9. Given that the network functions as a feedback system, requirements for unconditional stability become important. Implementation of series resistor Rd was included for this purpose. Figure 4-10 shows both stability factor as well as stability measure of the DAI for tuning voltage from 3.1 V to 3.5 V. Unconditional stability was achieved since stability factor > 1 and stability measure > 0.

The quality factor of the inductor for the range of tuning voltages is shown in figure 4-11. As mentioned in the previous section, quality factor trades with linearity and this tradeoff becomes obvious by observing the simulation results of figure 4-12. Quality factor ranges from about 14.8 to about 17.5 but IIP3 has values as high as 8.4 dBm.

The simulation results demonstrate that the proposed design technique is an excellent approach for the design of the DAI to properly function as part of the phase shifter network.

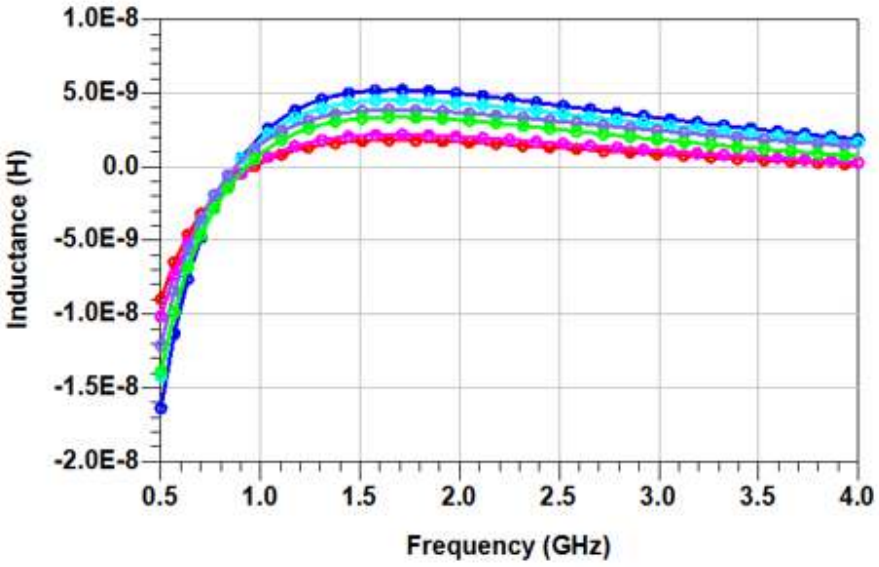


Figure 4-9. DAI inductance tuning range

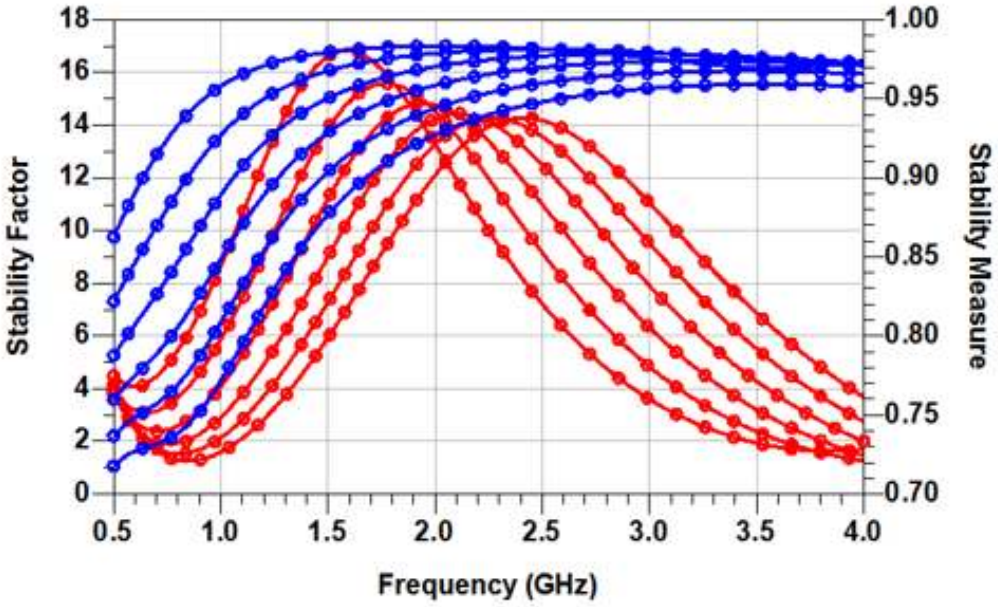


Figure 4-10. DAI stability simulation results

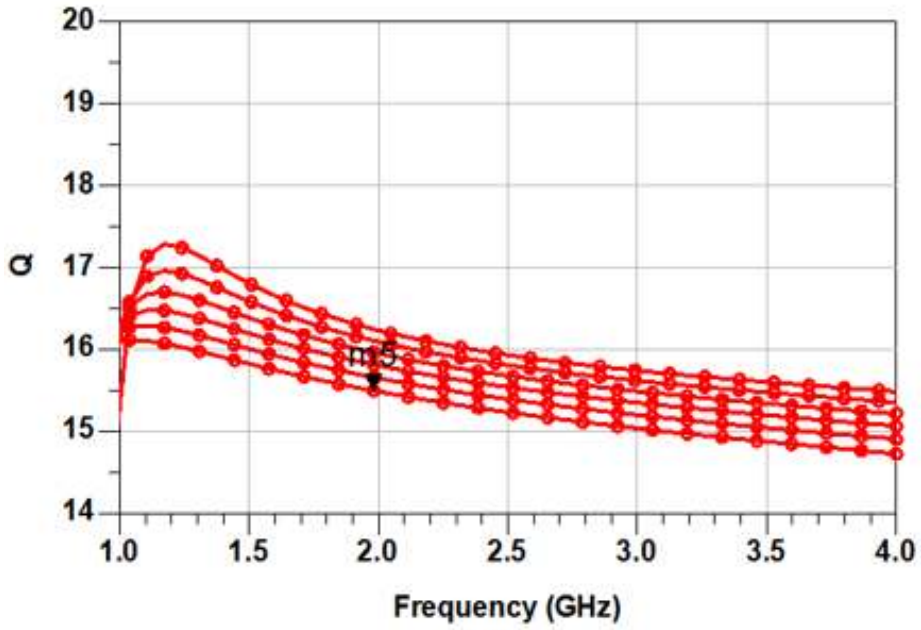


Figure 4-11. DAI quality factor for inductance tuning range

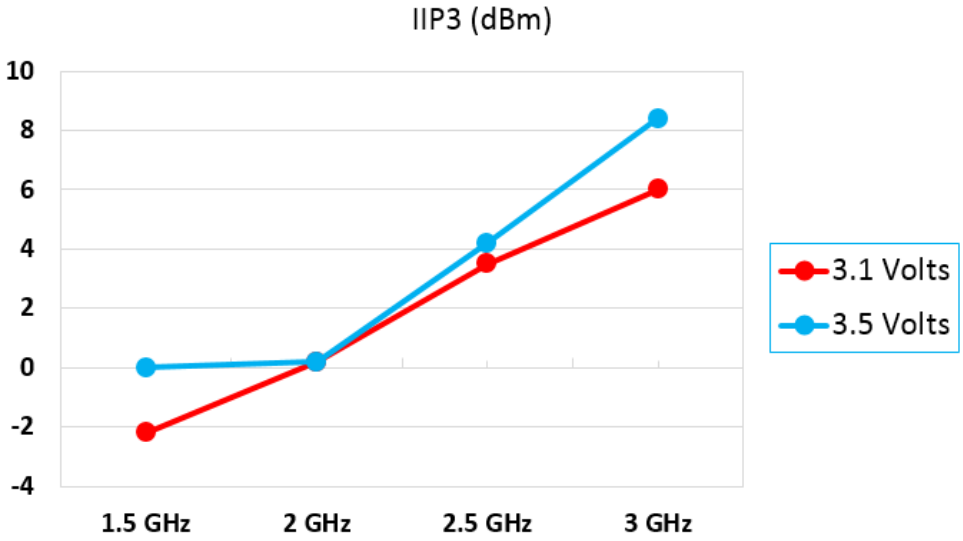


Figure 4-12. Input third order intercept point

## 4.6 Summary

This chapter presents a technical discussion on the design of single-ended as well as differential or floating active inductors using the gyrator as the core building block. An analysis of the frequency response was done to investigate the limitations of the active inductor in an effort to

improve the design for the given application. The quality factor of the active inductor was also investigated which called for the addition of a negative resistance network to compensate for series parasitic resistance. Finally, a differential active inductor was designed using the Triquint TQPED GaAs process. EM extracted simulation results demonstrate that the proposed design is an excellent approach for the design of the differential active inductor (DAI) forming the core of the phase shifter network.

**4.7 References**

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[4.2] R. Akbari-Dilmaghani, A. Payne, and C. Toumazou, "A High Q RF CMOS Differential Active Inductor," IEEE Pm. ISCAS, vol. 3. pp. 157- 160, 1998.

[4.3] F. Belmas, F. Hameau, and J-M. Fournier , "A New Method for Performance Control of a Differential Active Inductor for Low Power 2.4 GHz applications," IEEE International Conference on IC Design and Technology, June 2-4 2010.

[4.4] Chun-Lee Ler; bin A'ain, A.K.; Kordesch, A.V. "Compact, High-Q, and Low-Current Dissipation CMOS Differential Active Inductor" Microwave and Wireless Components Lett. , Oct. 2008

[4.5] X. Tang and K. Mouthaan, "Design of large bandwidth phase shifters using common mode all-pass networks," IEEE Microw. Wireless Components. Lett., vol. 22, no. 2, pp. 55–57, Feb. 2012.

# Chapter 5:

# Modified All-Pass Phase Shifter

## 5.1 System Level Design

The functional block diagram of the phase shifter is shown in Figure 5-1. The first stage is composed of an active balanced-to-unbalanced (balun) circuit followed by a single pole double throw (SPDT) switch. The balun is designed to provide a wideband 50 Ω impedance match at the RF input and reduce the insertion loss of the phase shifter by providing gain. The balun functions as a switched 180° phase shifter bit to complement the phase shift that is attained in the second stage. Therefore, accuracy in both phase and amplitude performance of the balun is crucial as it directly contributes to the overall performance of the phase shifter.

The second stage of the phase shifter is an all-pass network implemented using active inductors. All-pass networks are attractive for large phase shift bandwidths. It is typical to use them in digital implementations by including two switchable all-pass network blocks to form a phase shift bit [5.1] (e.g. a 22.5° bit). The complete phase shifter generally includes 4 to 6 such bits. However, implementation of this type of phase shifter causes the circuit area to be dominated by passive inductors, not only by the physical size of each inductor, but also the spacing needed between them to reduce mutual coupling to an acceptable level. Therefore, the all-pass network utilized in this work is based on an active tunable inductor that is compact and eliminates the need for several all-pass network blocks. The shunt inductor all-pass configuration (see Figure 5-1) requires identical inductance values for its inductors and is therefore chosen over the shunt capacitor design. As detailed in Chapter 4, the selected active inductor based all-pass network implementation provides

continuous adjustment of the phase shift within 0°-180° from 1.5 GHz to 3 GHz through a control voltage.

The third and final component of the functional block diagram comprises a two stage VGA that also acts as an output buffer. The first stage of the VGA is a common gate amplifier that provides a constant load impedance to the output of the active all-pass network. The second stage is another common gate amplifier with a variable bias resistor network in order to adjust the amplifier gain to balance the gain variations among the phase shift values. The output buffer at the end of the circuit is designed to provide a wideband 50 Ω match at the output. The following sections detail the design of each of the blocks within the proposed phase shifter with specific emphasis on the trade-offs between tunability, bandwidth and achievable phase shift associated with inclusion of active inductors within the all-pass network.

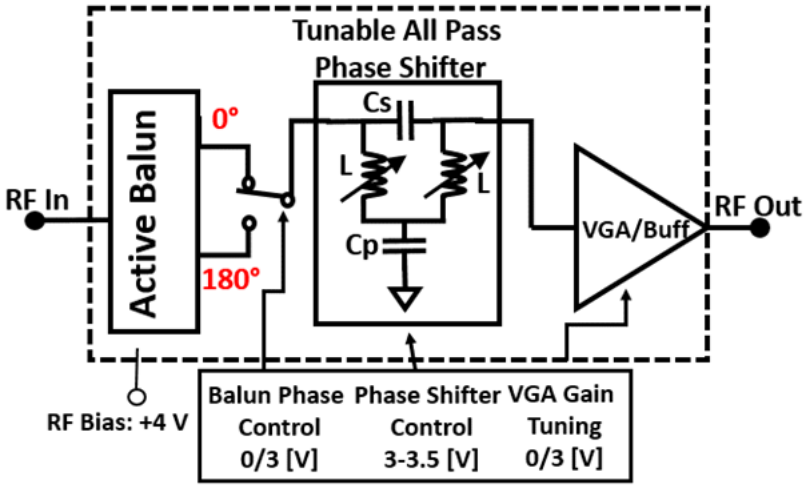



Figure 5-1. Functional block diagram.

### 5.2 Active Balun Based 180° Phase Shifter

The single-to-differential circuit topology shown in figure 5-2 has been extensively used to implement an active balun as documented in [5.2], [5.3] and [5.4]. These show reliable performance with moderate noise, good linearity, wideband input match and balanced outputs.

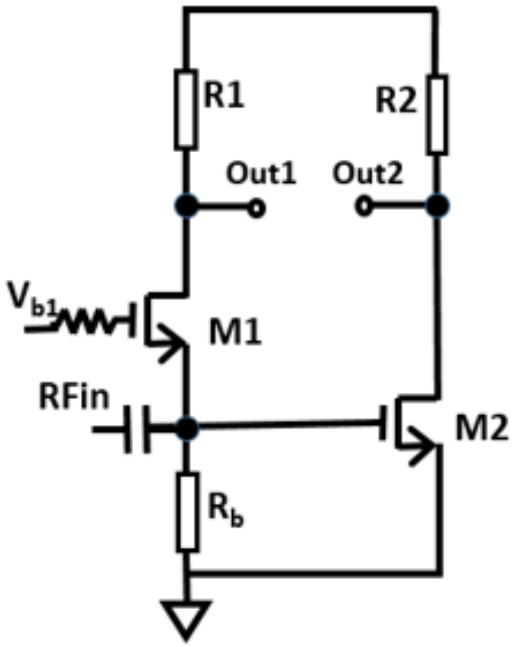



Figure 5-2. Common-gate common-source active balun

This topology functions by taking an input signal and splitting it into two separate signals that are ideally equal in magnitude but 180° apart. It combines a common gate (CG) amplifier M1 and a common source (CS) amplifier M2 to provide a wideband input impedance given as

$$Rin = \frac{1}{gm1} || \, R_b. \tag{5.1}$$

When Rb is large, the input impedance is dominated by the 1/gm1 parameter which means that Rb must be large to have minimal effect on input match as well as gain. The gain of the two branches then becomes

$$Av_{CG} = gm1xR1$$

$$Av_{CS} = -gm2xR2 \tag{5.2}$$

where gm1 represents the transconductance of the common gate transistor M1 and gm2 represents that of the common source transistor M2. Rb also serves to provide a bias voltage to M2. According to equation 12, for this topology to function as an active balun, the transconductance (gm) of each

stage in combination with corresponding load resistor must be equal. There are three different option to implement this which include equal gm values for M1 and M2 as well as equal value for load resistors, n times larger gm for CS stage with a load resistor n times smaller than that of CG stage and n times smaller gm for CS stage with a load resistor n times larger than that of CG stage.

For large values of Rb (400Ω - 700Ω) relative to a source resistance Rs (50 Ω) the input impedance of the CG stage is $Rin_{CG} = {}^{1}/_{gm1}$ with a corresponding gain $Av_{CG} = gm1xR1$. With matching conditions met at the input, the source impedance and input impedance of the CG stage are equal and the gain can be defined as

$$Av_{CG} = \frac{R1}{Rin_{CG}} \tag{5.3}$$

For the combined CG and CS branch to function as a balun, the phase difference should be 180° but the gain of each branch must be identical. This sets the condition for the CS branch to have a gain equivalent to (5.3) and given as

$$Av_{CS} = -Av_{CG} = \frac{-R1}{Rin_{CG}} = \frac{-R1}{Rs} \tag{5.4}$$

Figure 5-3 shows the active balun implemented in this design. The common gate stage (M1) provides a wideband input impedance match and $0^0$ phase shift while the common source stage (M2) provides the necessary $180^0$ phase shift. Only one output is used at a time depending on desired phase shift. To achieve this, addition of switches on the output branch of each path is used. This allows for the rerouting of the input signal providing the option of either $0^0$ or $180^0$ phase shift. Equalizing the gain of the two stages by tuning the load resistors completes the design. Both the CS and CG stages were cascoded for higher voltage gain and better isolation.

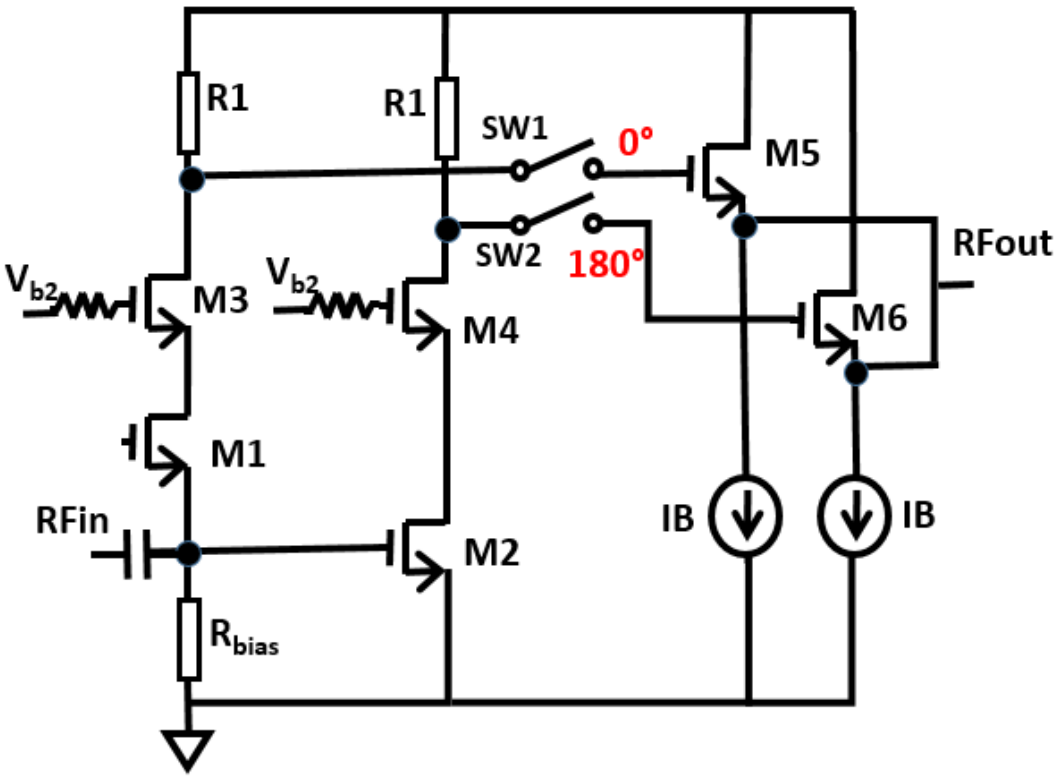



Figure 5-3. Active balun with switches

The switches were implemented using single enhancement mode transistors before the output buffers M5 and M6. The buffers were implemented to isolate the balun from the active all-pass phase shifter.

Simulation results of the active balun are shown in Figure 5-4 – Figure 5-6. Good input impedance match is achieved as can be seen in figure 5-4. Figure 5-5 shows the gain error between the two branches differ by a maximum of 0.5 dB and Figure 5-6 shows that the 180° phase difference requirement has been met.

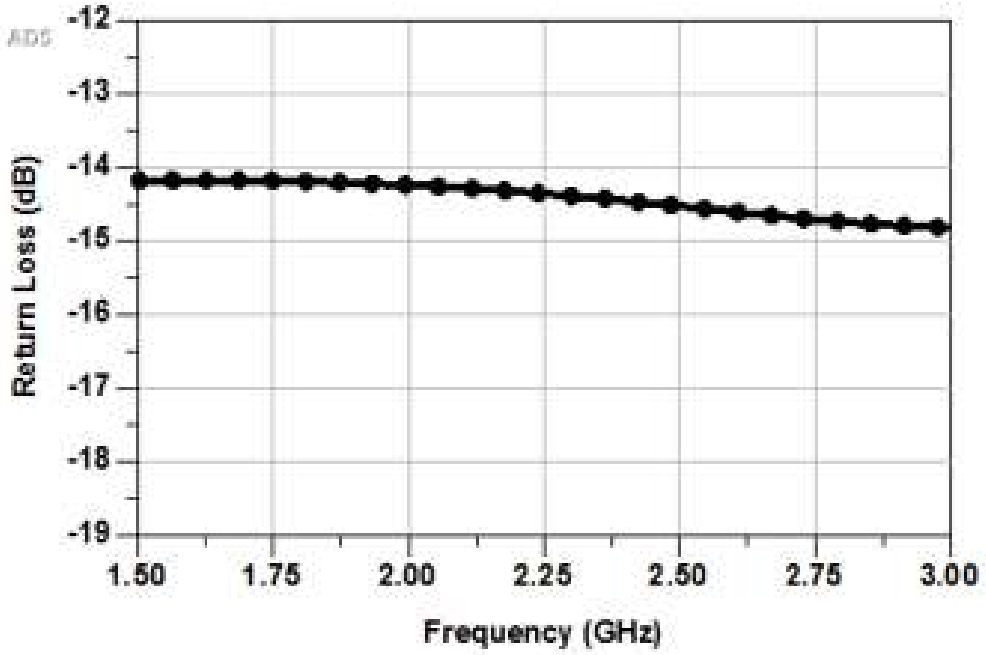



Figure 5-4. Return loss of active balun

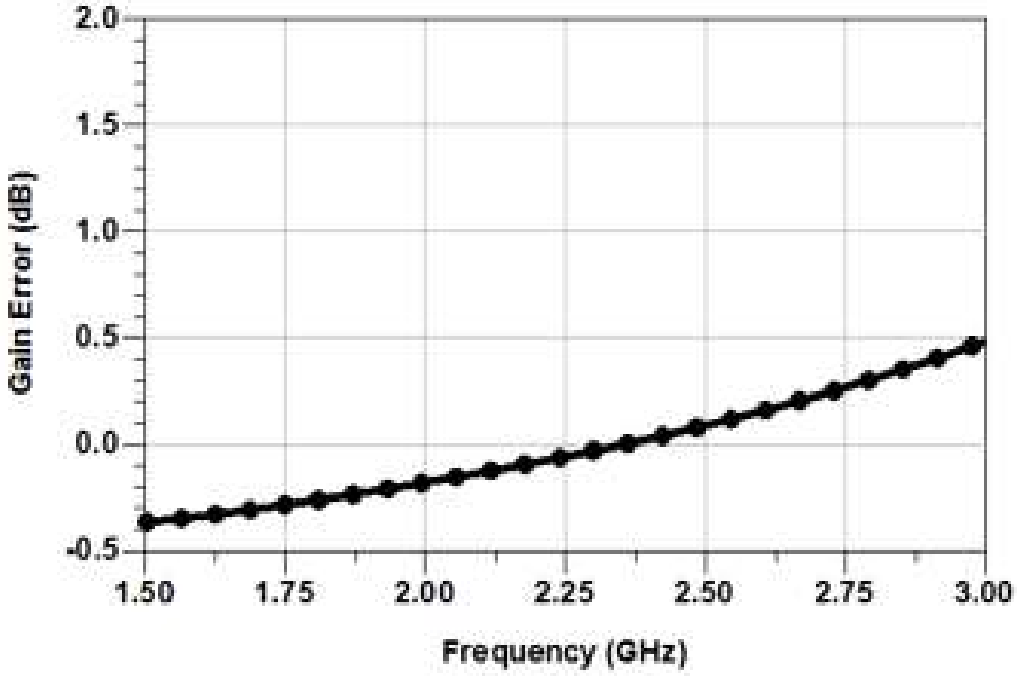



Figure 5-5. Gain error of active balun

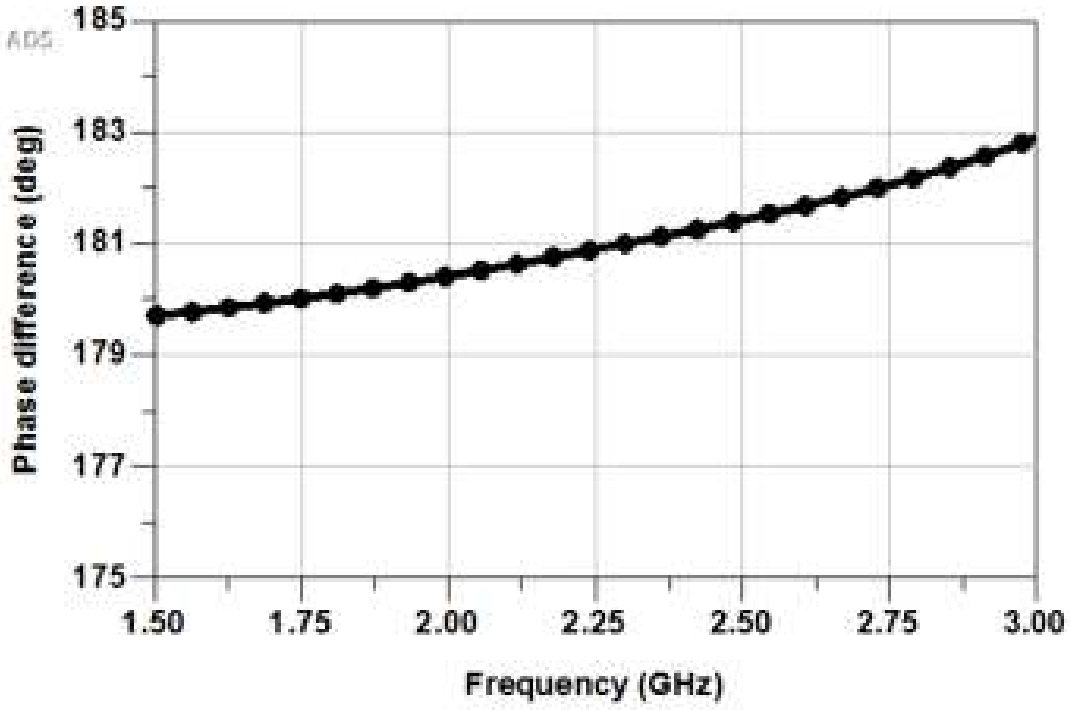



Figure 5-6. Phase difference of active balun

### 5.3 Active Inductor Loaded All-Pass Network

To utilize the active inductor circuit shown in Fig. 5-7 within the all-pass network for phase shifting purposes, the first step is to determine the inductance variation required to achieve a 180° phase shift range within the frequency band of interest. For this, the following design equations reported in [5.1] can be employed

$$L = \frac{p.Z_0}{\omega}$$

$$p = \frac{1}{2}\tan\left(\frac{\phi}{4}\right) + \sqrt{1 + \frac{1}{4}\tan\left(\frac{\phi}{4}\right)^2} \tag{5.5}$$

where $Z_0$ is the characteristic impedance and $\phi$ denotes the phase shift in radians. Equation (5.5) shows that there is a linear relationship between the value of the characteristic impedance $Z_0$ and the inductance value *L*. For 1.5 GHz operation and 180° phase shift, a 50 Ω characteristic

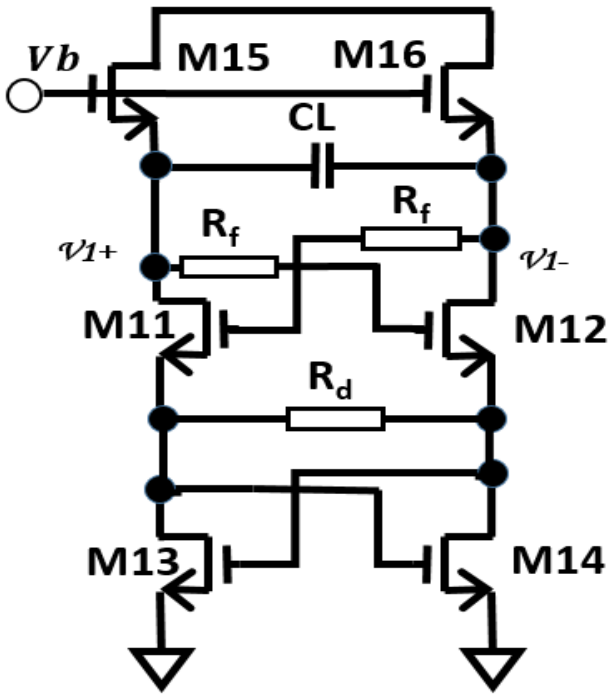



Figure 5-7. Differential active inductor (DAI)

impedance results in an inductance tuning range from 3.2 nH to 8.6 nH, whereas a 25 Ω characteristic impedance requires an inductance tuning range from 1.6 nH to 4.3 nH. Since the active inductor loaded all-pass network is preceded by the active balun and followed by the output VGA/buffer, it does not directly interact with the external 50 Ω connections and allows the freedom of choosing a lower characteristic impedance to minimize the required active inductance tuning range. Consequently, the all-pass network was designed with a 25 Ω impedance with the required inductance tuning range being 1.6 nH to 4.3 nH and 0.9 nH to 2.2 nH at 1.5 GHz and 3 GHz, respectively.

Having determined the required inductance variation range, the procedure described in Chapter 4 is used to design the active inductor loaded all-pass network. Equations (4.2) – (4.7) are used as a starting point in the initial stages of the inductor design. M11 and M12 are the most critical transistors forming the core of the gyrator-c network based active inductor concept. Table 5.1 summarizes how the transconductance variation of these transistors affects the active inductance, series resistance, and frequency range. The well-known equation $gm = \sqrt{2K(W_{11,12}/L_{t_{11,12}})I}$ (where $K$ is the process transconductance parameter, $W$ is transistor width and $L_t$ is transistor length, $I$ is the bias current) relates transconductance to the transistor size and bias current. Changing the bias current to change transconductance for inductance tuning also affects the operational frequency range of the inductor and therefore the frequency range needs to be adjusted by properly sizing the M11 and M12 transistors. It is also assumed that the series and parallel capacitances of the all-pass network, denoted by $Cs$ and $Cp$ in Figure 5-1, are in parallel with the parasitic capacitances of the transistors and contribute to $C_L$ thereby impacting the inductance value. (The values of $Cs$ and $Cp$ are 1.8 pF and 6.8 pF, respectively, as determined from [5.1] at the center frequency of 2.25 GHz). Hence, although [5.1] is useful for estimating a transconductance range, the transistor sizing and achievable inductance tuning range via bias current control must be investigated by utilizing circuit and layout models associated with the fabrication process to account for critical parasitic effects. In doing so, the quality factor and operational frequency range of the active inductor must also be considered since the transistor sizes can be reduced to increase L but this in turn impacts $R_s$ and $\omega z$ as indicated in (4.2) and (4.4). Consequently, the M11 and M12 sizes are best determined through circuit and layout modeling. In these modeling steps, the inductance value is extracted from the S-parameters of the entire all-pass network. Specifically these transistors exhibited $gm_{11,12}$ = 0.9 mS and $gm_{11,12}$ = 2.8 mS at

the 850 μA and 2.7 mA bias current levels. Transistors M15 and M16 serve as current mirrors to vary the $gm$ of M11 and M12 to tune the inductance.

Table 5.1
Effects of Varying Transconductance and Feedback Resistance on Performance of the Tunable Active Inductor

| $\boldsymbol{gm}$ | $\boldsymbol{L}$ | $\boldsymbol{R_s}$ | $\boldsymbol{\omega p}$ | $\boldsymbol{\omega z}$ |
|---|---|---|---|---|
| ↑ | ↓ ↓ | ↓ ↓ | ↑ | ↓ |
| ↓ | ↑ ↑ | ↑ ↑ | ↓ | ↑ |
| $\boldsymbol{R_f}$ | $\boldsymbol{L}$ | $\boldsymbol{R_s}$ | $\boldsymbol{\omega p}$ | $\boldsymbol{\omega z}$ |
| ↑ | ↓ | ↓ | ↑ | ↓ ↓ |
| ↓ | ↑ | ↑ | ↓ | ↑ ↑ |

Once M11 and M12 sizes are determined to achieve the necessary inductance values, the next design step is to minimize the series resistance of the equivalent RF network in an effort to further increase the quality factor of the active inductor. In the DAI network shown in Figure 5-7, transistors M13 and M14 form the negative resistance network and they are customarily sized to be identical with equal transconductance. Since sources of the active inductor transistors and drains of the negative resistance transistors are connected to each other (e.g., M11 and M13), they are biased with the same current. Therefore, the smallest bias current (i.e., 850 μA) used to tune the inductor results in the largest absolute value of negative resistance as can be observed in (4.6) with the opposite occurring for the largest bias current (i.e., 2.7 mA). Hence, transistors M13 and M14 are sized to produce a negative resistance to minimize the series resistance of the network under the 850 μA bias current condition. Specifically, the transistor sizes were determined in a way to keep the total series resistance of the entire all-pass network slightly above zero (~5 Ω) in order to

increase the quality factor while retaining a positive resistance margin to prevent the occurrence of oscillations due to fabrication tolerances. Stability simulations were also conducted and $R_d$ of 100 Ω was added to the network to ensure unconditional stability. It is important to note that addition of $R_d$ does not impact the $Q$ performance as it is in parallel with the total series resistance. Since the negative resistance circuit is also in parallel with the active inductor, it has a minimal impact on the inductance value and its frequency behavior.

Once the above procedure is completed for achieving the inductance tuning range at the center frequency, the entire tunable active inductor circuit must be investigated for its frequency dependent behavior. This observation reveals that the frequency range should be enhanced by introducing the feedback resistors $R_f$ shown in Fig. 5-7 as described in Chapter 4. Since the feedback resistors change the voltage attenuation factor $\alpha$, the achievable inductance tuning range is also impacted as indicated by (4.7). Moreover, the desired inductance tuning per control voltage is not identical across the frequency band as already mentioned. This necessitates parametric studies and optimizations to achieve the desired inductance tuning across the operation bandwidth while maintaining the quality factor and stability performance. The value of $R_f$ was determined as 70 Ω from simulation. Table 5.2 shows the transistor sizes of the optimized circuit.

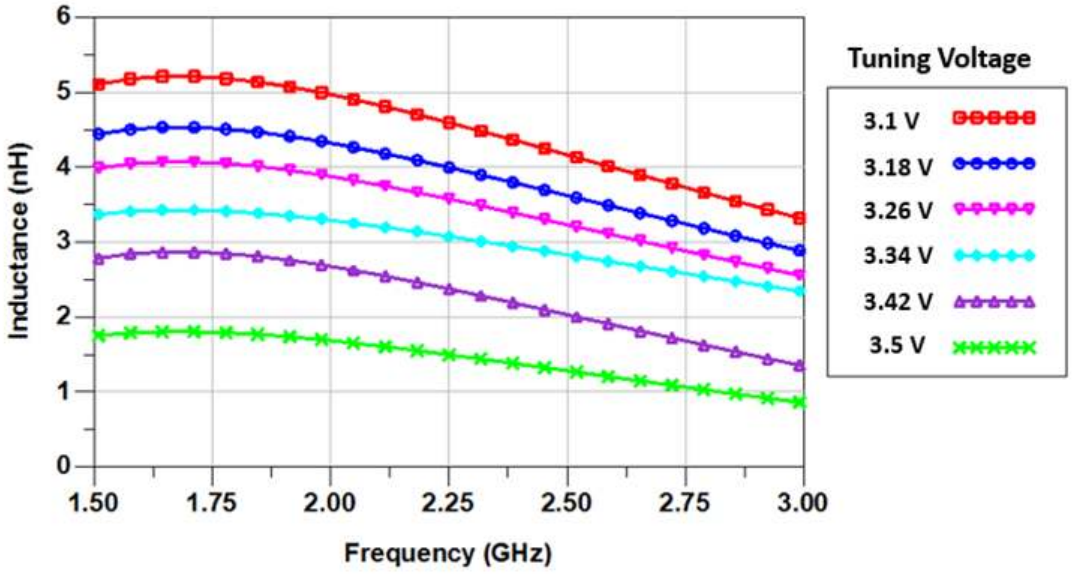
Table 5.2
Transistor Sizes of the Optimized Tunable Active Inductor

| **Transistor** | **W/L$_t$, µm/µm** | **Number of Fingers** |
|---|---|---|
| M11, M12 | 130/0.5 | 2 |
| M13, M14 | 50/0.5 | 2 |
| M15, M16 | 100/0.5 | 2 |

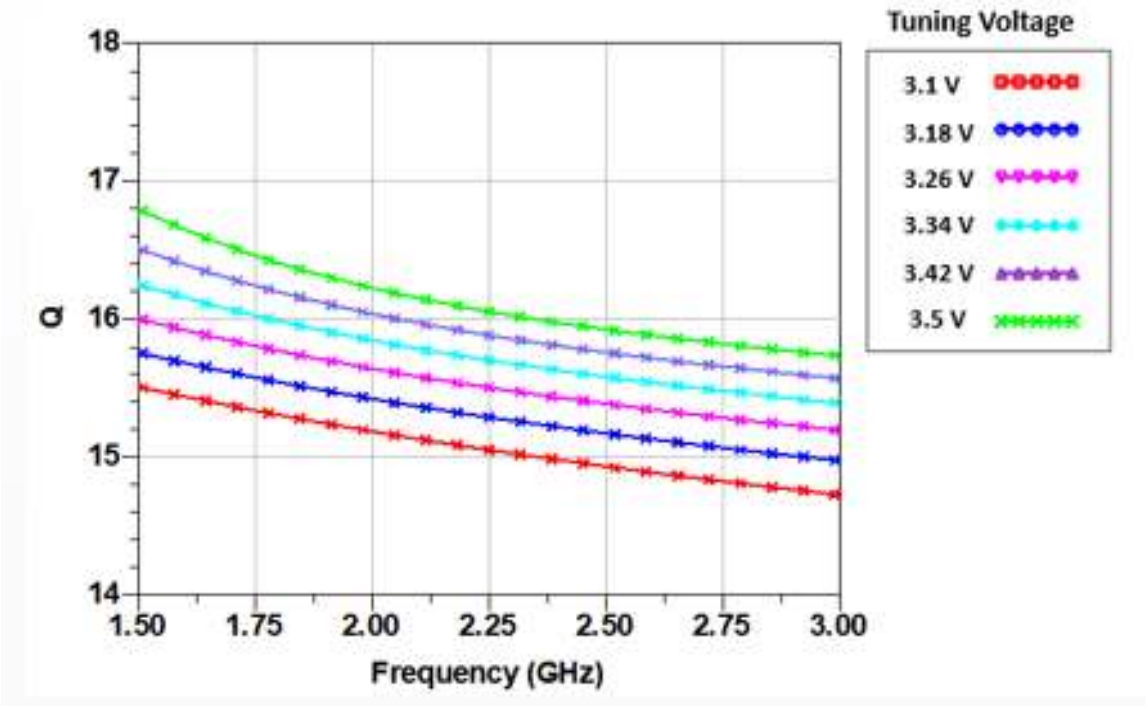
Full-wave layout simulations were performed using the Keysight ADS Momentum suite to account for parasitic effects. Optimization of the transistor size as mentioned previously resulted in achievement of the desired tuning range of inductance over a frequency range from 1.5 GHz to 3 GHz as shown in Figure 5-8(a) for tuning voltage varying from 3.1 V to 3.5 V. Unconditional stability was achieved with a stability factor > 1 and stability measure > 0 across the entire frequency range. The quality factor is shown in Figure 5-8(b). It ranges from 14.8 to 17.5. These simulation results demonstrate that this approach can be used as an alternative to passive inductors in applications where inductance tunability is advantageous, such as in the design of tunable all-pass or matching networks.

**5.4 Output VGA/Buffer**

The last stage of the functional block diagram consists of VGA/buffer circuits as shown in Figure 5-9. The first block of the circuit is a common gate amplifier that provides a constant 25 Ω load impedance to the output of the active tunable inductor loaded all-pass network. It has a cascode to provide better isolation. Given that the input impedance of the common gate amplifier M17 is approximately equal to $1/gm_{17}$ the impedance value can be set by adjusting bias current and/or transistor size. The operating point is adjusted using the bias at the source terminal which in this case is implemented by using a resistor $R_{bias2}$ that sets the bias current of M17. The transistor size used was $W/L_t$ = 33 µm/0.5 µm with two fingers. $R_{bias2}$ is selected as 700 Ω for a

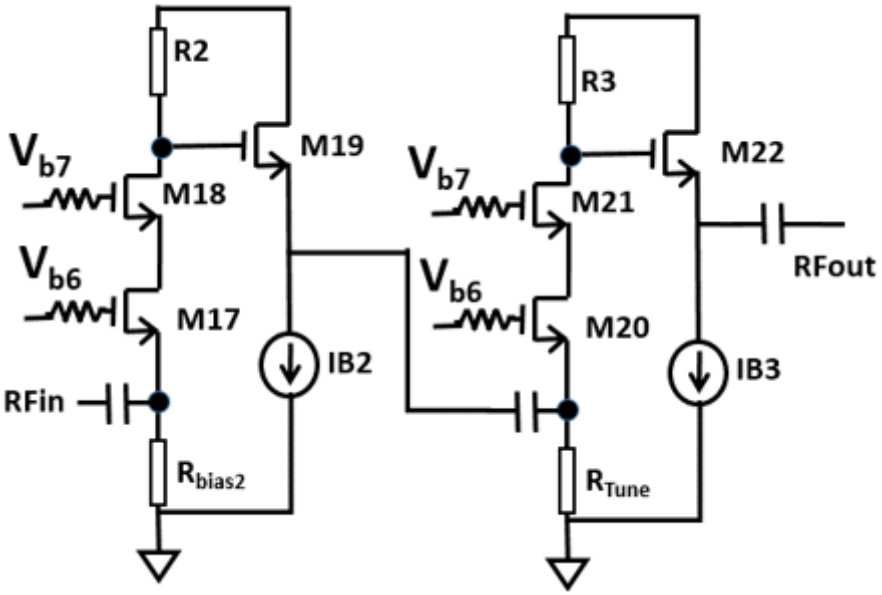



(a)

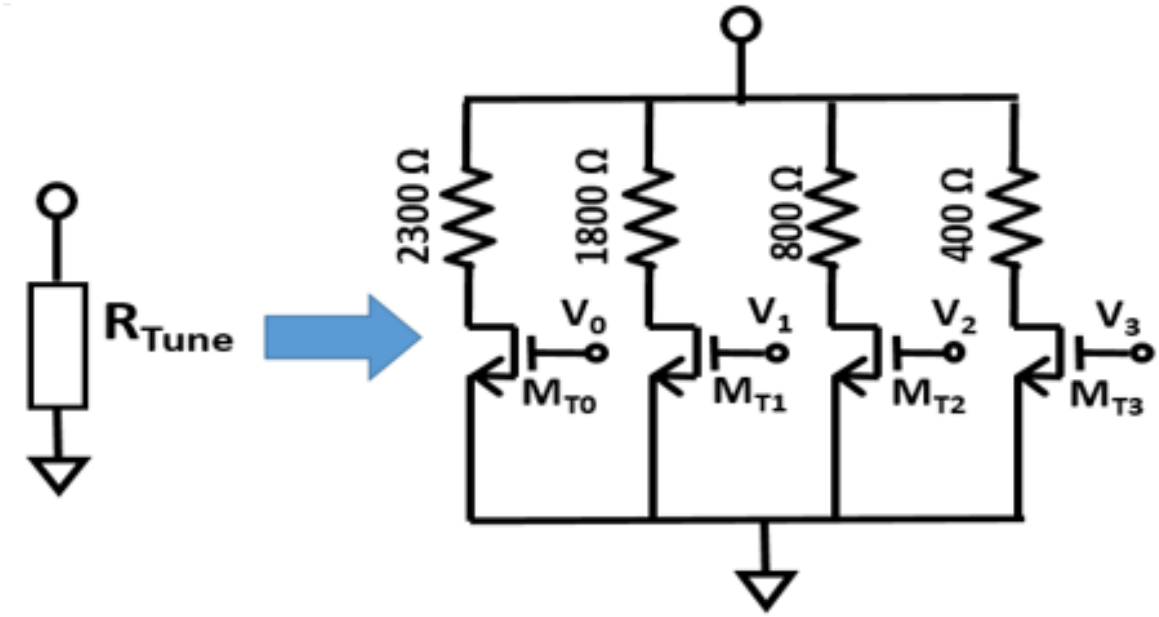



(b)

Figure 5-8. Inductance tuning range (a) and quality factor variation (b) of DAI




(a)




(b)

Figure 5-9. Circuit schematics of the output VGA/buffer (a) and resistive network (b).

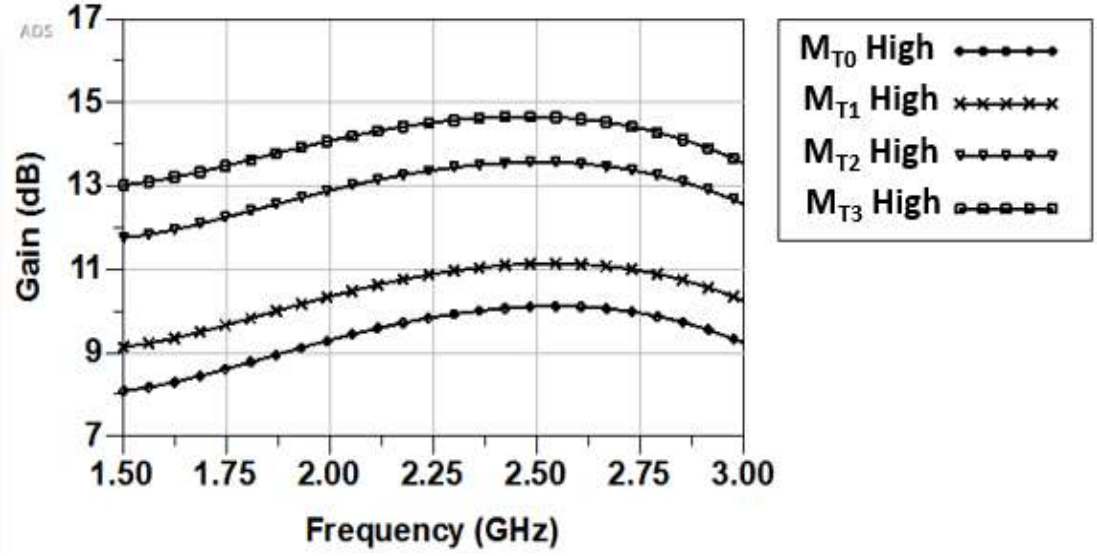
bias current of 1.2 mA. M18 and M19 are sized the same as M17 with $V_{b6}$ set to 1.4 V and $V_{b7}$ set at 2.5 V. The second block of the circuit is another common gate amplifier similar to the first but

with a variable resistance at the source (i.e., source of transistor M20) to tune the gain for compensating the $S_{21}$ variations across the different phase shift values. The resistive tuning network is shown in Figure 5-9(b) and consists of four parallel resistors that can be used as $R_{Tune}$ by activating appropriate switches $M_{T0}$-$M_{T3}$ ($W/L_t$ = 50 µm/0.5 µm with number of fingers = 2). The different resistor values vary the bias current through the common gate amplifier M20 and can be used to vary the voltage gain, which in a first order approximation becomes

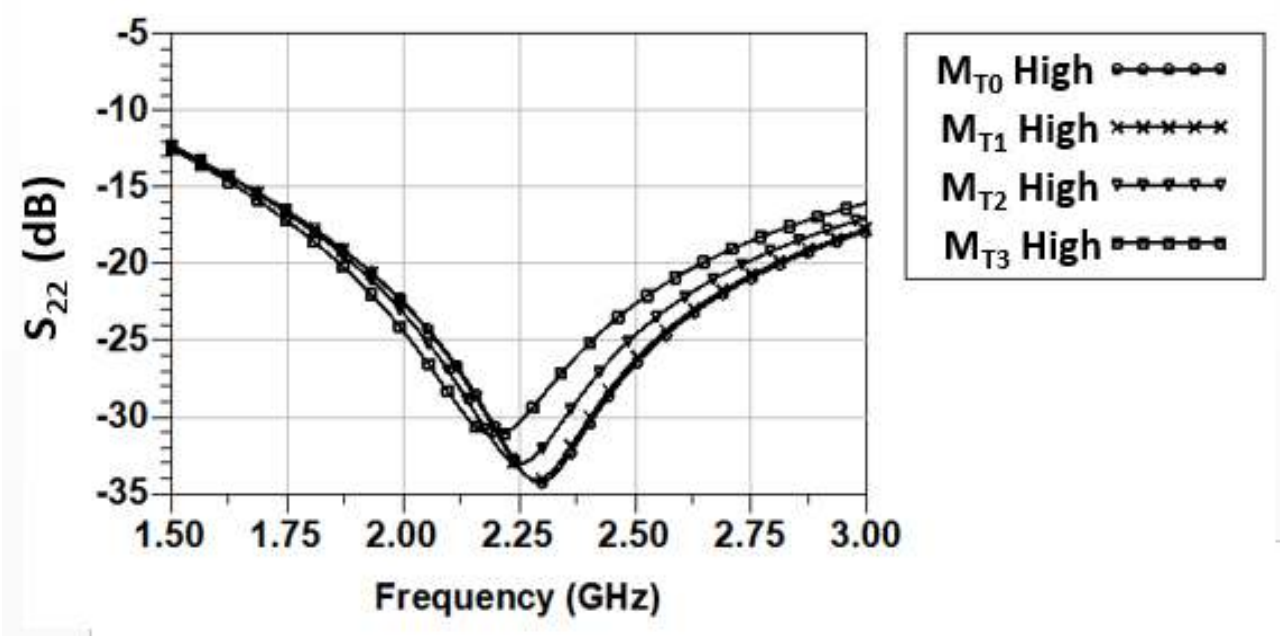
$$Av \approx gm_{20} \times R3 \tag{5.6}$$

Based on the resistor value chosen, the bias current varies from 0.4 mA to 3.5 mA for a voltage gain variation from 8 dB to 15 dB. Within this range, using the 4 resistor network, 15 discrete gain steps are available with ~0.5 dB steps. The output buffer is designed to provide a wideband 50 Ω match at the output using the same approach pursued at the input of the common gate amplifier. However, transistor M22 is sized as $W/L_t$ = 20 µm/0.5 µm with number of fingers = 2 and a bias current of 3 mA to achieve a 50 Ω output impedance. Bias current sources IB2 and IB3 are implemented using common source transistors (15µm/0.5µm, number of fingers = 2) with external voltage applied to the gate, both providing 3 mA bias current. The simulated performance of the VGA/buffer layout is shown in Figure 5-10. The complete schematic of the entire phase shifter is shown in Figure 5-11 where all components and interconnects are implemented on chip. The simulated phase shift performance of the designed layout is shown in Fig. 5-12. Greater than 360° phase shift is achieved across the entire frequency range with a mean gain of 11 dB and maximum gain error of 1.5 dB. The simulated input and output return losses are >13 dB across the entire frequency range. The all-pass network as a stand-alone unit is bidirectional which with implementation of double-pole double-throw switches could also be used in a transceiver. The success achieved with the simulated performance motivated the experimental verification of the

designed phase shifter as detailed in the following section. Figure 5-13 shows the final completed layout of the phase shifter.




(a)




(b)

Figure 5-10. Simulated gain (a) and $S_{22}$ (b) of the designed VGA/buffer circuit

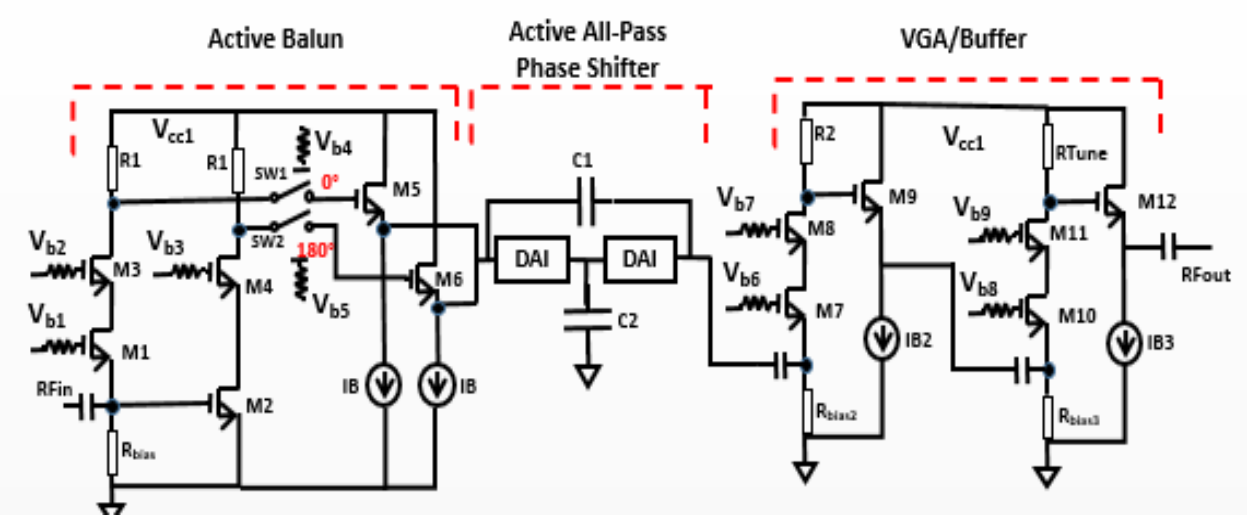



Figure 5-11. Expanded circuit schematic of the phase shifter. DAI schematic is given in Fig. 7

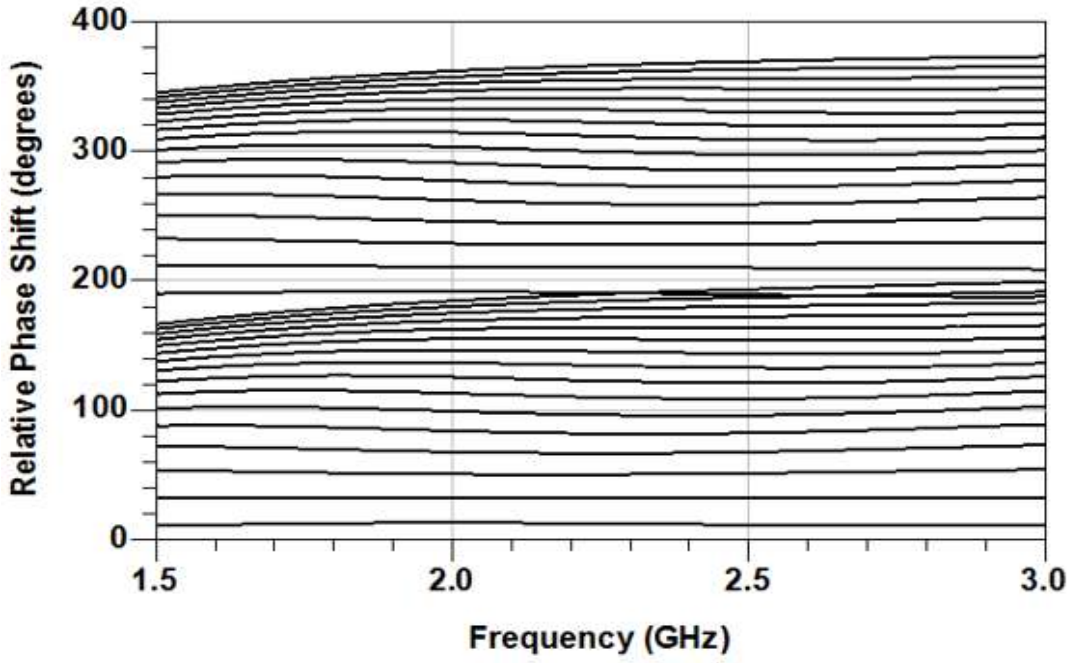



Figure 5-12. Simulated phase shift performance from the designed layout.

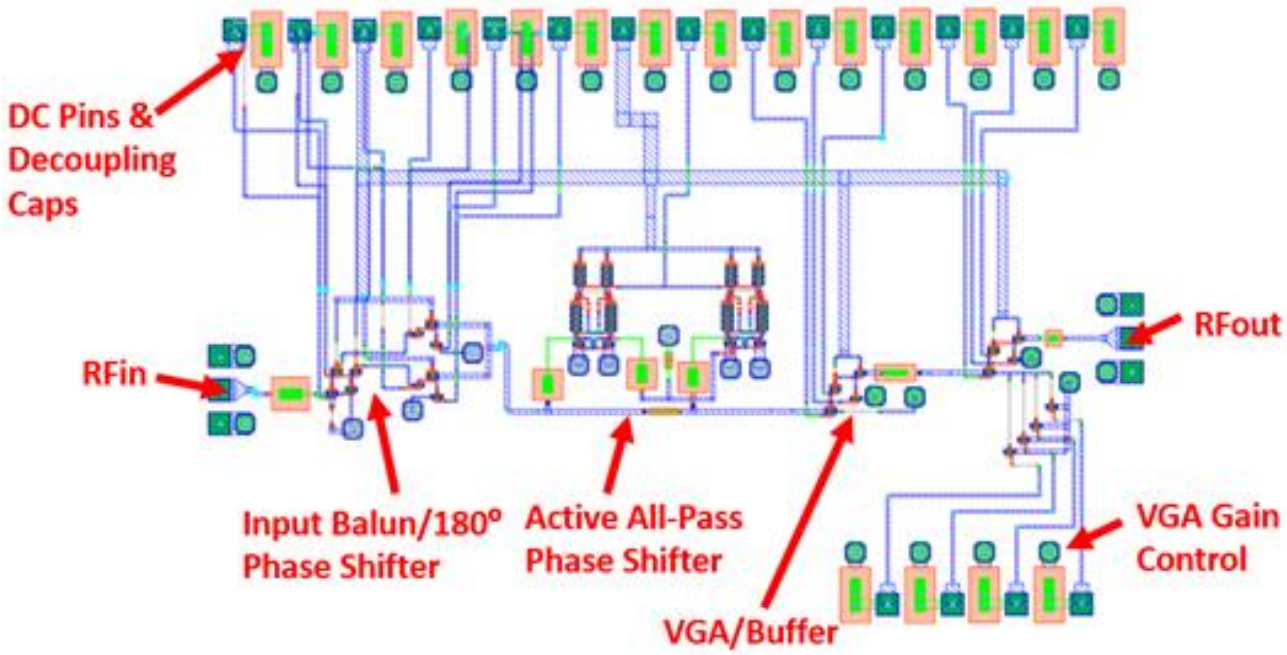
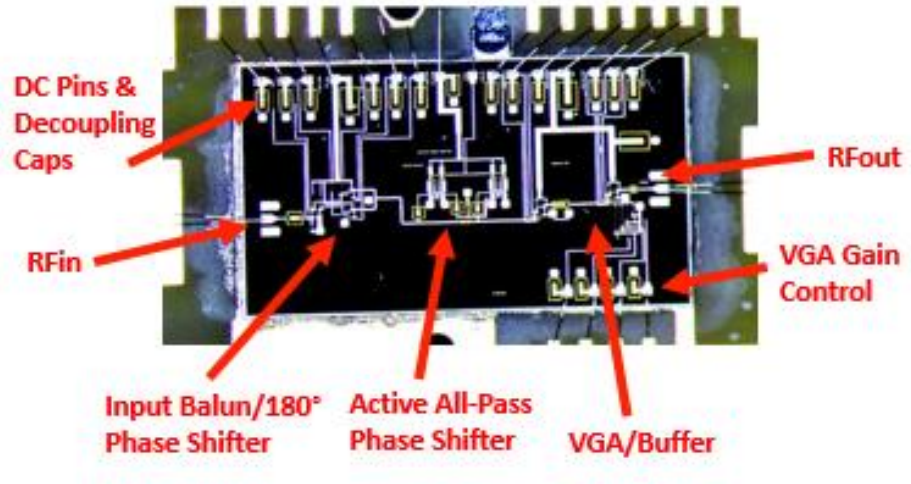



Figure 5-13. Layout of the complete phase shifter.

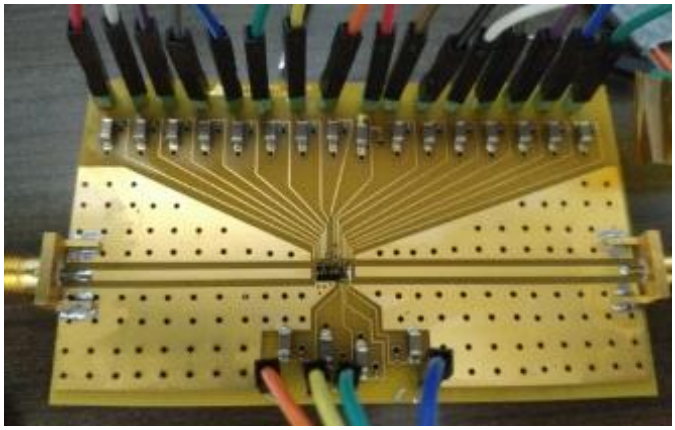
### 5.5 Experimental Verification

The phase shifter was implemented in the 0.5 µm Triquint TQPED GaAs process with a chip size of 2.7 × 4.5 $mm^2$ including all bias lines and bond pads (1 × 3.95 $mm^2$ without the bond pads (see Figure 5-14(a)). The chip is mounted on a test board (see Figure 5-14(b)) that utilizes grounded coplanar waveguides for input/output RF excitations and narrower conductive traces for DC bias and control. The test board is an 8.1 × 4.8 $cm^2$ 0.79 mm thick FR4 board. All traces on the test board were fabricated using 1 oz. copper with Electroless Nickel Electroless Palladium Immersion Gold (ENEPIG) surface finish to allow for the addition of wire bonds. The RF input and output pads of the chip are wedge wire bonded to the test board with two parallel 18 µm diameter gold wires to minimize the parasitic series inductance associated with the wire bonds. The 20 pF decoupling capacitors of the circuit are implemented on chip. The test board also utilizes 1 µF 0603 and 0.1 µF 0201 sized surface mount decoupling capacitors in order to provide low frequency filtering and a low impedance path to ground for any high frequency signals on the dc

bias lines. 50 Ω SMA connectors are attached to both the input and output RF ports to facilitate the measurements while the four wire gain of the VGA. The top part of the board consists of DC




(a)

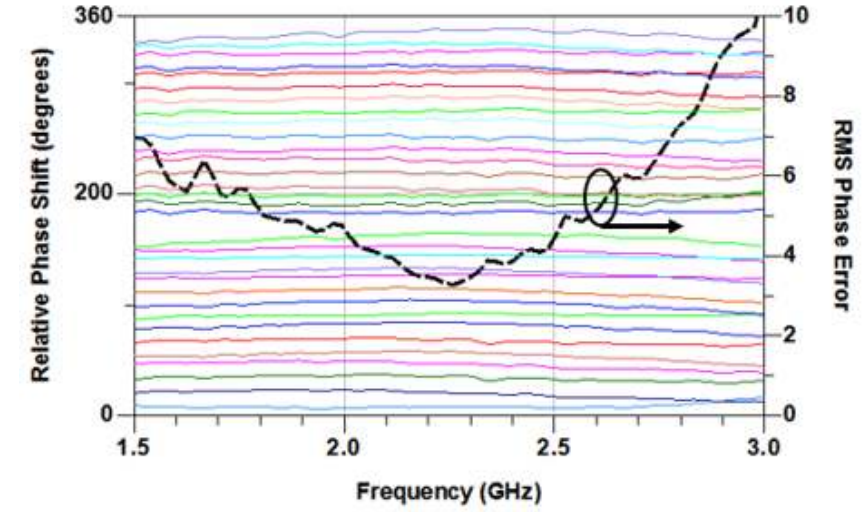


(b)

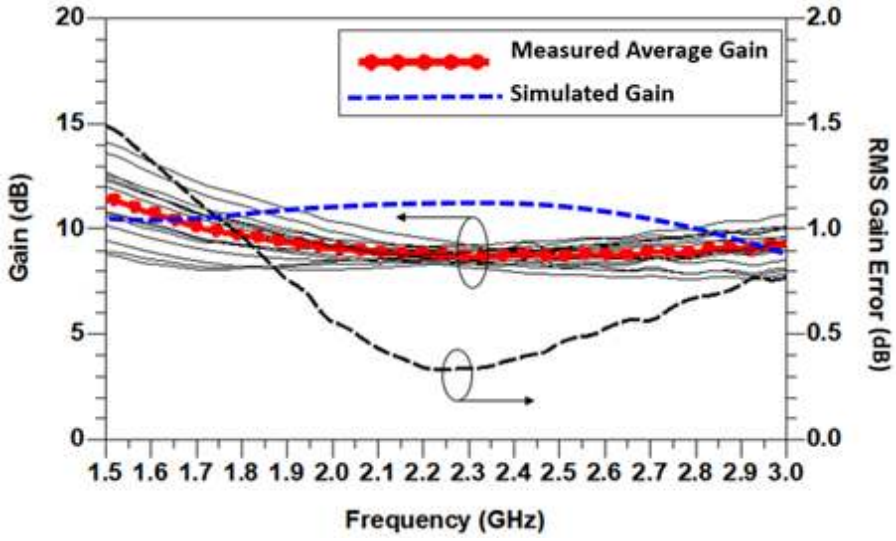
Figure 5-14. Fabricated phase shifter: (a) microphotograph; (b) test board

bias connections used to bias $V_{b1\text{-}9}$ and $V_{cc1}$ in Figure 5-11 as well as to vary the tuning voltage $V_b$ of the active inductor (Figure 5-7). The gain is varied via the VGA to minimize gain errors around the center frequency of 2.25 GHz. The VGA settings used for each phase shift state are derived

from the circuit and layout simulations and depend on the gain variation between reference and phase state.

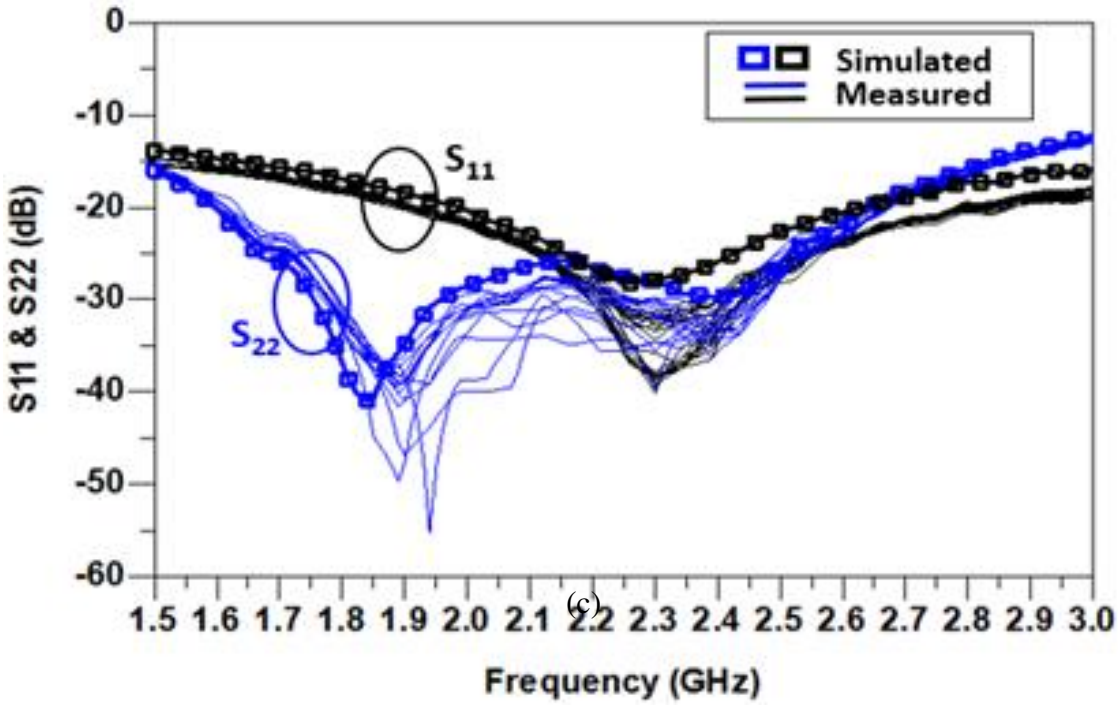



(a)




(b)

Figure 5-15. Measured performance of the fabricated phase shifter: (a) Phase response and RMS phase error; (b) Gain and RMS gain error; (c) $S_{11}$ and $S_{22}$.




(c)

Figure 5-15. (Continued)

Figure 5-15(a) shows the measured phase response covering the entire $360^0$ range as well as the RMS phase error. The input balun/180° phase shifter was set to the 0° phase shift option by activating switch SW1 in Figure 5-11. The tuning voltage of the active inductor ($V_b$ Figure 5-7) was varied in 30 mV increments from 3.1 V to 3.5 V for phase shifts up to 180°. To achieve the next consecutive 180° phase shift for a full 360°, switch SW2 of 180° phase shifter was activated instead of SW1. The RMS phase error is calculated using [5.2]

$$\theta_{\Delta,RMS} = \sqrt{\frac{1}{N-1} \sum_{i=2}^{N} |\theta_{\Delta i}|^2} \tag{5.7}$$

where $N$ is the number of phase states used to achieve a 360° phase shift and $\theta_{\Delta i}$ is the phase difference between simulated and measured phase shift for 32 distinct phase states equivalent to a 5 bit phase shifter. The RMS phase error ranges from 5° to 9° over the entire frequency range. Results observed in Fig. 5-15(a) show that phase shift is not uniform across the entire frequency range.

For instance, from 1.5 GHz to 2.0 GHz there is not coverage from approximately 150° to 180°. However, it should be remarked that the presented design is a continuous phase shifter and finer phase tuning can be achieved with smaller voltage increments. In addition, it is important to note that a more robust solution could also be achieved by cascading another all-pass network stage and designing these all-pass networks for different center frequencies within the 1.5 GHz to 3 GHz frequency range. This cascading approach would decrease the inductance requirements and result in a flatter phase response, but would also require larger chip area and power consumption. Figure 5-15(b) shows the measured gain for the different measured phase shift states depicted in Figure 5-15(a) along with the average gain. The measured RMS gain error, calculated using

$$A_{\Delta,RMS}\sqrt{\frac{1}{N}\ \sum_{i=1}^{N}|A_{\Delta i}|^2} \tag{5.8}$$

is also shown in Figure 5-15(b) where $A_{\Delta,RMS}$ is the RMS amplitude error. RMS gain error <1.5 dB was obtained. Figure 5-15(c) presents the measured $S_{11}$ and $S_{22}$ performances of the phase shifter. The difference between measured and simulated gain can be attributed to additional losses of RF traces on the test board, as these were not accounted for in simulation. These data demonstrate that impedance matching is satisfied with >15dB return losses across the frequency range and are independent of the phase shifter state due to the functionalities of the active balun acting as an input buffer and VGA cascaded with an output buffer. Measured results show an input 1 dB compression point (P1dB) of -1 dBm and -2 dBm at 1.5 GHz for the low and high gain settings of the VGA, respectively. At 3 GHz, the measured P1dB is -1 dBm and 0 dBm for the low and high gain settings of the VGA, respectively. As an example, Fig. 5-16 presents the measured P1dB performance at 3 GHz for the high gain setting of the VGA and demonstrates a P1dB value of 0 dBm. The total current consumption of the active balun, active tunable inductor

loaded all-pass network and output VGA/buffer is 8 mA, 3.4 mA and 8 mA, respectively. The DC supply voltage is 4 V and results in a total power consumption of 78 mW for the phase shifter.

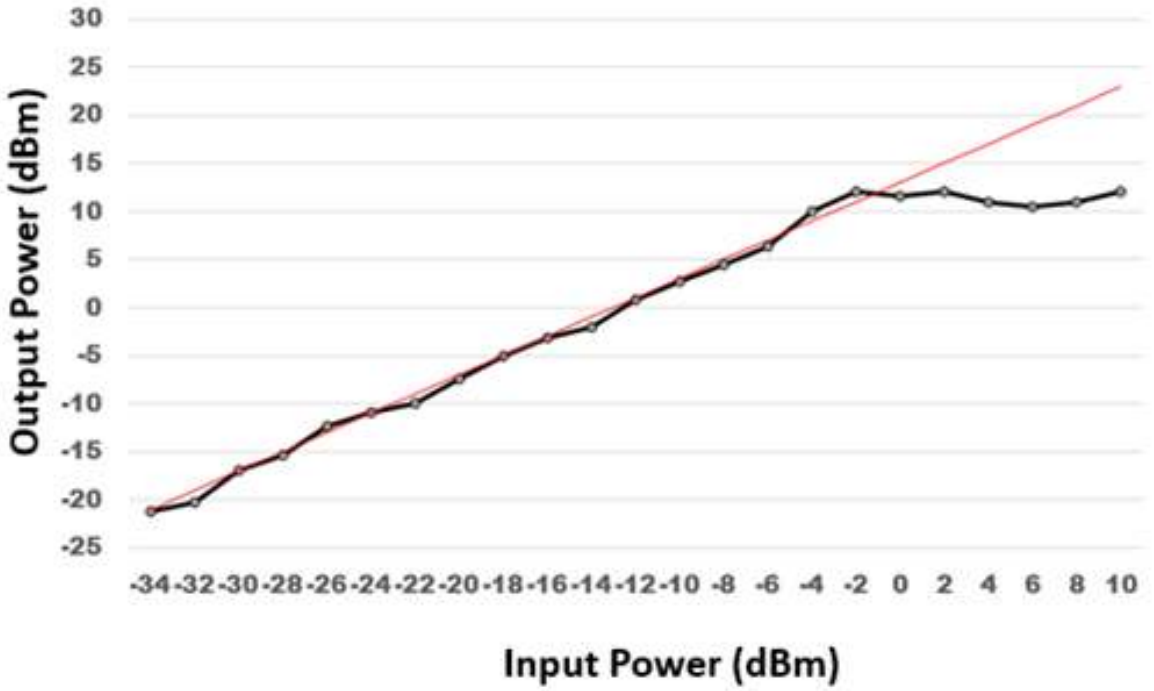



Figure 5-16. Measured P1dB performance at 3 GHz for high gain setting.

Table 5.3 summarizes the measured performance of the phase shifter and compares it with performances of the previously published state-of-the-art MMIC phase shifters that are tailored towards L and S band applications. The 67% fractional bandwidth of the presented design outperforms that of the others given in the table. Its footprint is only larger than the phase shifter presented in reference [31]-[33]. However, as compared to these, the presented phase shifter exhibits 10 dB gain in addition to its significantly larger bandwidth. The RMS gain error is on-par with the other phase shifters. The RMS phase shift error is larger than desired but can potentially be reduced in future iterations with the addition of a 90° phase shifter in conjunction with the 180° balun already used. This design change would require less tuning range in the active inductor. The phase shifters presented in [29] and [30] provide large gains, however they also occupy more chip

area than the presented design. In addition, power consumption of the phase shifter in [29] is 500 mW, which is more than six times the consumption of the presented design. Measured results show an output P1dB of 12 dBm which is similar to [29] and [30] but less than the passive design in [31] which has 6.5 dB insertion loss. Reference [33] has an output P1dB of -27.3 dBm but operates at a higher frequency.

Table 5.3 Performance Comparison

| | [29] | [30] | [31] | [32] | [33] | This work |
|---|---|---|---|---|---|---|
| Technology | 0.5 um pHEMT | 0.5 um pHEMT | 0.5 um pHEMT | 0.18 um CMOS | SiGe | 0.5 um pHEMT |
| Frequency (GHz) | 1.8 – 3.2 | 2.5 – 3.5 | 0.85 – 1.15 | 3.4-3.5 | 10-13 | 1.5 - 3 |
| Phase Control | 360°/6 bits | 360°/6 bits | 360°/5 bits | 360°/6 bits | 360° /4 bits | 360° /5 bits |
| Gain (dB) | 26 | 26 | -6.5 | -5.4 | 3.7 | 10 |
| RMS Phase Error (deg.) | < 6 | < 3 | < 7 | 3 | - | < 9 |
| RMS Gain Error (dB) | <1 | - | < 1.5 | -2 | - | < 1.5 |
| Power (mW) | 500 | not reported | not reported | - | 54 | 78 |
| $P_{out}$1dB (dBm) | 12 | 13 | 21 | - | -27.3 | 12 |
| Fractional Bandwidth (%) | 56 | 22 | 10 | 3 | 6 | 67 |
| Size ($mm^2$) | 4 × 4 | 5.5 × 5.5 | 1.87 × 0.87 | 1.2 x 2.3 | 1.92 x .78 | 2.7 × 4.5 |

## 5.6 References


[5.1] X. Tang and K. Mouthaan, "Design of large bandwidth phase shifters using common mode all-pass networks," *IEEE Microw. Wireless Compon. Lett*., vol. 22, no. 2, pp. 55–57, Feb. 2012.

[5.2] T. Chen, S. Rodriguez, E. Alarcon, and A. Rusu, "A 2 GHz - 8.7 GHz Wideband Balun-LNA with Noise Cancellation and Gain Boosting," in *Proc. of IEEE Ph.D Research in Microelectronics and Electronics (PRIME)*, 2012.

[5.3] S.-C. Chou, F.-C. Huang, and C.-K. Wang, "A 60 GHz wideband active balun using magnitude and phase concurrent correction technique in 65nm CMOS," *IEEE Asian Solid-State Circuits Conference*, 2012, pp. 273-276.

[5.4] S. C. Blaakmeer, E. A. M. Klumperink, D. M. W. Leenaerts, and B. Nauta, "Wideband balun-LNA with simultaneous output balancing, noise-canceling and distortion-canceling," *IEEE J. Solid-State Circuits*, vol. 43, pp. 1341–1350, Jun. 2008.

# Chapter 6:

# Conclusion and Future Work

## 6.1 Summary and Conclusion

A broadband S- and L- band 4-bit all-pass passive phase shifter was designed using a commercially available GaAs process. Each bit in the sequence consisted of three stages. Three stages per bit was found to be necessary to provide the required phase shift over frequency and found to be an optimum tradeoff between bandwidth, insertion loss and chip size. To compensate for the loss in the network, wideband amplifiers were placed between the stages. The amplifiers were designed as low noise wideband amplifiers using simultaneous noise and power match techniques. The complete system resulted in a chip size of 6800 um x 4900 um which was the maximum allowed by the foundry. The chip passed the initial DC test but failed the functionality test giving acceptable results for input/output return loss but not for insertion loss and phase shift. The root cause of the functionality test failure was caused by spiral mutual inductance and coupling effects from the close proximity of the 60 inductors! The EM model inaccuracies and high coupling between the inductances which are very close to each other due to compact layout caused the difference between post layout simulation and measurement results.

To eliminate the bulky inductors in the all-pass phase shifters responsible for the failure of the first design, a novel compact and wideband phase shifter concept based on tunable active inductor loaded all-pass networks has been introduced and experimentally verified for potential S and L band applications. Specifically, the presented phase shifter has $1 \times 3.95$ mm$^2$ die area without bond pads and operates within the 1.5 GHz to 3 GHz band with 10 dB gain, less than 1.5 dB RMS gain

error and less than 9° RMS phase error. A comparison with the state-of-the-art MMIC phase shifters operating in S and L bands demonstrates that the presented phase shifter exhibits a remarkable bandwidth performance from a very compact footprint with low power consumption. Although the phase shifter is implemented using a GaAs MMIC process, the concept is suitable to be implemented on silicon processes as the functionality of the active inductors has already been successfully verified. In addition, the compact circuit area of the presented concept is promising to include additional all-pass network segments within the design to further increase the bandwidth performance, potentially to cover a decade or more.

### 6.2 Future Work

Measured results as shown in Fig. 5-12 demonstrate the limits of achievable phase shift of the active phase shifter. Results observed in Fig. 5-12 show that phase shift is not uniform across the entire frequency range. For instance, from 1.5 GHz to 2.0 GHz there is not coverage from approximately 150° to 180°. However, it should be remarked that the presented design is a continuous phase shifter and finer phase tuning can be achieved with smaller voltage increments. In addition, it is important to note that a more robust solution could also be achieved by cascading another all-pass network stage and designing these all-pass networks for different center frequencies within the 1.5 GHz to 3 GHz frequency range. This cascading approach would decrease the inductance requirements and result in a flatter phase response, but would also require larger chip area and power consumption. These limits are based on the limitations of the tunable inductor to provide the required inductance. One way to improve this and obtain lower RMS phase error for phase shifte between 90° and 180° would be to include a discrete (digital) 90° phase shifter to function similarly to the 180° balun/phase shifter. This would ease the tuning

requirements on the active inductor since the maximum tuning range required would be 90° instead of 180° as shown in Fig. 6-1.

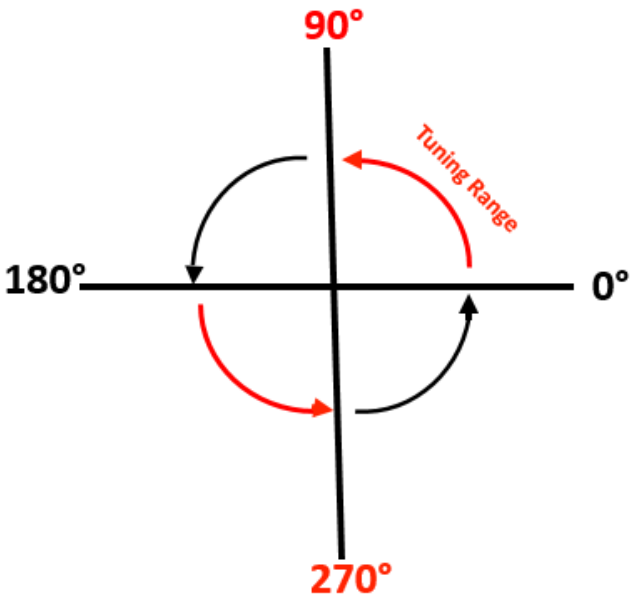



Figure 6-1. Tuning range of active all-pass filter with digital 90° phase shifter

Polyphase RC filters are commonly used for this purpose but they are narrowband so cannot be used in this application. One way of achieving the 90° phase shift over a wide bandwidth would be using a coupled transmission lines. For MMIC applications, this could be implemented using broadside couplers which make use of the different metal layers included in the design kit. A broadside coupler was designed for proof of concept using the same TQPED GaAs process as shown in Fig. 6-2 using the M2 and M3 metal layers. Switches at port 2 and port 3 could be implemented as was done with the balun to control desired phase shift.

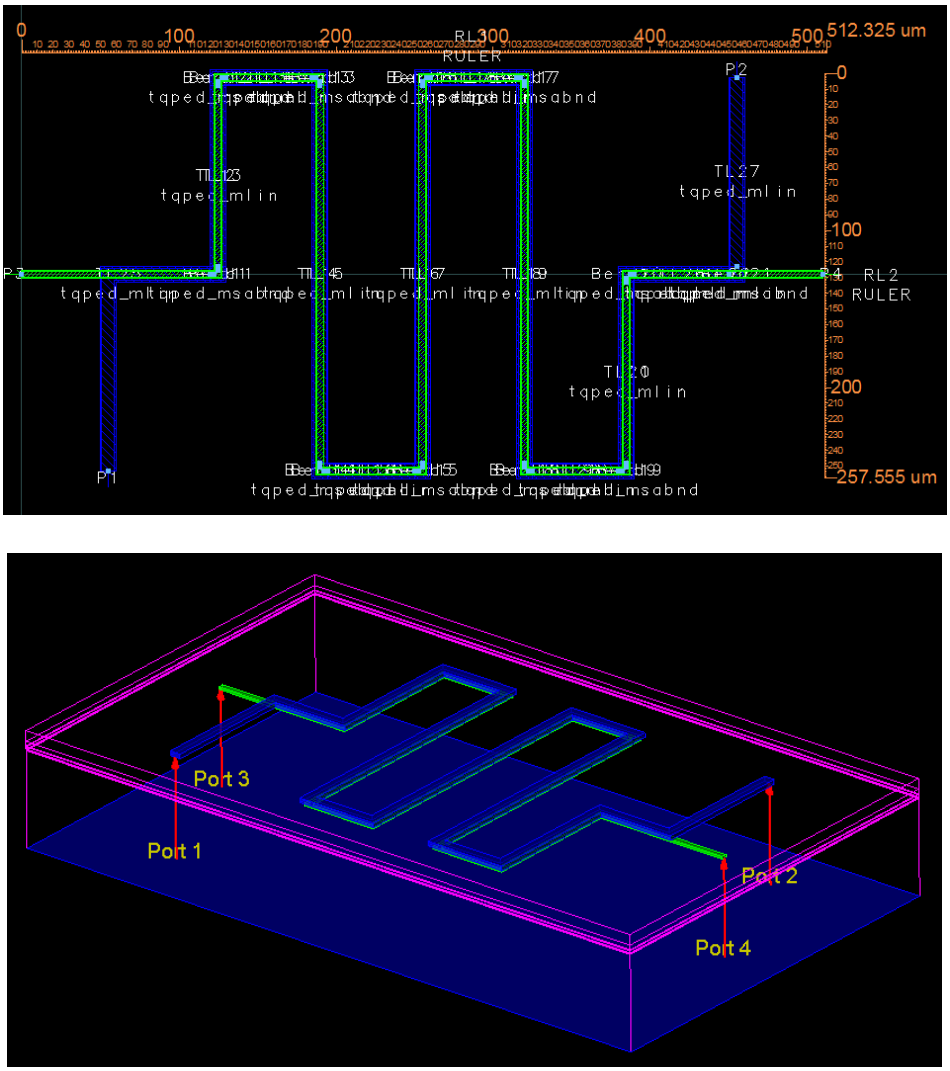



Figure 6-2. Broadside 90° coupler and 3D view

Simulation results of the broadside coupler are shown in Fig. 6-3 and show the broadband nature of the design with nearly uniform phase shift across the frequency band as well as good input match. Fig. 6-3 shown a system lineup of what the improved design would look like.

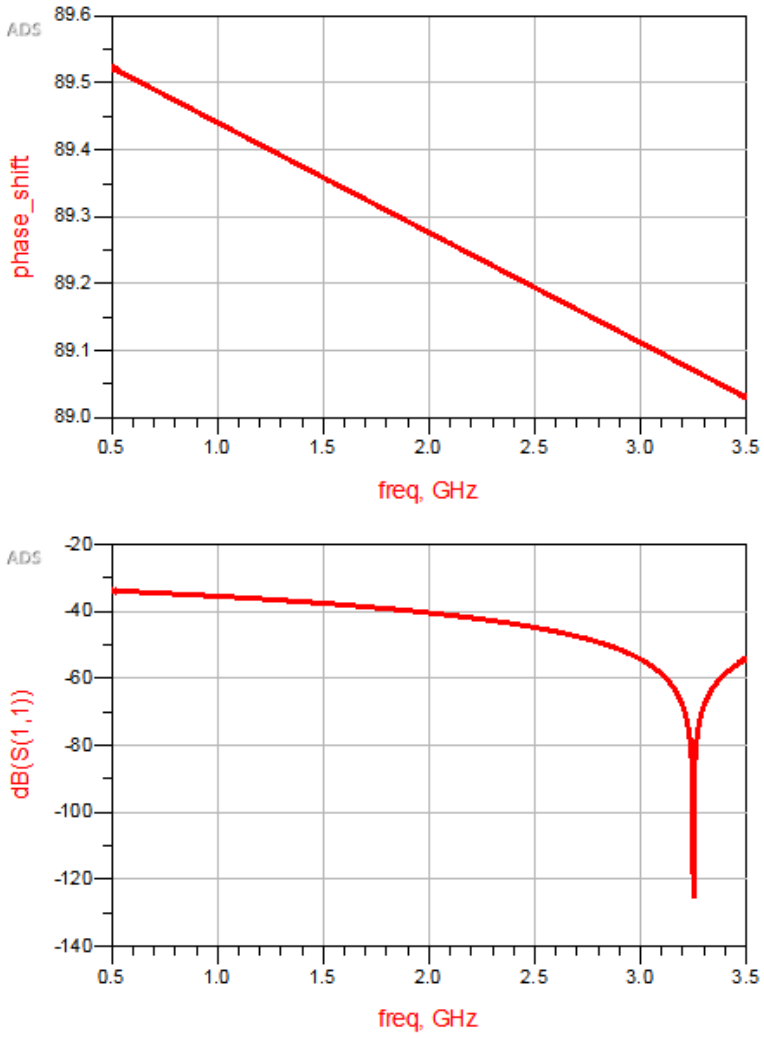



Figure 6-3. Simulated performance of broadside coupler

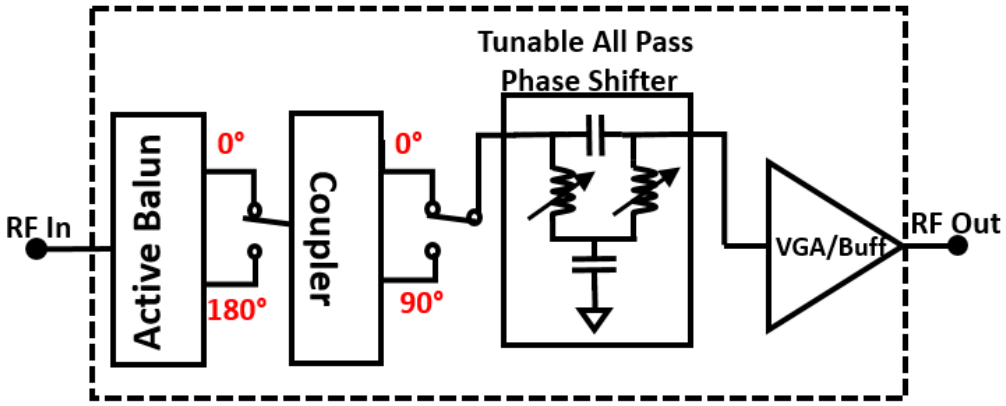



Figure 6-4. System level view with broadside coupler

## Appendix A:

## Design Tutorial

### A.1 Passive All-Pass Filter Design

Before designing active inductor for tunable all-pass phase shifter, the required tuning range for the inductor must be determined. This tuning range is based on design of passive all-pass phase shifters presented below. Design equations are provided below together with sample MathCAD worksheet (figure A-2). Refer to reference [A.1] for more detailed information on passive all-pass phase shifters.

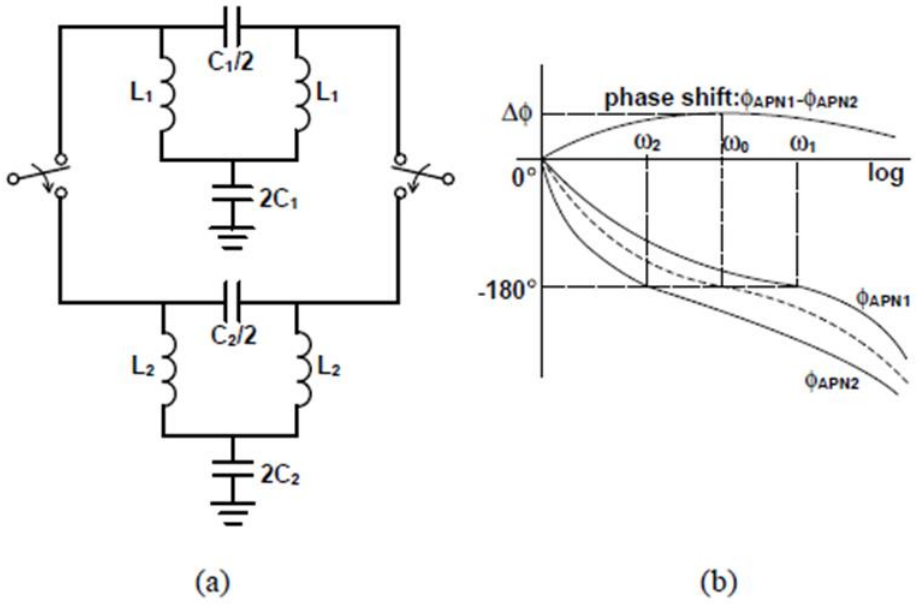



Figure A-1. Switched all-pass phase shifter

$$L_1 = \frac{pZ_0}{\omega_m}$$

$$L_2 = \frac{Z_0}{p\omega_m}$$

$$C_1 = \frac{p}{Z_0\omega_m}$$

$$C_2 = \frac{1}{pZ_0\omega_m}$$

$$p = \frac{1}{2}\tan\left(\frac{\emptyset_m}{4}\right) + \sqrt{1 + \frac{1}{4}tan^2\left(\frac{\emptyset_m}{4}\right)} \qquad \text{(A1)}$$

$f1 := 2.25 \cdot 10^9$

phase_shift := 180 Zo := 50

Phase shift is for each branch i.e total phase shift is 2X of above phase_shift value

ϕ needs to be in radians

$\phi := \frac{phase\_shift \cdot \pi}{180}$

$\omega 1 := 2 \cdot \pi \cdot f1$

$p := \frac{1}{2} \cdot \tan\left(\frac{\phi}{4}\right) + \sqrt{1 + \frac{1}{4} \cdot \tan\left(\frac{\phi}{4}\right)^2}$

$p = 1.618$

$L1 := \frac{p \cdot Zo}{\omega 1}$ $L2 := \frac{Zo}{p \cdot \omega 1}$

$C1 := \frac{p}{Zo \cdot \omega 1}$

$L1 = 5.723 \times 10^{-9}$ $\frac{C1}{2} = 1.145 \times 10^{-12}$ $C1 \cdot 2 = 4.578 \times 10^{-12}$

$L2 = 2.186 \times 10^{-9}$ $\frac{C2}{2} = 4.372 \times 10^{-13}$ $C2 \cdot 2 = 1.749 \times 10^{-12}$

Figure A-2. MathCAD worksheet

The value of L1 and L2 obtained for phase shift up to 180° will be the values used as the limits for tuning range of active inductor in the design steps that follow. The average of capacitor values for C1/2 and C2/2 will be used as the value for series capacitor in all-pass network (C1/2 and C2/2 in figure A-1). The same is done for shunt capacitor, taking average value of 2C1 and 2C2 as determined using MathCAD and using this value for the shunt capacitor (2C1 and 2C2 in figure 1).

To minimize tuning range of inductor in as effort to ease design requirements for active inductor design, the system impedance can be decreased to a value less than 50 Ω. This can be done if the phase shifter will be embedded with a chip and buffered at input and output.

**A.2 Active Inductor Design**

Once tuning range has been determined, design of tunable active inductor can be done. For a more technical discussion on differential gm-C active inductor design, use the references [A.2]-[A.4].

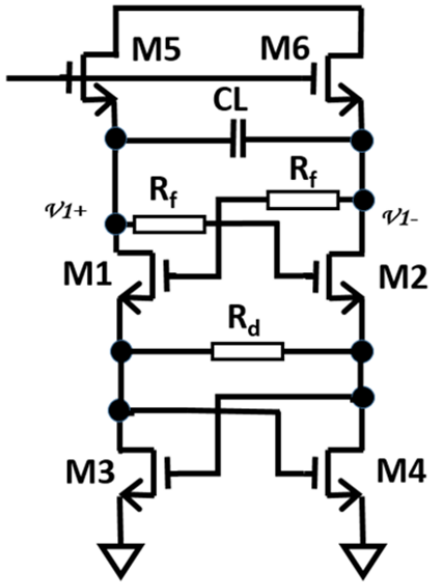



Figure A-3. Tunable active inductor

$$L = \frac{2Cgs}{gm_1 gm_2} \quad \text{(A2)}$$

$$f = \frac{1}{2\pi\sqrt{LC}} = \frac{1}{2\pi}\sqrt{\frac{gm1gm2}{2Cgs}} \quad \text{(A3)}$$

Figure A-3 is the schematic of the tunable active inductor described in chapter 4 and forms the bulk of the tunable all-pass phase shifter.

1. Having determined range of inductance value needed for tunable active inductor from passive all-pass filter design described previously, equation (A2) and equation (A3) can be used to find range of $gm$ values needed.
2. Use the smallest $gm$ value to get an approximate size of transistor M1 and M2 (W/L) knowing that:

$$gm = \sqrt{2K(W/L)I}$$

3. Use similar size for M3, M4, M5 and M6 as a starting point.
4. Add resistor $R_d$ and perform stability analysis to ensure unconditional stability. Vary bias current through M1 and M2. Vary $R_d$ value starting with small value of about 5 Ω, gradually increasing while observing changes in stability and quality factor.
5. Simulate inductance value by varying bias current passing through M1 and M2. This is done by varying voltage source at gate of M5 and M6. Perform over required frequency range. Add $R_f$ as shown in figure A-3. This will add another variable to the design. Start with a large value (about 500 Ω) for minimal feedback and tune using equations and plot in figure A-4 as a guide. This will affect not only inductance value but also frequency response. CL in figure A-3 is approximated as $2Cgs$ where $Cgs$ is parasitic gate to source

capacitance of M1 and M2 as shown in basic transistor model in figure A-4. Varying size of M1 and M2 combined with $gm$ tuning can be used to tune the design value to get the necessary range of inductance values.

6. Use figure A-5 and table A1 as a guide to fine tune design until required inductance range is achieved across frequency band of interest. Double arrows in table signify more rapid change in values compared to single arrow.

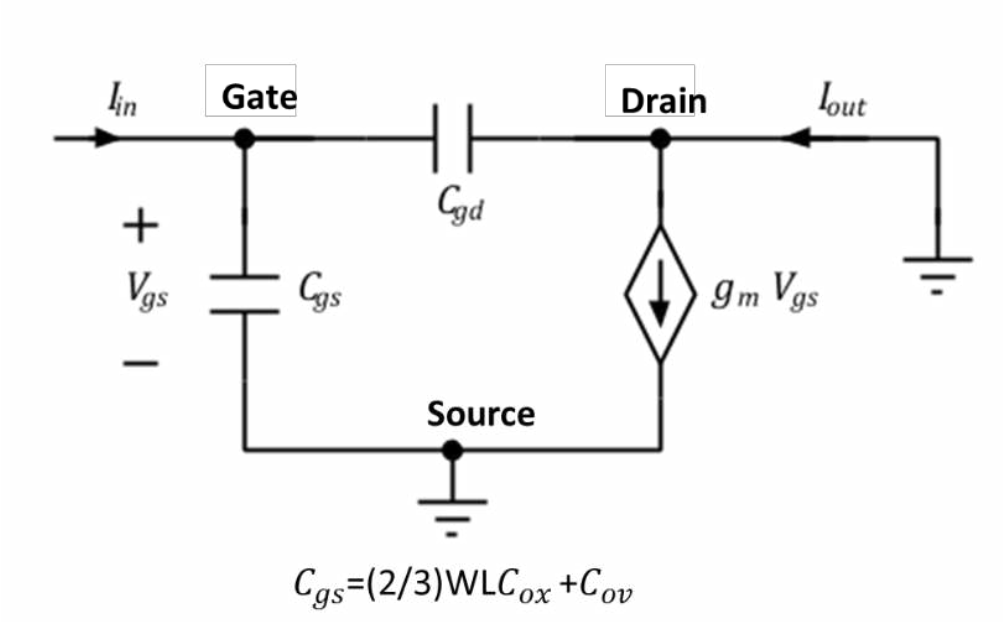
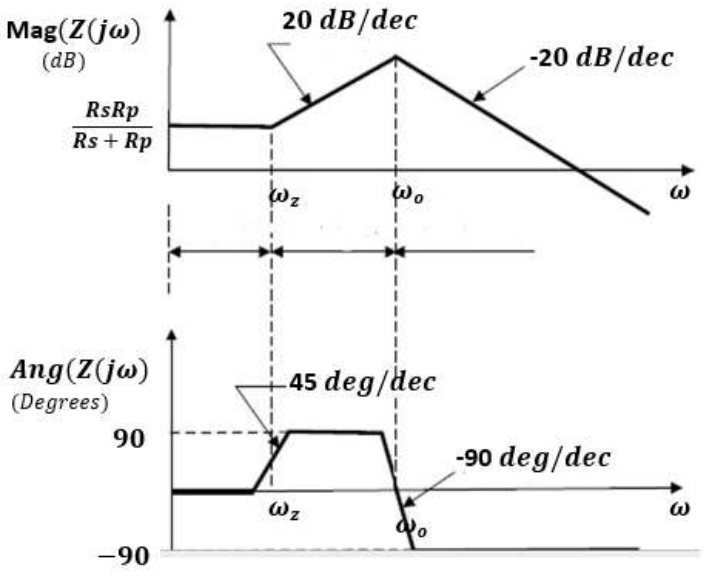



Figure A-4. Basic transistor model




$$\omega p \approx \sqrt{\frac{1}{C_L L}}, \qquad \omega z = \frac{R_s}{L}.$$

$$Q = \frac{\omega L}{R_s}.$$

$$R_s = \frac{\frac{1}{R_T} - \omega p^2 . Cgs_{11,12} . C_L . R_f}{gm_{11} . gm_{12}}$$

$$R_T = R_f \left\| R_d \right\| ro_{11,12} \left\| ro_{13,14} \right.$$

$$L = \frac{C_L}{\alpha (gm_{11} gm_{12})}$$

Figure A-5. Frequency response of active inductor

Table A1
Effects of Varying Transconductance and Feedback Resistance on Performance of Tunable Active Inductor

| $gm$ | $L$ | $R_s$ | $\omega p$ | $\omega z$ |
|---|---|---|---|---|
| ↑ | ↓↓ | ↓↓ | ↑ | ↓ |
| ↓ | ↑↑ | ↑↑ | ↓ | ↑ |
| $R_f$ | $L$ | $R_s$ | $\omega p$ | $\omega z$ |
| ↑ | ↓ | ↓ | ↑ | ↓↓ |
| ↓ | ↑ | ↑ | ↓ | ↑↑ |

## A.3 Active All-Pass Phase Shifter Design

Next step in the design is so replace inductors in passive all-pass phase shifter as shown in figure A-1 with active inductors. The two branches controlled by switches as shown in figure A-1 are replaced with a single tunable all-pass network with active inductors as shown in figure A-6.

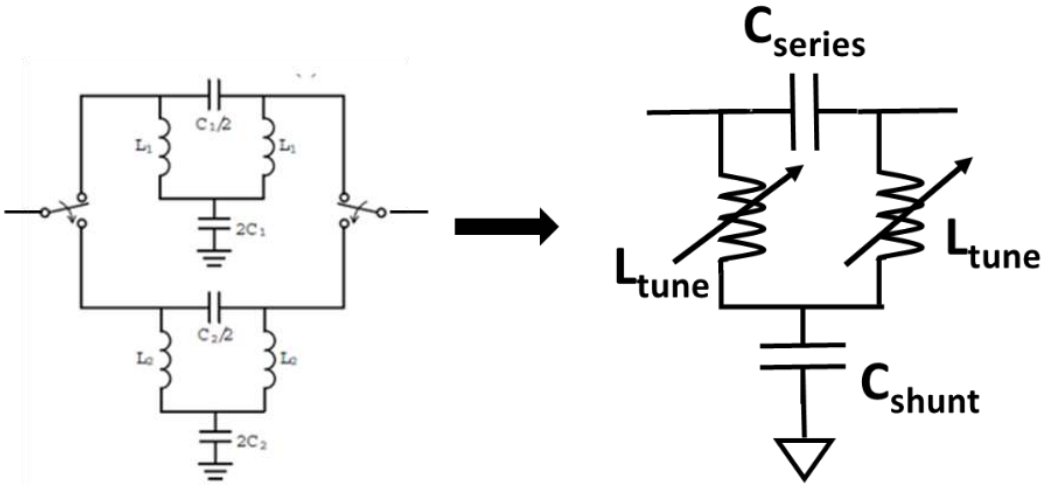



Figure A-6. Replacing all-pass switch network with tunable version

Optimization of design via simulation becomes necessary here, varying parameters used previously in active inductor design as well as values for $C_{series}$ and $C_{shunt}$ in figure A-6 where $C_{series}$ is average value of C1/2 and C2/2 and $C_{shunt}$ is average value of 2C1 and 2C2 as shown in figure A-1 and figure A-6. This is done at tuning voltage increments of about 30 mV which will correspond to incremental phase shifts up until about 180°. Stability analysis should be done at all bias conditions.

**A.4 Active Balun Design**

Detailed analysis of an active balun design can be found in reference [A.5] listed below. Figure A-7 shows the version implemented in this design. The difference between this version and the one in the reference is that it implements single transistor switches SW1 and SW2 at the output of each branch of the balun. These are fed to the common source buffers (M5 and M6) that combine the signals at the output so that instead of having two output signals, the combination of switches and balun provide only a single output that is either 0° or 180°. The switches can be sized appropriately through simulation to find the ideal tradeoff between isolation and insertion loss. The buffer output impedance is controlled by bias current IB as described by the equation

$$Zout = \frac{1}{gm} \quad where\ gm = \sqrt{2K(W/L)IB}$$

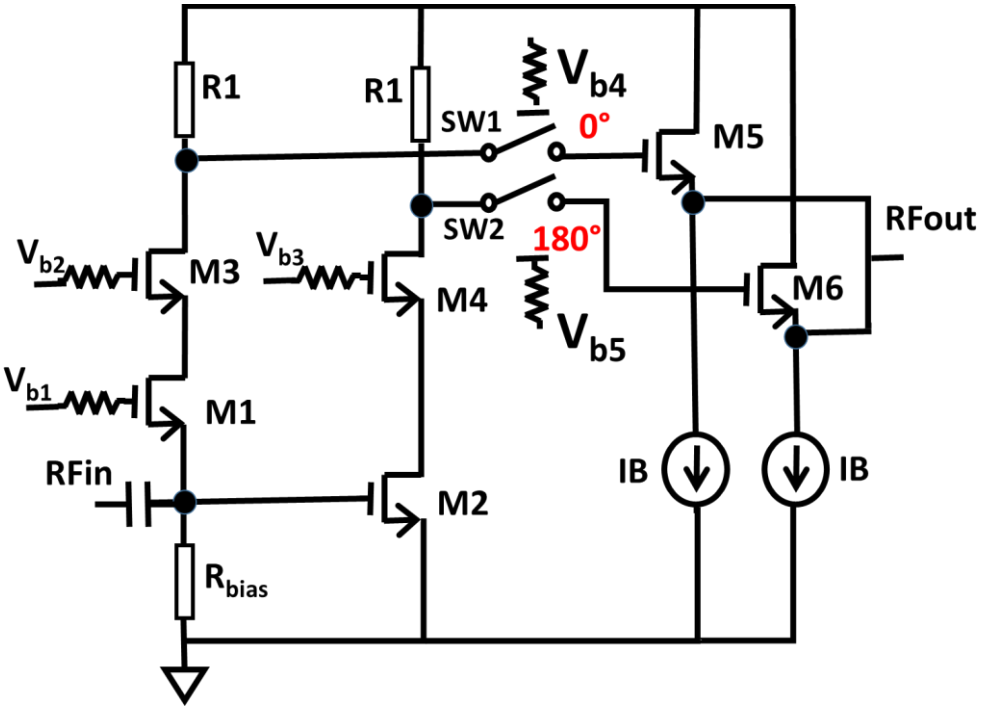



Figure A-7. Active balun

**A.5 VGA/Buffer Design**

The VGA/Buffer design is basically a common gate cascode transistor with an output buffer like that of active balun. The two stage design used in this work is shown in figure A-8. The current biasing of each stage is set by $R_{bias2}$ and $R_{Tune}$. Given that the voltage gain of a common gate stage is

$$A_v = gm_{M17,M20}\ x\ R_{2,3}$$

variation of $gm$ in the second stage for variable gain can be achieved by making $R_{Tune}$ a variable resistor. Varying this value changes the bias current which in turn changes $gm_{M20}$. Refer to chapter 5 of dissertation for more details on the design.

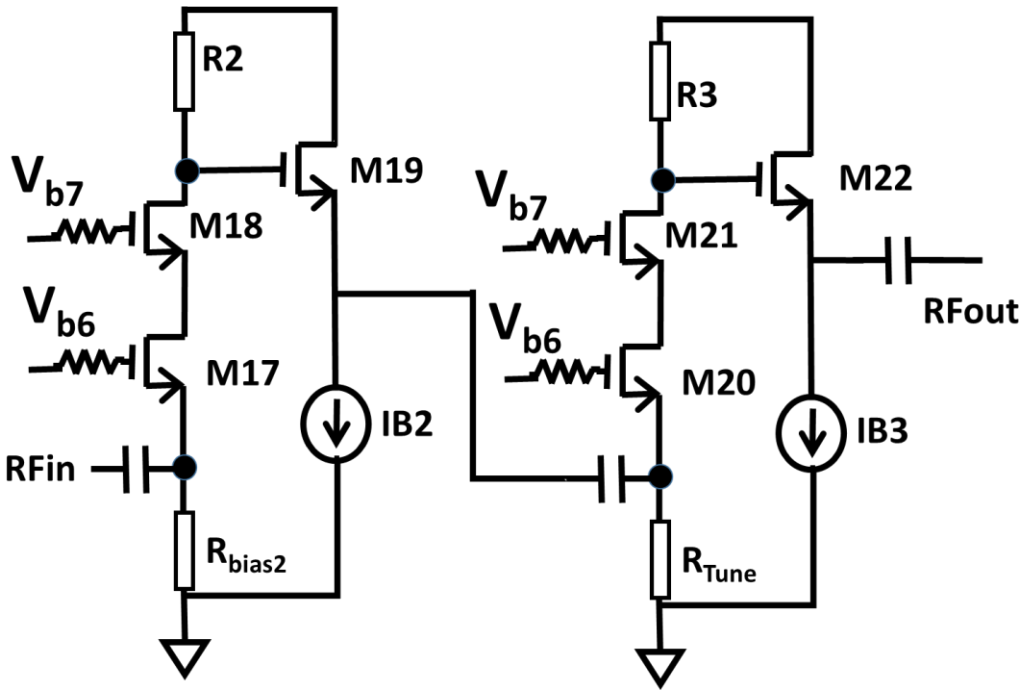



Figure A-8. VGA/Buffer schematic

## A.6 References

[A.1] D. Adler and R. Popovich, "Broadband Switched-Bit Phase Shifter Using All-Pass Networks," 1991 IEEE MTT-S Int. Microwave Symp. Dig., vol. 1, pp. 265- 268, July 1991.

[A.2] Chun-Lee Ler; bin A'ain, A.K.; Kordesch, A.V. "Compact, High-Q, and Low-Current Dissipation CMOS Differential Active Inductor" Microwave and Wireless Components Lett. , Oct. 2008

[A.3] F. Belmas, F. Hameau, and J-M. Fournier , "A New Method for Performance Control of a Differential Active Inductor for Low Power 2.4 GHz applications," IEEE International Conference on IC Design and Technology, June 2-4 2010.

[A.4] Fei Yuan, "CMOA Active Inductors," in CMOS Active Inductors and Transformers, Principle, Implementation, and Applications, 1st ed., New York: Springer Science, 2008, pp. 21–98.

[A.5] S. C. Blaakmeer, E. A. M. Klumperink, D. M. W. Leenaerts, and B. Nauta, "Wideband balun-LNA with simultaneous output balancing, noise-canceling and distortion-canceling," IEEE J. Solid-State Circuits, vol. 43, pp. 1341–1350, Jun. 2008.

## About the Author

David M. Zaiden (S'01-M'05) was born in Belize, Central America. He received the B.S. in electrical engineering from the University of Houston, Houston, TX, USA in 2000. He worked at Motorola in Austin, TX, USA from 2000-2002. He received the M.S. in electrical engineering from the University of South Florida, Tampa, FL, USA, in 2005 with a focus on RF and Microwave circuit design. From 2005-2012 he was employed as an RFIC design engineer with Insyte/ITT/Exelis in Tampa, FL, USA. Since 2013 he has been pursuing his Ph.D. degree in electrical engineering as a Draper Labs Fellow at the University of South Florida, Tampa, FL, USA, with a focus on MMIC phase shifter design.

He currently works for Harris Corporation in Palm Bay, FL, USA as an RF engineer involved in the design of MMIC's for phased array systems. He lives in Melbourne, FL with his wife Jesusita and his four boys, Antonio, Adiel, Athan and Alzan.