Compact Millimeter-Wave Bandpass Filters Using Quasi-Lumped Elements in 0.13-μm (Bi)-CMOS Technology for 5G Wireless Systems

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***Abstract*— A design methodology for a compact millimeter-wave on-chip bandpass filter (BPF) is presented in this paper. Unlike the previously published works in the literature, the presented method is based on quasi-lumped elements, which consists of a resonator with enhanced self-coupling and metal–insulator–metal capacitors. Thus, this approach provides inherently compact designs comparing with the conventional distributed elements-based ones. To fully understand the insight of the approach, simplified LC-equivalent circuit models are developed. To further demonstrate the feasibility of using this approach in practice, the resonator and two compact BPFs are designed using the presented models. All three designs are fabricated in a standard 0.13-μm (Bi)-CMOS technology. The measured results show that the resonator can generate a notch at 47 GHz with the attenuation better than 28 dB due to the enhanced self-coupling. The chip size, excluding the pads, is only 0.096 × 0.294 mm^2. In addition, using the resonator for BPF designs, the first BPF has one transmission zero at 58 GHz with a peak attenuation of 23 dB. The center frequency of this filter is 27 GHz with an insertion loss of 2.5 dB, while the return loss is better than 10 dB from 26 to 31 GHz. The second BPF has two transmission zeros, and a minimum insertion loss of 3.5 dB is found at 29 GHz, while the return loss is better than 10 dB from 26 GHz to 34 GHz. Also, more than 20-dB stopband attenuation is achieved from dc to 20.5 GHz and from 48 to 67 GHz. The chip sizes of these two BPFs, excluding the pads, are only 0.076 × 0.296 mm^2 and 0.096 × 0.296 mm^2, respectively.**

***Index Terms*— Bandpass filter (BPF), Bi-CMOS, microwave, millimeter wave (mm wave), miniaturization, on-chip resonator, RFIC, silicon–germanium (SiGe).**

I. Introduction

THE rise of 5G begins an exciting new era in the world of mobile connectivity. The so-called millimeter-wave (mm-wave) technology is one of the key factors, which enables not only wireless transmission of gigabits per second that are 20 times faster than the current 4G network, but also low-latency communication that is the fundamental of many emerging applications, such as autonomous vehicles. Among different potential applications, the 28-/39-GHz cellular network [1], 60-GHz Wi-Gig [2], and 77-GHz automotive radar [3] are likely to be widely deployed to support the commercialization of the upcoming 5G in the very near future.

One of the major differences between the conventional transceiver architecture that operates for sub-6 GHz and the emerging mm-wave transceiver architecture is that either subharmonic mixing or frequency multiplication technique is usually used for local oscillator (LO) generation. Both techniques utilize nonlinearity of active devices to produce an mm-wave signal source for the purpose of up/down frequency conversion. Because of nonlinearity is used, the unwanted harmonics must be suppressed sufficiently; otherwise, the overall performance of the mm-wave system could be deteriorated severely. To generate the required LO source operating at mm-wave region, frequency doubler and tripler are the most popular building blocks [4], [5]. Although odd-order harmonics can be inherently suppressed in theory for a "push–push" frequency doubler, a bandpass filter (BPF) is still required for rejecting the unwanted fourth-order harmonics as well as further suppressing the fundamental and third-order harmonics. If a frequency tripler is used in an LO chain, a BPF is also necessary to suppress the fundamental, second-order, and fourth-order harmonics. In addition, the concept of passive-inspired designs has drawn extensive attention recently. It has been widely used for the design of high-performance building blocks, such as amplifiers, signal sources, and switches [4]–[12]. Filter designs are no longer simply treated for interference suppression, but also used for impedance transformation and co-design with other active components.

As far as on-chip filter designs are concerned, several design tradeoffs need to be considered to satisfy different design specifications, such as miniaturized physical size and reduced insertion loss. Several prior works can be found in the literature on this regard, which includes bandstop [13], low-pass [14], [15], and BPFs [16]–[28] design in standard silicon-based technologies. By miniaturizing physical dimensions of

Manuscript received October 14, 2018; revised December 30, 2018; accepted January 4, 2019. This work was supported by the Australian Research Council under Grant DE160101032. *(Corresponding author: Xi Zhu.)*

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Digital Object Identifier 10.1109/TMTT.2019.2895581

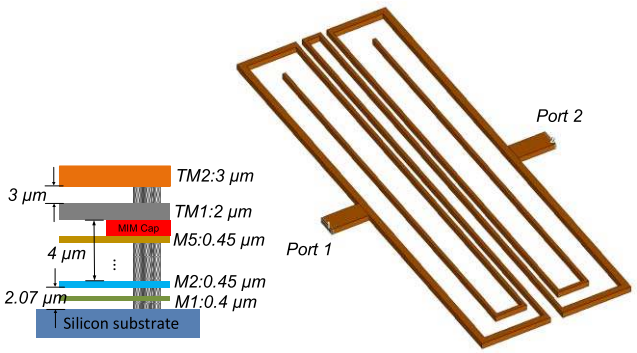


Fig. 1. 3-D view of the proposed resonator and the metal stack-up used for implementation. (Note that ground shielding is removed for better visibility.)

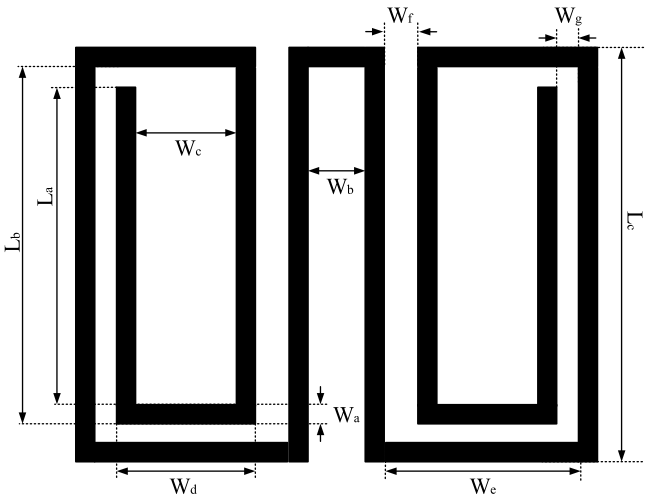


Fig. 2. 2-D view of the proposed resonator with enhanced self-coupling.

passive components, not only the overall die size can be reduced, but it is also useful for reducing conductor loss of the metal strips. As a result, the overall insertion loss can be optimized efficiently. For these reasons, several novel approaches for the design of miniaturized devices have been presented in the literature. Unlike using the conventional distributed components approach for filter designs [16]–[20], the quasi-lumped components approach has gained attention recently [21]–[28]. The key idea of this emerging approach is to enhance the so-called self-coupling by fully utilizing provided metal stack-up. One of the possible solutions is to use broadside-coupled structures [22]–[25]. However, this idea has a limitation, which is that the vertical gap between each metal layer cannot be changed in the design as they are predefined physical parameters. As a result, the design flexibility is dramatically restricted. Because of this limitation, it is desirable to design a planar structure that can be implemented using single metal layer only to perform the required self-coupling mechanism.

In this paper, a design methodology based on quasi-lumped elements is proposed. By taking advantage of the inherent self-coupling inside a spiral inductor, a resonator is designed to be capable to generate a strong notch at a specific frequency. Using this feature along with metal–insulator–metal (MIM) capacitors, two compact on-chip BPFs are developed and implemented in a standard (Bi)-CMOS 0.13-μm technology. A good agreement between the simulations and measurements has been achieved for all three designs. The rest of this paper is organized in the following way. In Section II, the principle of the designed resonator with enhanced self-coupling is presented. Using this resonator as a baseline, two BPF design examples are given in Section III and IV, respectively. These are followed by the measured results in Section V, and conclusions are drawn in Section VI.

II. Design and Implementation of the Resonator With Enhanced Self-Coupling

A. Overview of the Resonator

The 3-D view of the proposed resonator and the metal stack-up used for its implementation is shown in Fig. 1. The metal stack-up is from a standard 0.13-μm (Bi)-CMOS technology that has seven metal layers with aluminum as the thick top two metal layers. The additional MIM layer is placed between TM1 and M5. In addition, the height of the silicon substrate is 200 μm. The dielectric constant of SiO_2 is 4.1, and the loss tangent is 0.01.

The 2-D view of the resonator is given in Fig. 2. Unlike previously published works, this resonator is based on a planar structure which only requires a single metal layer for implementation. As can be seen, the resonator has a symmetrical structure and consists of a symmetrically folded strip-line. The physical dimensions of the resonator can be varied, depending on which metal layer is selected for its implementation which will be further discussed later.

B. Simplified LC-Equivalent Circuit Model of the Resonator

To understand the principle of the EM structure presented in Fig. 2, a simplified *LC*-equivalent circuit model is given in Fig. 3. For simplicity, a half-circuit model is first presented in Fig. 3(a). As illustrated, the folded meander line can be split into two parts, which are colored in black and red, respectively. In addition, the capacitors are used to model the capacitive coupling between two parts through edge coupling. To construct a simplified full-circuit model, the half-circuit model can be further simplified to a combination of two inductors L_1 and L_2 representing the black and red inductors, and one capacitor C_1 representing the mutual coupling. In Fig. 3(b), the simplified full-circuit model is presented that consists of two half-circuit models presented in Fig. 3(a).

The input admittance of the resonator can be expressed as

$$Y_{\text{in}} = -j\frac{1}{\omega L_2} + \frac{j\omega C_1}{1-\omega^2 L_1 C_1}. \tag{1}$$

To determine the resonant frequency of the resonator, one can solve the equation $Y_{\text{in}} = 0$. In this case, the resonant frequency is found to be located at

$$f_o = \frac{1}{2\pi} \times \sqrt{\frac{1}{(L_1+L_2)\,C_1}}. \tag{2}$$

The 3-D mapping of the relation between f_0, L_1, and C_1 is provided in Fig. 4. It is straightforward to find out that

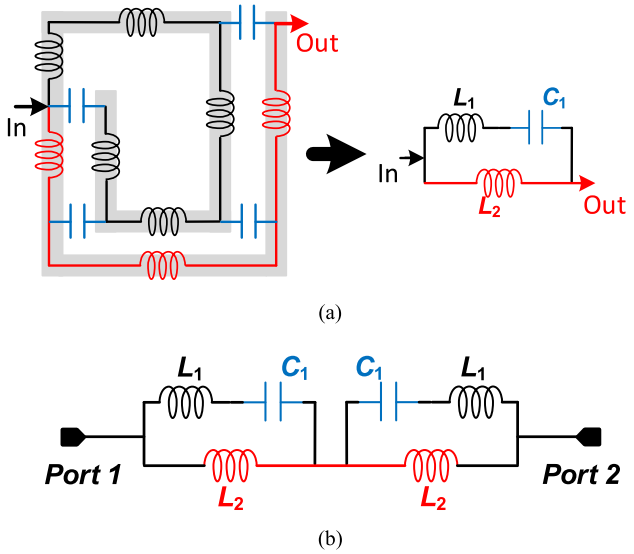


Fig. 3. Simplified *LC*-equivalent circuits. (a) Half circuit. (b) Full circuit.

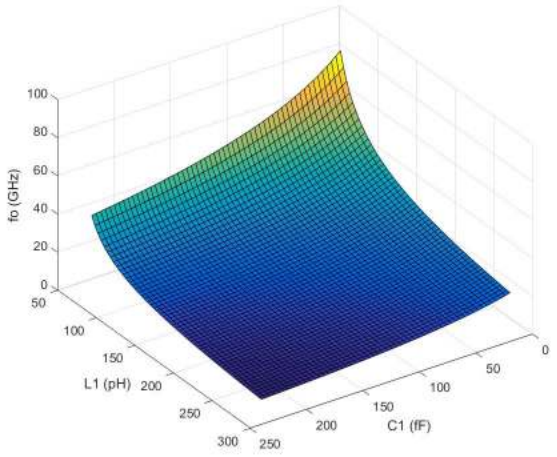


Fig. 4. Simulated resonant frequency using the circuit model presented in Fig. 3.

the resonance f_0 is inversely proportional to L_1 and C_1. By changing the values of L_1 and C_1, the resonance can be effectively controlled. Here, it is assumed that L_1 is equal to L_2 for simplicity. If either of them is fixed, a similar variation pattern can be found as well.

C. Implementation of the Resonator

In order to verify the principle of the resonator as well as the simulated results using the ideal lumped components, two design examples are given in this section. The proposed resonator is implemented first using the topmost metal layer, namely, TM2. The detailed physical dimensions of the resonator for this case are summarized in Table I. As previously analyzed, three physical parameters, L_c, W_g, and W_f, can be used to adjust the frequency response of the resonator. Thus, a parametric study is presented in this section to investigate their impact on the resonator design. By fixing the values of W_g and W_f, the value of L_c is swept from 172 to 272 μm with a step of 50 μm. As illustrated in Fig. 5(a), the resonance can be shifted from 46 to 72 GHz. It indicates that the generated transmission notch is relatively reliable and can be controlled efficiently across a broad bandwidth. Thus, by tuning the length of the resonator, a coarse tuning can be performed. On the other hand, as illustrated in Fig. 5(b) and (c), by fixing the value of W_g and L_c, the optimized value for W_f can be determined. Likewise, if the values of L_c and W_f are fixed, the value of W_g can be used for fine-tuning. Consequently, the resonator can be implemented in a very flexible way.

TABLE I
PHYSICAL DIMENSIONS OF THE RESONATOR IMPLEMENTED IN TM2 LAYER

W_a	W_b	W_c	W_d	W_e
2 μm	8 μm	16 μm	20 μm	26 μm
W_f	W_g	L_a	L_b	L_c
4 μm	2 μm	258 μm	262 μm	268 μm

III. DESIGN AND IMPLEMENTATION OF THE FIRST BPF

To prove that the presented resonator is useful in practice, in this Section, an on-chip BPF design example is given, which uses a combination of the resonator with MIM capacitors.

A. Simplified LC-Equivalent Circuit Model of the First BPF

Using the previously presented resonator as a baseline, a BPF can be designed by introducing an L-type capacitive feeding network to the resonator [28], [29]. To understand the impact on the center frequency as well as the bandwidth of the filter due to using different feeding capacitances, a simplified *LC*-equivalent circuit model is given first as shown in Fig. 6.

It is observed that the equivalent circuit model consists of two parts: one is the resonator with enhanced self-coupling, which has been shown in Fig. 3; another part is the L-type feeding network that has a series capacitance C_2 and a shunt capacitance C_3. Both capacitors could affect the resonance and the bandwidth of the BPF simultaneously. Therefore, it is critical to choose appropriate values for them based on predetermined specifications.

To design a BPF, two aspects need to be focused, which are resonance and bandwidth. For the resonance, the position of the resonance pole can be found by solving the following equation:

$$Y_{\text{in}} = 0$$

where

$$Y_{\text{in}}(\omega) = \frac{j\omega C_2 + j\omega C_3 - j\frac{1}{\omega L_2} + \frac{j\omega C_1}{1-\omega^2 L_1 C_1}}{j\omega C_2 \cdot \left(j\omega C_3 - j\frac{1}{\omega L_2} + \frac{j\omega C_1}{1-\omega^2 L_1 C_1}\right)}. \quad (3)$$

Equivalently, the resonance can be solved by

$$j\omega C_2 + j\omega C_3 - j\frac{1}{\omega L_2} + \frac{j\omega C_1}{1-\omega^2 L_1 C_1} = 0. \quad (4)$$

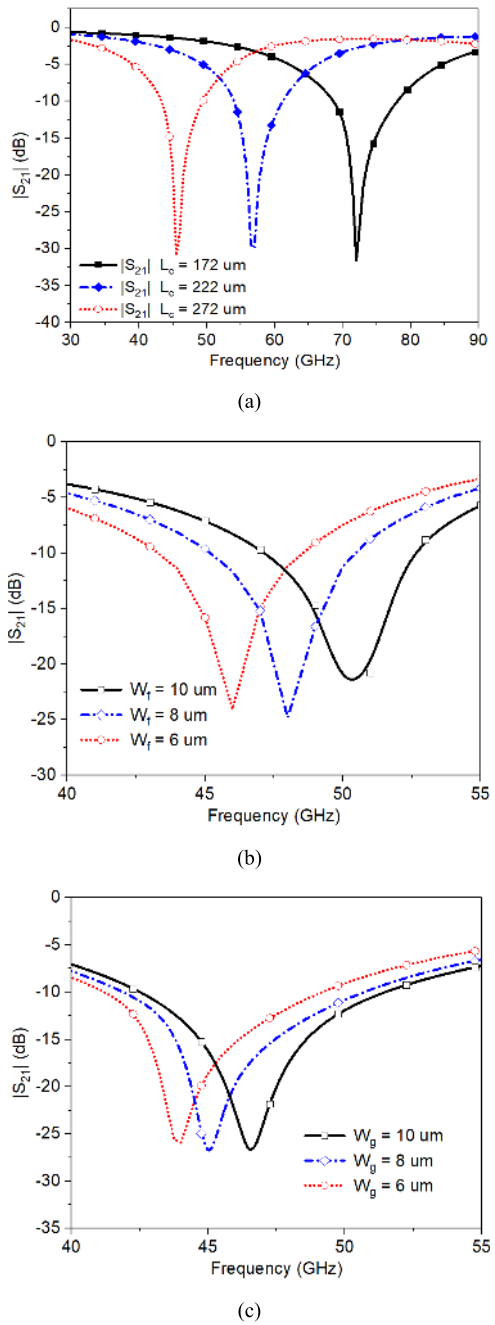


Fig. 5. EM simulated $|S_{21}|$ of the inductor implemented in TM2. (a) W_f and W_g are fixed as 2 and 4 μm, respectively. (b) W_g and L_c are fixed as 4 and 268 μm, respectively. (c) W_f and L_c are fixed as 2 and 268 μm, respectively.

The resonances are found to be located at

$$f_1 = \frac{1}{2\pi} \times \sqrt{\frac{s - \sqrt{s^2 - 4t}}{2t}} \tag{5}$$

$$f_1^{'} = \frac{1}{2\pi} \times \sqrt{\frac{s + \sqrt{s^2 - 4t}}{2t}} \tag{6}$$

where

$$s = C_1 L_1 + (C_1 + C_2 + C_3) L_2 \tag{7}$$

$$t = L_1 L_2 C_1 (C_2 + C_3). \tag{8}$$

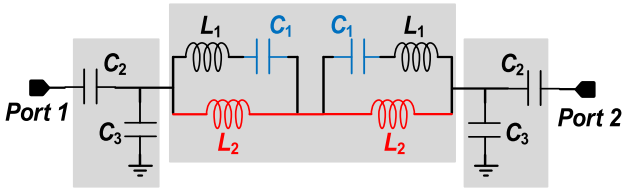


Fig. 6. Simplified LC-equivalent circuit model of the first BPF.

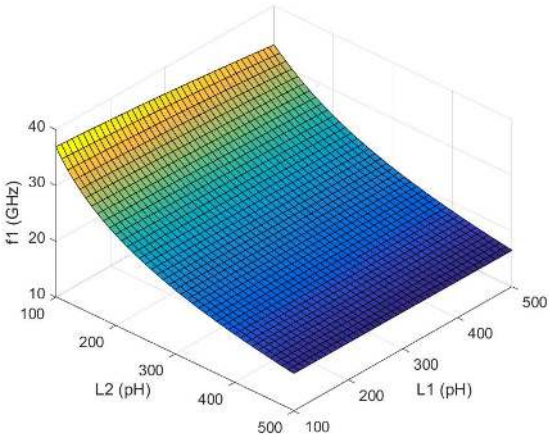


Fig. 7. 3-D mapping of the resonant frequency f_1 against L_1 and L_2.

As shown, the two resonances f_1 and $f_1^{'}$ are generated. For the BPF design, f_1 is used to form the passband while $f_1^{'}$ is a spurious harmonic located at the upper-stopband, which should be suppressed. Though the resonances are related to $C_1, C_2, C_3, L_1,$ and L_2, the values of $C_1, L_1,$ and L_2 are determined first by (2), since the resonator can produce a transmission zero at f_0. The resonance of the BPF f_1 can be controlled by $L_1, L_2,$ and C_1. The relation among f_1, L_1, L_2can be described in a 3-D mapping figure, which is shown in Fig. 7. As can be seen that L_2 affects the position of f_1 while L_1 almost has no impact on f_1. Fig. 8 shows the 3-D mapping relation among f_1, L_2 and C_1. Considering (2), the position of the transmission zero and the value of C_1 can be decided first, and then the value of $(L_1 + L_2)$ is decided. Then, according to Fig. 8, one can determine the values of L_1 and L_2 according to the requirement of f_1.

The external quality factor and bandwidth of the filter are mainly controlled by C_2 and C_3. For the coupling condition, the external quality factor of the BPF is determined by the susceptance slope parameter of the BPF, which is calculated by

$$Q_{\text{ex}} = \frac{2b}{Y_o} \tag{9}$$

where

$$b = \frac{\omega_o}{2} \times \frac{\partial \text{Im}[Y_{in}]}{\partial \omega}\bigg|_{\omega=\omega_o}. \tag{10}$$

Here, b is the susceptance slope parameter of the resonator and Y_{in} is the input admittance of the BPF considering the effect of C_2 and C_3. Replacing b in (9) and using (10), the Q_{ex} can

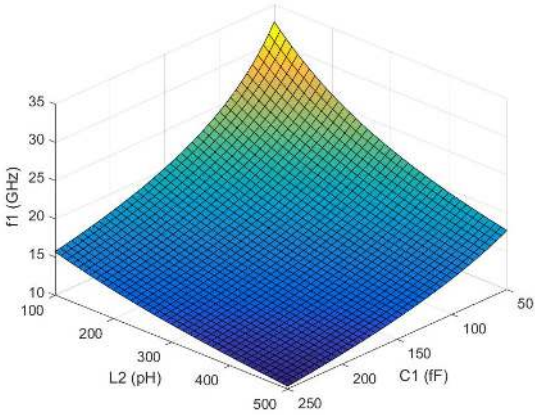


Fig. 8. 3-D mapping of the resonant frequency f_1 against C_1 and L_2.

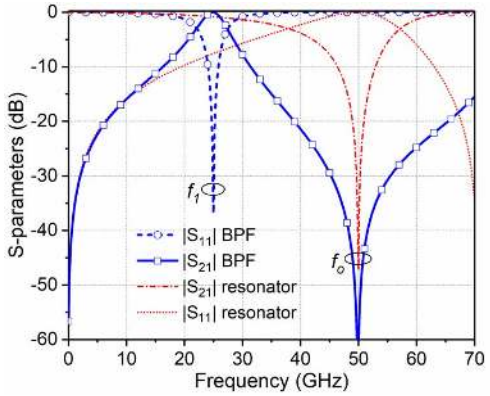


Fig. 9. Calculated S-parameters of the resonator and the first BPF design example using this resonator.

be expressed as

$$Q_{\text{ex}} = \frac{\omega_o}{2Y_o} \times \left\{ C_3 + \frac{1}{\omega_o^2 L_2} + \frac{C_1\left(1+\omega_o^2 L_1 C_1\right)}{\left(1-\omega_o^2 L_1 C_1\right)^2} + \frac{\frac{2\omega_o C_2^2}{Y_o^2}}{\left[1+\left(\frac{\omega_o C_2}{Y_o}\right)^2\right]^2} \right\}. \tag{11}$$

Meanwhile, the external quality factor of the BPF is closely related to the fractional bandwidth (FBW), which can be expressed as

$$Q_{\text{ex}} = \frac{\sqrt{g_0 g_1}}{\text{FBW}} \tag{12}$$

where g_0 and g_1 refer to the basic values of the traditional lowpass filter. As can be seen from (11) and (12), the FBW and Q_{ex} are related to $C_1, C_2, C_3, L_1,$ and L_2 simultaneously. Since $C_1, L_1,$ and L_2 are subjected to the selection of the transmission zero f_0 and the resonant pole f_1, these three variables are predetermined and thus cannot be changed for the BPF design. In this case, only C_2 and C_3 are used to control the external coupling as well as the bandwidth of the filter. The cascaded capacitor C_2 and shunted capacitor C_3 at the input–output port can be calculated using the following equation:

$$C_2 = \frac{J_{01}}{\omega_o \sqrt{1-(J_{01}/Y_o)^2}} \tag{13}$$

$$C_3 = \frac{C_2}{(\omega_o C_2/Y_o)^2} \tag{14}$$

where

$$J_{01} = \sqrt{\frac{Y_o b \times \text{FBW}}{g_0 g_1}}. \tag{15}$$

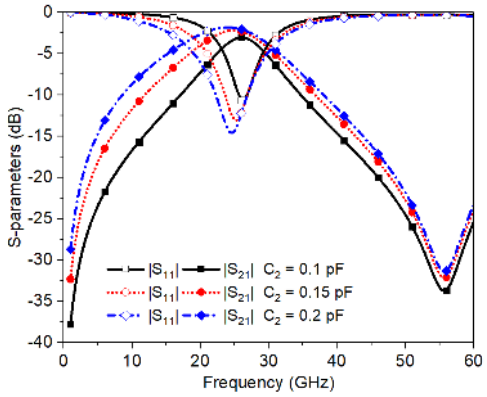
When $C_1, L_1,$ and L_2 are chosen, the susceptance slope parameter b is fixed as well. Then, the values of C_2 and C_3 can be decided based on (13) and (14) with given design targets for g_0, g_1, FBW, and Q_{ex}. The calculated S-parameters of the resonator and the BPF are given in Fig. 9, while the associated values are selected as $C_1 = 40$ fF, $C_2 = 120$ fF, $C_3 = 200$ fF, and $L_1 = L_2 = 125$ pH. It is seen that the transmission zero f_0 and that of the BPF are located at the same position. This is because the transmission zero is created by the resonator and its position is purely determined by (2). This indicates that the transmission zero can be adopted in the filter design to enhance the upper-stopband suppression of the BPF. Moreover, the resonant pole f_1 is located at a lower frequency than f_0, which forms the passband of the filter. The bandwidth and the external quality factor can be controlled by tuning the values of C_2 and C_3 which will not affect the transmission zero. In this case, a BPF can be built based on the previously presented resonator with an appropriate external coupling factor provided by the capacitors.

TABLE II
PHYSICAL DIMENSIONS OF THE FIRST BPF

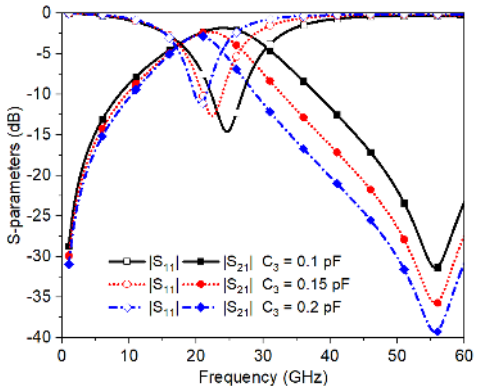
W_a	W_b	W_c	W_d	W_e
2 μm	8 μm	6 μm	10 μm	16 μm
W_f	W_g	L_a	L_b	L_c
4 μm	2 μm	258 μm	264 μm	272 μm

B. Implementation of the First BPF

To prove that the provided analysis is correct, the first BPF is designed and implemented. The physical dimensions of the filter are summarized in Table II. As previously discussed, once the physical dimensions of the resonator are fixed, the selection of feeding network becomes a vital task for BPF design. To verify the impact on the frequency responses due to using a different combination of C_2 and C_3, the EM simulator is used in conjunction with swept capacitance values. The simulated results are given in Fig. 10. As shown in Fig. 10(a), the capacitance C_2 is fixed, and the capacitance C_3 is swept from 0.1 to 0.2 pF with a step of 50 fF. A similar procedure is repeated with C_3 being fixed and C_2 being swept, while the results are given in Fig. 10(b). As illustrated, both feeding capacitances have a similar impact on the frequency response of the BPF, including the center frequency, insertion loss, return loss, and harmonic suppression. In practice, the selection of the shunt capacitance is more critical because it can be



(a)



(b)

Fig. 10. Simulated S-parameters of the first BPF with different feeding capacitances. (a) C_3 is fixed as 0.1 pF. (b) C_2 is fixed as 0.2 pF.

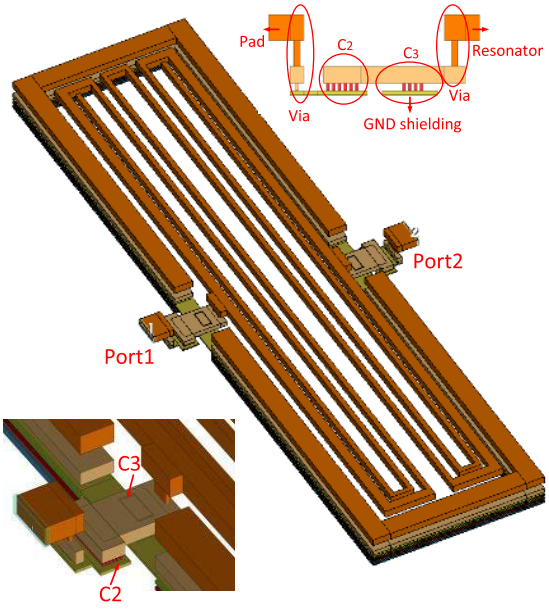


Fig. 11. 3-D view of the first BPF with highlighted MIM capacitors.

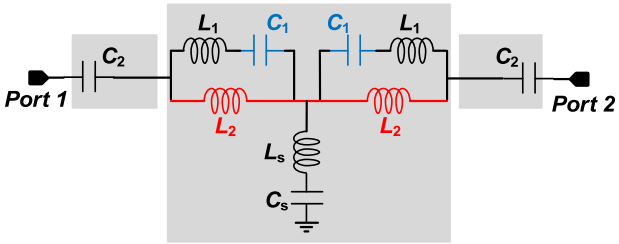


Fig. 12. Simplified *LC*-equivalent circuit model of the second BPF.

significantly affected by the grounded parasitic capacitance. Thus, a sufficient margin needs to be taken into consideration. In this design, $C_2 = 0.16$ pF and $C_3 = 50$ fF are used. In order to ensure not only a miniaturized design but also high accuracy in terms of the frequency responses, both capacitors used for the *L*-type feeding network are implemented using MIM structures. The 3-D view of the designed BPF and the implementation of a MIM capacitor is given in Fig. 11. As shown, the TM1 and M5 are used to implement the top and bottom plates of the MIM capacitor, respectively.

IV. Design and Implementation of the Second BPF

Although it has proved that the presented design methodology can be used for BPF design in Section III, the realized filter is a first-order filter and only has one transmission zero at high frequency. To improve the selectivity of the passband, it is desired to design higher order filters which have another transmission zero at a lower frequency to improved the band selectivity. To that end, the second design example is presented in this section with an additional transmission zero at the low frequency. This transmission zero can be introduced by loading a series-*LC* network in the middle point of the folded stripline. The schematic is given in Fig. 12. The resonant condition of the transmission zero ω_2 can be written as

$$j\omega_2 C_s - j\frac{1}{\omega_2 L_s} = 0. \tag{16}$$

Therefore, the position of the TZ f_2 can be solved as

$$f_2 = \frac{1}{2\pi} \times \sqrt{\frac{1}{L_s C_s}}. \tag{17}$$

The relations between f_2 and the series-*LC* network L_s and C_s are presented in Fig. 13. It is possible to design the transmission zero at any desired position, and the required value of L_s and C_s for the corresponding f_2 can be found from Fig. 13.

It is observed both from (14) and Fig. 13 that f_2 will move to lower frequencies when L_s or C_s decreases. For f_2, the value of L_s is relatively small and limited within a small range, which is because L_s refers to the parasitic inductance. The capacitance C_s is obtained using on-chip MIM capacitor. Since L_s is almost unchanged, it is possible to select appropriate value of MIM capacitor C_s to determine the position of f_2. It is noted that the f_2 is different from the expression of f_o, where the capacitance C_1 is relatively small and L_1 is dominant. The comparisons of the calculated results between the BPFs with and without the low-frequency transmission zero is given in Fig. 14. Comparing with the results presented in Fig. 9, the transmission zero f_0 at higher frequency is located at exactly the same position, which is due to the reason that the resonant conditions of f_0 are the same for

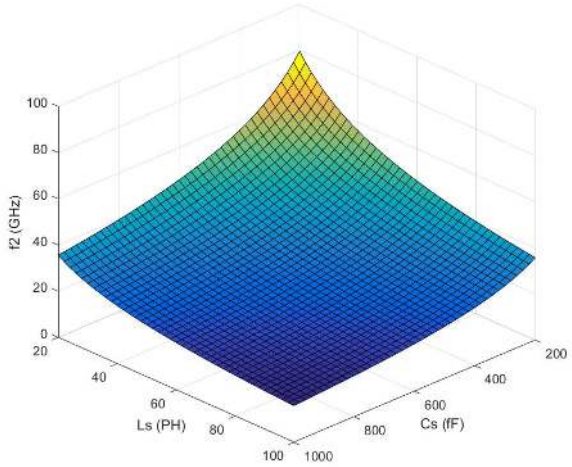


Fig. 13. 3-D mapping of the resonant frequency f_2 against C_s and L_s.

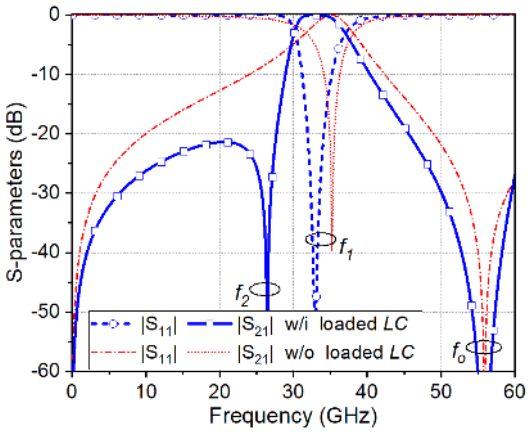


Fig. 14. Comparison of the calculated S-parameters of two designed BPFs with and without low-frequency transmission zero.

TABLE III
PHYSICAL DIMENSIONS OF THE SECOND BPF

W_a	W_b	W_c	W_d	W_e
2 μm	8 μm	16 μm	20 μm	26 μm
W_f	W_g	L_a	L_b	L_c
4 μm	2 μm	258 μm	264 μm	272 μm

both cases. Meanwhile, it is noted that the resonance pole of the BPF f_1 is slightly shifted to a lower frequency, because f_1 is also affected by the series-LC network. To further investigate the impact on frequency reponses due to the selection of C_2 and C_s, EM simulation is used. The simulated results are given in Fig. 15. As illustrated, both capacitances are critical for the BPF design. The value of C_2 is important for the stopband attenuation at the low freuqency, while the the value of C_s can be used to control the location of low-frequency transmission zero. To achieve an optimized performance, in this design, $C_s = 0.79$ pF and $C_2 = 0.08$ pF are used. In addition, the detailed physical dimensions of the folded strip-line for this case are summarized in Table III and the 3-D view of this BPF is given in Fig. 16.

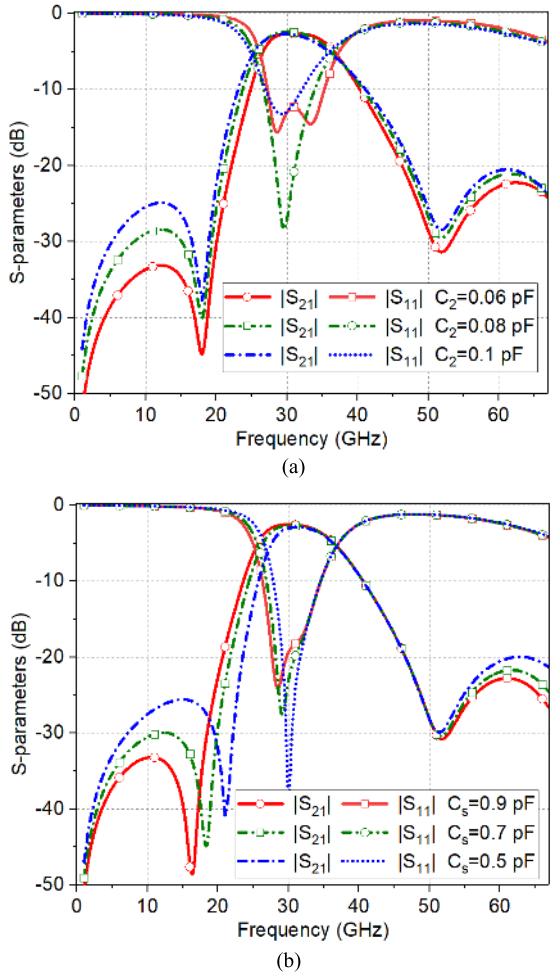


Fig. 15. Frequency responses of the second BPF. (a) $C_s = 0.78$ pF and C_2 is swept from 60 fF to 100 fF with a step of 20 fF. (b) $C_2 = 80$ fF and C_s is swept from 0.5 pF to 0.9 pF with a step of 0.2 pF.

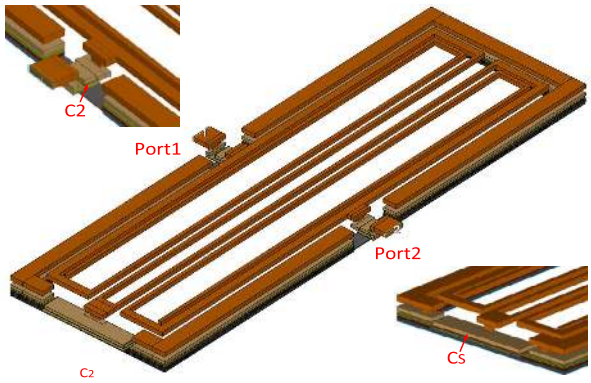
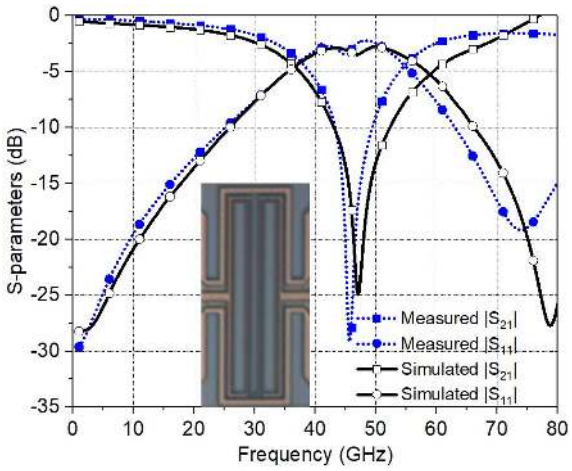


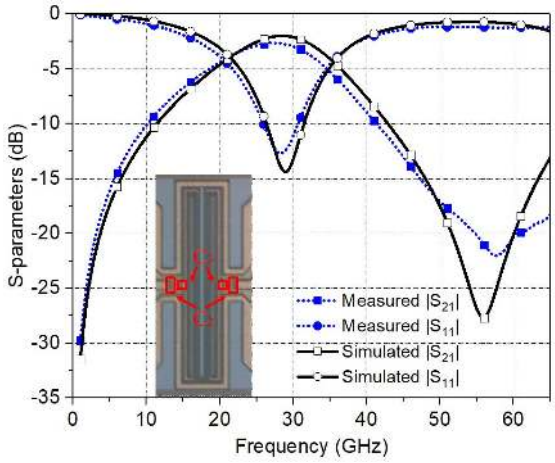
Fig. 16. 3-D view of the second BPF with highlighted MIM capacitors.

V. MEASUREMENT RESULTS AND DISCUSSION

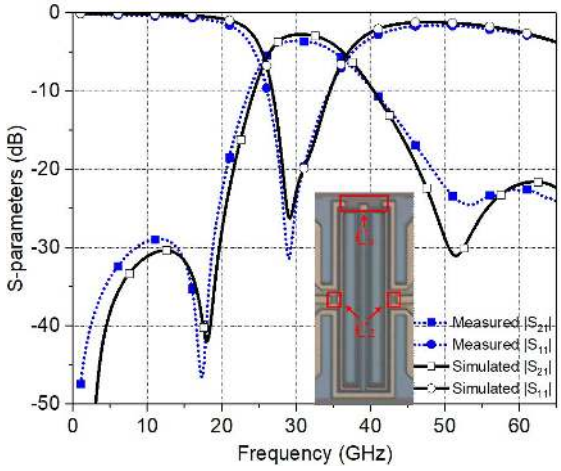
To evaluate the performance of the implemented resoantor as well as two BPFs, all three designs are fabricated in a standard 0.13-μm (Bi)-CMOS technology. Excluding the testing ground–signal–ground (G-S-G) pads, the chip sizes of the two BPFs are only 0.076×0.296 mm^2 and 0.096×0.296 mm^2, respectively. The size of the resonator is 0.096×0.294 mm^2. The measurements are conducted using on-wafer G-S-G



(a)



(b)



(c)

Fig. 17. Measured S-parameters. (a) Resonator. (b) First BPF. (c) Second BPF.

probing from 1 GHz up to 67 GHz with the help of a vector network analyzer E8361A and N5260-60003 from Keysight and 100-μm pitch (GSG) Waveguide Infinity Probes from FormFactor, Inc. The on-wafer calibration was made by using a conventional short–load–open–thru to move the reference planes from the connectors of the equipment to the tips of the RF probes. For comparison, both the EM simulated and measured $|S_{21}|$ and $|S_{11}|$ of the resonator as well as BPFs are plotted in Fig. 17(a)–(c), respectively.

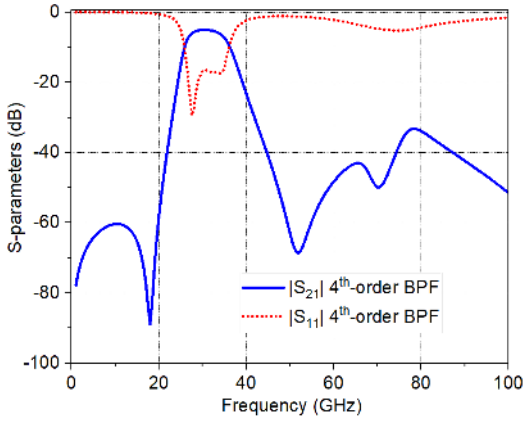


Fig. 18. EM simulation result of a fourth-order BPF using the presented resonators.

As illustrated in Fig. 17(a), the simulated self-resonant frequency appears at 47 GHz with 25-dB attenuation while the measured one has a notch at 46 GHz with 28-dB attenuation. Thus, a reasonable agreement between the EM simulated and measured results of the resonator is obtained. Moreover, as can be seen in Fig. 17(b), the first BPF has one transmission zero at 58 GHz with a peak attenuation of 23 dB. The center frequency of this filter is 27 GHz with an insertion loss of 2.5 dB, while the $|S_{11}|$ is better than 10 dB from 26 to 31 GHz. As demonstrated in Fig. 17(c), the second BPF has two transmission zeros, and a minimum insertion loss of 3.5 dB is found at 29 GHz. The $|S_{11}|$ is better than 10 dB from 26 to 34 GHz. Also, more than 20-dB stopband attenuation is achieved from dc to 20.5 GHz and from 48 to 67 GHz. The discrepancy between the simulated and measured results and some ripples that appeared in the measured results above 50 GHz are caused by the G-S-G pads and testing environment, which are not included in the EM simulation. The performance summaries of the presented BPFs as well as the other state-of-the-art designs are given in Table IV. Due to the lossy silicon substrate and ohmic loss, silicon-based BPFs have inherently high insertion loss comparing with their counterparts implemented in other technologies, such as GaAs. However, the presented designs, both the first- and second-order ones, have demonstrated an improved performance in terms of insertion loss, which can be found in the comparison table.

To further demonstrate that the presented approach is also feasible for implementation of a high-order BPF filter, a fourth-order BPF is also designed and the EM simulated results are given in Fig. 18. This BPF is implemented by cascading two of the previously presented second-order filters with additional interstage matching capacitance. It is clearly seen that a flat passband is formed with excellent cutoff selectivity and out-of-band rejection. The insertion loss is around 5.2 dB, and the in-band return loss is below the level of -17 dB. Moreover, due to the high order of the filter, the upper-stopband harmonic f_1', which is located at 78 GHz, is suppressed to -30 dB. Fig. 18 indicates that the proposed

TABLE IV
PERFORMANCE COMPARISONS WITH THE OTHER STATE-OF-THE-ART DESIGNS

REF.	*fc* (GHz)	Insertion loss (dB)	Filter order	Fractional bandwidth (%) ^	No. of TZs	Stopband suppression @ low frequency (dB)	Stopband suppression @ high frequency (dB)	Area (mm^2)	Technology
[17]	60	9.3	1st	10	n/a	n/a	n/a	0.11	0.18-µm CMOS
[18]	35	4.5	2nd	37.8	**2**	n/a	50	0.124	0.18-µm CMOS
[19]	65	3.4	2nd	18.5	2	35	30	0.074	0.18-µm CMOS
[20]	60	4.1	2nd	17	2	52	50	0.287	0.13-µm SiGe
[21]	25	2.5	2nd	31	3	50	38	0.28	0.13-µm CMOS
[22]	60	4	2nd	27.6	2	28	38	0.16	0.18-µm SiGe
[23]	60	2.5	1st	21	2	15	20	0.156	0.18-µm CMOS
[24]	31	2.4	1st	22.6	1	n/a	20	0.024	0.13-µm SiGe
[25]	33	2.6	1st	18	**1**	n/a	44	0.031	0.13-µm SiGe
[26]	59.5	3.3	2nd	21.7	2	17	27	0.054	0.18-µm CMOS
[27]	40	1.7	2nd	20	1	n/a	21	0.012	0.13-µm SiGe
[28]	31	3.9	3rd	68.5	2	25	45	0.073	0.13-µm SiGe
DESIGN 1	**27**	**2.5**	**1st**	**17.5**	**1**	**n/a**	**23**	**0.023**	**0.13-µm SiGe**
DESIGN 2	**29**	**3.5**	**2nd**	**26.7**	**2**	**47**	**24**	**0.028**	**0.13-µm SiGe**

NOTE: ^ The $|S_{11}|$ is better than -10 dB. All results are extracted from the manuscripts.

method can be used to implement high-order BPFs with better out-of-band rejections and in-band performance. The higher the filter order implemented, the higher the insertion loss must be accommodated. Thus, there is a design tradeoff between stopband suppression and in-band insertion loss.

VI. CONCLUSION

In this paper, a novel design methodology based on quasi-lumped elements is presented for miniaturized on-chip BPFs operating in mm-wave region. One resonator with enhanced self-coupling and two BPF design examples using this resoantor are given to satisfy different design specifications. To qualitatively demonstrate the principle of the presented designs, simplified *LC*-equivalent circuit models are given to investigate their transmission characteristics. Based on the investigation, the dimensions of both designs are optimized in a quantitative way using an EM simulator. To further prove that the presented designs are feasible in practice, all three designs are fabricated in a standard 0.13-μm (Bi)-CMOS technology. A reasonable agreement between the EM simulated and measured results is obtained. According to the overall performances of both designed BPFs, it can be concluded that the proposed methodology is particularly suitable for miniaturized design in silicon-based technologies. In addition, it can be codesigned with other building blocks where harmonics need to be tuned or suppressed, such as power amplifiers and frequency multipliers.

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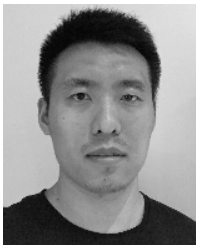

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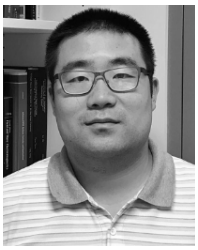

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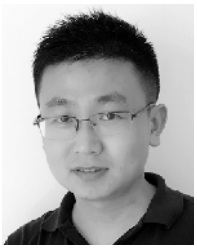

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