Compact Model Application to Statistical/Probabilistic Technology Variations

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ABSTRACT

ULSI systems are designed by electronic design automation (EDA) tools with performance figures-of-merit (FOM) measured by SPICE circuit simulation, in which nonlinear transistors are modeled by the compact model (CM) with its nominal set of parameters extracted from a golden die of the given technology. Inevitable technology variations are represented by parameter statistical distributions, from which process corners and variations are checked by Monte Carlo simulations within the design margins.

In this paper, we examine CM application to statistical and probabilistic technology variations based on the predictive and non-binnable model with minimal physically meaningful parameters. To capture geometry variations physically, a binned model with too many empirical fitting parameters can never provide physically meaningful statistics. Statistics and probability theories are applied to the mathematical CM for describing major transistor FOM and their bias, geometry, and process variations as well as functional parameter sensitivities. Propagation of model statistics and variations to higher-level primitives (such as logic gates) and its application to probabilistic CMOS design paradigms is explored.

Keywords: predictive compact model, probabilistic CMOS, process fluctuation, sensitivity analysis, statistical variation.

1 INTRODUCTION

As semiconductor technology continues to scale down following Moore's Law, statistical parametric variations have become a main show stopper and a dominating factor in design/yield considerations before reaching fundamental physical and technological limits. Traditionally, ULSI systems are designed by electronic design automation (EDA) tools with performance figures-of-merit (FOM) measured by SPICE circuit simulation, in which nonlinear transistors are modeled by the compact model (CM) with its nominal set of parameters extracted from a golden die of the given technology. Inevitable technology variations are represented by parameter statistical distributions, from which process corners and variations are checked by Monte Carlo simulations within the design margins. In such a design paradigm, the assumption is that the compact model faithfully captures the variations in all the dimensions of the identified parameter variations. This requires the model to be as physical and having a small number of parameters as possible in order to have meaningful statistics.

The "corner" models at the minimum/maximum values of the identified parameters from a CM represent the "worse/best"-case scenarios, although whether it is "worse" or "best" depends on the target parameters, and they usually give much larger design margins than realistically required. It is based on deterministic evaluations of the CM at its corner conditions that do not incorporate any probabilistic behaviors and parameter correlations.

In this paper, we apply our Xsim compact model [1] to statistical characterization of the silicon-nanowire (SiNW) MOSFET to demonstrate its predictive capability in capturing device structural/bias variations deterministically and statistically. The model has a small parameter set (~20) and has been fully calibrated with numerical devices as well as verified with experimental data. Similar approaches can be applied to bulk/SOI technologies. Transistor statistical characterization is a pre-requisite for accurate, meaningful circuit/gate-level statistical analysis. Application of the statistical/probabilistic-CM approach to the probabilistic-CMOS (PCMOS) [2] design paradigm is explored.

2 TRANSISTOR STATISTICAL CHARACTERIZATION

CM is essentially *transistor analytical characterization*, as opposed to TCAD, which is *transistor numerical characterization*, both aim to reproduce the electrical terminal characteristics of a real transistor, and both are deterministic in nature. What is being modeled is an idealized device with known geometries (gate length, oxide and body thickness, etc.) at given applied terminal biases. Variations of the device structure can be studied by changing the device parameters around their nominally designed values. For a good predictive CM or a well calibrated TCAD model, it should capture major variations as obtained from fabricated chips. In the context of designing circuits in the presence of parametric variations due to process fluctuations, such a predictive or scalable model is a pre-requisite, from which corner or statistical

models can be built with meaningful distributions and reliable target estimations.

We take a gate-all-around (GAA) SiNW MOSFET as the example to demonstrate the approach to transistor statistical characterization. The conceptual device cross section is shown in Fig. 1, with three major structural parameters, gate length L_g, NW radius R, and oxide thickness T_{ox}. A corresponding numerical device is also simulated by Medici for CM calibration. The device terminal dc characteristic is described by the CM as a function of its terminal biases V_{gs} and V_{ds}, as well as device parameters:

$$I_{ds} = f\left(V_{gs}, V_{ds}; L_g, R, T_{ox}, \ldots\right). \quad (1)$$

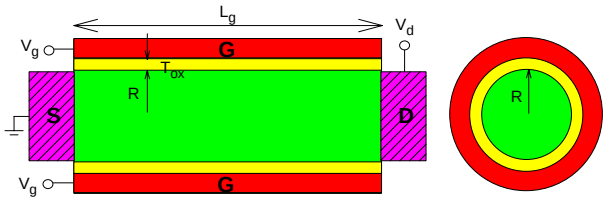


Figure 1: SiNW structure: three device parameters for variation: gate length (L_g), NW radius (R), and oxide thickness (T_{ox}).

2.1 Target–Variable Design Space and Model Calibration

At the single-transistor level, for digital designs, the target figures-of-merit (FOM) can be the turn-on (drive) current, defined as

$$I_{on} \equiv I_{ds}\big|_{V_{gs}=V_{ds}=V_{dd}} = f_1\left(V_{dd}; L_g, R, T_{ox}, \ldots\right) \quad (2)$$

and the turn-off (leakage) current, defined as

$$I_{off} \equiv I_{ds}\big|_{V_{gs}=0, V_{ds}=V_{dd}} = f_2\left(V_{dd}; L_g, R, T_{ox}, \ldots\right) \quad (3)$$

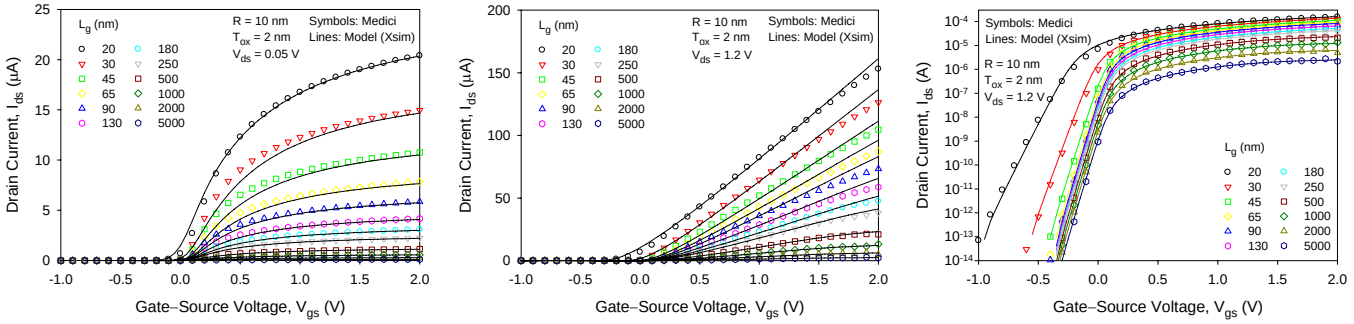
where V_{dd} is the supply voltage, which becomes a parameter with possible variations. For analog designs, FOM can be the transconductance

$$g_m \equiv \left.\frac{dI_{ds}}{dV_{gs}}\right|_{V_{gs}=V_{ds}=V_{dd}} = f_3\left(V_{dd}; L_g, R, T_{ox}, \ldots\right) \quad (4)$$

and the drain conductance

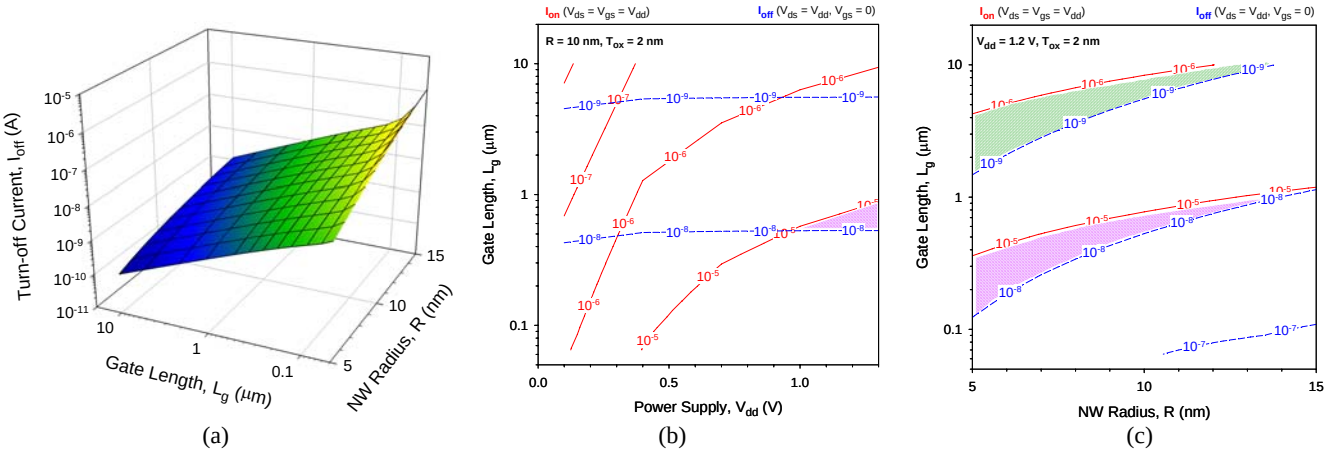
$$g_d \equiv \left.\frac{dI_{ds}}{dV_{ds}}\right|_{V_{gs}=V_{ds}=V_{dd}} = f_4\left(V_{dd}; L_g, R, T_{ox}, \ldots\right) \quad (5)$$

and its ratio g_m/g_d gives the intrinsic voltage gain. Other target parameters of interest can be the threshold voltage, subthreshold swing, etc.



(a) (b) (c)

Figure 2: Xsim SiNW model playback (lines) compared with the same Medici devices (symbols) at the nominal NW radius R = 10 nm and oxide thickness T_{ox} = 2 nm for various gate lengths L_g indicated in (a) linear region and in saturation region on (b) linear and (c) log scales.



(a) (b) (c)

Figure 3: (a) 3D surface plot of I_{off} vs. L_g and R. I_{off} and I_{on} contour plots for (b) L_g vs. V_{dd} and (c) L_g vs. R. Shaded regions indicate common parameter windows for satisfying both I_{off} and I_{on} optimization.

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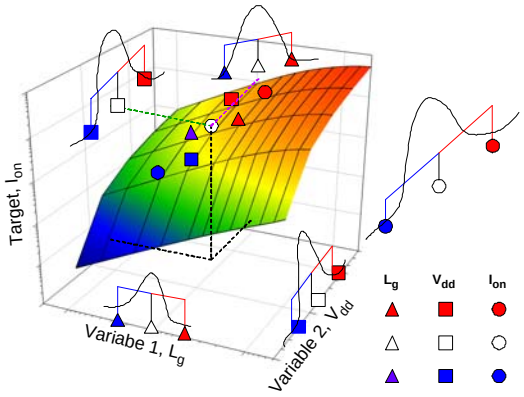


Figure 4: 3D surface plot of I_{on} vs. L_g and V_{dd}.

In this example, the Xsim model [1] has been calibrated to the 45-nm SiNW technology data from Medici with the nominal device parameters: L_g = 45 nm, R = 10 nm, T_{ox} = 2 nm. The model includes all major short-channel effects [3, 4] such as vertical/lateral-field mobility, velocity saturation/ overshoot, drain-induced barrier lowering (DIBL), series resistance, etc. Playback of I–V characteristics for various L_g (from 5 μm down to 20 nm) using a single parameter set is shown in Fig. 2. Model validation with the numerical data gives confidence in model prediction for geometry/bias variations and application to statistical analysis. The same model (with ~20 parameters) has also been verified with measured SiNW devices of various sized.

For two-target (I_{off} and I_{on}) optimization in the variable (L_g, R, T_{ox}, V_{dd}) design space, target–variable 3D surface plots and 2D contour plots can be easily generated. Fig. 3(a) shows one example 3D plot of I_{off} as a function of L_g and R. Figs. 3(b) and 3(c) are I_{off} and I_{on} optimization contour plots for L_g vs. V_{dd} and L_g vs R, respectively, in which a parameter window (shaded region) can be identified for a given set of $I_{off,max}$ and $I_{on,min}$ criteria.

2.2 Corner Models

Corner models are generated with ±12% variations around the nominal values of the three identified parameters. Due to physical scalability of the CM, any model evaluation within the corners can be validated with a corresponding numerical device with reasonable accuracy. Fig. 4 shows an example of the I_{on} surface plot vs. two variables, L_g and V_{dd}. Along each variable projection, the nonlinear target response (value) and its sensitivity (derivative) are well captured by the CM in the window of individual parameter corners, while the response to the combined variations gives 2^n target corners where n is the number of variables. Since these are deterministic evaluations of the CM, it is expected that the target will be bounded by the corner values from which best/worse-case scenarios can be determined.

2.3 Statistical Models

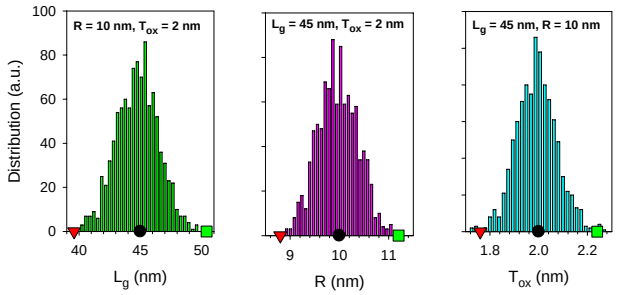


Figure 5: Individual parameter Gaussian distribution for (a) L_g, (b) R, and (c) T_{ox} with mean at nominal value and 3σ = 12% while the other two parameters being held at the nominal values; symbols indicate nominal (circle) and corner values (±12%).

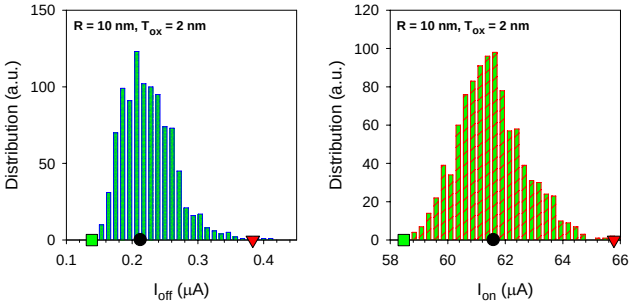


Figure 6: Monte Carlo results for (a) I_{off} and (b) I_{on} variations due to L_a variation alone; symbols for the corner model.

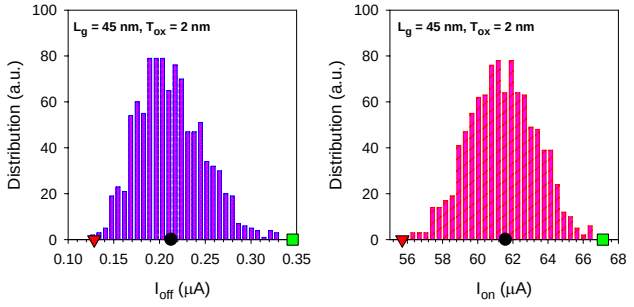


Figure 7: Monte Carlo results for (a) I_{off} and (b) I_{on} variations due to R variation alone; symbols for the corner model.

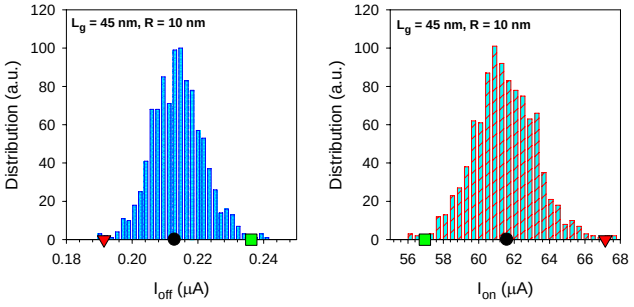


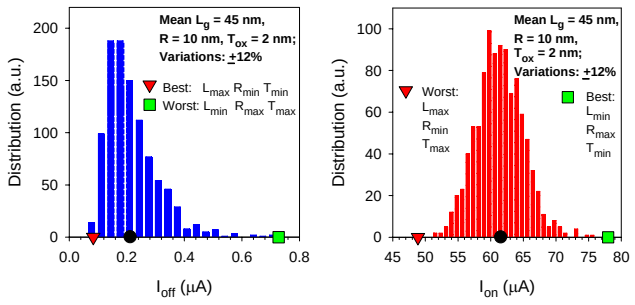
Figure 8: Monte Carlo results for (a) I_{off} and (b) I_{on} variations due to T_{ox} variation alone; symbols for the corner model.

For transistor statistical characterization using the CM, individual parameters (L_g, R, T_{ox}) are given a Gaussian

distribution with the mean (at nominal value) and 3σ variations (±12%), and random sampling is performed by the Monte Carlo method for a total of N = 1,000 samples. Fig. 5 illustrates the three individual parameter Gaussian distributions, together with the nominal/corner values.

Although each run is still the same (deterministic) CM evaluation, due to the nature of random sampling, the targets also follow some form of a Gaussian distribution, and some may be "distorted" due to the nonlinear model. This is shown in Figs. 6 to 8 for the I_{off} and I_{on} distributions due to one Gaussian random variable while holding the other two parameters at their nominal values. The corner-model values are also indicated by the symbols, which validate the sampled response from Monte Carlo runs.

With three combined random variations, parameter correlations are automatically captured and the joint probability distributions of I_{off} and I_{on} are shown in Figs. 9(a) and 9(b), respectively. There are eight corners for each target and the best/worse-case for I_{off} and I_{on} are found, as indicated in the plots, which tally with the physical understanding. The joint distributions fall well within the corner-model predictions, and are found to have narrower spread than the best/worse-case corners due to compensating effects.



(a) (b)

Figure 9: Monte Carlo results for (a) I_{off} and (b) I_{on} variations due to combined L_g, R, T_{ox} variations; symbols for the best/worse-case among the 8 corner models.

3 APPLICATION TO PROBABILISTIC-CMOS PARADIGM

The methodology presented in the previous section for transistors can be readily extended to intrinsic logic gates, in which gate-level FOM, such as delays, static/dynamic power, noise margin, etc., can be similarly characterized. Treating CM parameters as distributions or random variables and finding the FOM's distributions by Monte Carlo sampling or their moments from probability theory provides the notion of a "statistical/probabilistic compact model" (stat/prob-CM). This can be applied to the "Probabilistic-CMOS" (PCMOS) [2] design paradigm that exploits randomness in futuristic devices by taking advantage of probabilistic behaviors into chip designs. By allowing uncertainties in certain parts of the functional blocks for trading off power savings, algorithms with probabilistic Boolean theories have demonstrated feasibility and promising potential for PCMOS in sustaining future technology scaling.

One example of such an application is in the voltage or geometry (over)-scaling to trade off power consumption with probability of error in logic gates/blocks. In such a new design paradigm, it is essential to link a physically-based predictive CM to the probability distributions of gate-level FOM captured through statistical analysis.

4 SUMMARY AND CONCLUSIONS

In summary, a CM approach to transistor statistical characterization has been demonstrated with the Xsim SiNW model, validated by numerical data and the well predicted corner models. The approach can be generalized with more parameters and targets and can be extended to bulk/SOI CMOS. Similar approaches can be applied to basic circuit/gate building blocks, in which high-level FOM can be statistically characterized and modeled by the statistical/probabilistic compact model. Similar to the role CM has played in designing and optimizing system performance and correlating to technology variations, the systematic study centered on the *stat/prob-CM* paradigm provides a first step towards bridging the physical cause of random variations in real wafers to the performance of the circuits/systems being designed, in a new paradigm of technology/circuit co-design.

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REFERENCES

[1] G. J. Zhu, X. Zhou, G. H. See, S. H. Lin, C. Q, Wei, and J. B. Zhang, "A unified compact model for FinFET and silicon nanowire MOSFETs," *Proc. NSTI Nanotech*, Houston, TX, May 2009.

[2] B. E. S. Akgul, L. N. Chakrapani, P. Korkmaz, and K. V. Palem, "Probabilistic CMOS technology: a survey and future directions," *Proc. IFIP VLSI-SoC*, Nice, France, Oct. 2006.

[3] G. J. Zhu, G. H. See, S. H. Lin, and X. Zhou, "'Ground-referenced' model for three-terminal symmetric double-gate MOSFETs with source/drain symmetry," *IEEE Trans. Electron Devices*, vol. 55, no. 9, pp. 2526–2530, Sep. 2008.

[4] G. H. See, X. Zhou, K. Chandrasekaran, S. B. Chiah, Z. M. Zhu, C. Q. Wei, S. H. Lin, G. J. Zhu, and G. H. Lim, "A compact model satisfying Gummel symmetry in higher order derivatives and applicable to asymmetric MOSFETs," *IEEE Trans. Electron Devices*, vol. 55, no. 2, pp. 624-631, February 2008.