Compact Modeling of Organic Transistors with Multi-Finger Contacts

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I. Summary And Motivation

Organic thin-film transistors (OTFTs) with multi-finger contacts based on dinaphtho[2,3-b:2′,3′-f]thieno[3,2-b]thiophene (DNTT) exhibit near-zero turn-on voltage, hysteresis-free behavior, and high transconductance of 30-80 μA at V_{DS} = V_{GS} = −2 V. [1] In addition, common-source amplifiers based on such transistors deliver voltage gain even when the supply voltage is limited to 5 V, making them attractive for flexible/ wearable analog sensors. This paper presents the results of compact modeling, implemented in Matlab Simulink, applied to such transistors. The measured transistor transfer characteristics are used to extract the parameters for the semi-empirical model. The model was validated in 3 ways on 8 OTFTs with varied geometries and substrates (glass or PEN). The validation included calculations of (a) transistor output characteristics, (b) a.c. drain currents for 1 Hz sinusoidal gate voltages, and (c) output voltages of the common-source amplifier, and their comparison to the measured data.

II. Advances over Previous Works

The commercial success of thin-film transistors (TFTs) based on polycrystalline and hydrogenated amorphous silicon started the development of physical and/or semi-empirical transistor models to aid in the design of circuits and systems. [2] In the past 30 years such models have been extended to other TFT technologies, OTFTs including. Physical transistor models tend to be complex as a result of accurately capturing the physical behavior of the devices. If this requirement is relaxed, semi-empirical mathematical equations can be used to accurately describe the transistor drain current. Such models involve 'empirical', i.e., 'fitting' parameters, yet are able to predict with high accuracy the operating characteristics of the transistors while requiring shorter computation times.

To address particular principles and features of the OTFTs and/or adopt simplifications to provide an accessible analysis, various OTFT compact models were developed. [3-5] Examples include, a d.c. model considering Schottky barrier limitation on carrier injection in short channel transistors and a small signal a.c. non-quasi-static model addressing parasitic capacitances in printed devices which exhibit large process tolerances [6]. The aim of our semi-empirical model is to help with the design of flexible sensors and circuits implementing low-voltage OTFTs with multi-finger contacts based on DNTT and this paper represents the first step. The measured transistor transfer characteristics constitute the input data for the model that starts by producing the mathematical expression for the OTFT drain current as a function of the voltages applied on OTFT terminals. This drain current fitting procedure involves all transistor operating regimes including the subthreshold regime and the off-state. Afterwards one can model the drain current for d.c. and low-frequency a.c. conditions and output voltage of a common-source amplifier.

III. Results and Methodology

A compact model proposed in [7] served as a foundation for the model used in this work. Similar to [7], the transistor dimensions contribute via W and L, with no special provisions made for the source/drain finger geometry. In addition, the following simplifications were performed: (a) the number of empirical/fitting parameters was reduced from 5 to 4, and (b) the source/drain contact resistance was neglected. The model developed in Matlab Simulink environment computes the OTFT drain current based on a set of measured transfer characteristics. Eq. (1) defines the modeled drain current I_D

$$I_D = \frac{W}{L\left(1-\frac{\Delta L}{L}\right)} \cdot \frac{\mu_o}{\left(\frac{V_{SS}}{2+\gamma}\right)^{\gamma}} \cdot C \cdot \left[\frac{\left(V_{SS}\ln\left\{1+\exp\left[\frac{V_G-V_T-V_S-(V_G-V_S)\delta_{VT}}{V_{SS}}\right]\right\}\right)^{(\gamma+2)}}{\gamma+2} - \frac{\left(V_{SS}\ln\left\{1+\exp\left[\frac{V_G-V_T-V_D-(V_G-V_D)\delta_{VT}}{V_{SS}}\right]\right\}\right)^{(\gamma+2)}}{\gamma+2} \right] \quad (1)$$

where

$$\frac{\Delta L}{L} = \lambda(V_D - V_S) \cdot \frac{(V_D-V_S)+V_{GT\Delta L}}{2(V_D-V_S)+V_{GT\Delta L}} \geq 0 \quad (2)$$

Here V_G, V_D, and V_S are voltages on the gate, drain and source terminals, W is the channel width, L the channel length, C the gate dielectric capacitance and V_T the threshold voltage. The specific transistor determines W, L, C and V_T, as well as the transistor off-current. In addition, $V_{GT\Delta L} = \max(V_G - V_T, 0.01\,V)$ and $\lambda = 0.02$. The four empirical/fitting parameters are the subthreshold slope voltage V_{ss}, mobility enhancement factor γ, low-field mobility μ_o, and threshold voltage bias sensitivity δ_{VT}. To compute these parameters an objective function, defined as the mean squared error of the measured and fitted data, was minimized using a genetic algorithm.

The OTFT data used to develop and test the model were taken from the prior experiments performed with two types of multi-finger OTFTs shown in Figs. 1(a) and 1(b). [1] These low-voltage bottom-gate, top-contact p-channel OTFTs based on DNTT were fabricated either on glass (Ossila) or PEN

(Optfine, DuPont Teijin) substrates following the procedure described in [8]. The testing of the model was performed in 3 steps, each time producing a comparison with the measured data. Initially, the transistor transfer and output characteristics were simulated, next the a.c. drain currents for 1 Hz sinusoidal gate voltage were produced, and finally the output voltages of the common-source amplifier were modeled.

Figure 2 shows the measured and simulated transfer and output characteristics of a wide-gate transistor with W = 17.12 mm and L = 46.15 μm in linear and saturation regimes. As shown, the developed model is able to replicate the electrical performance of the transistor with high accuracy.

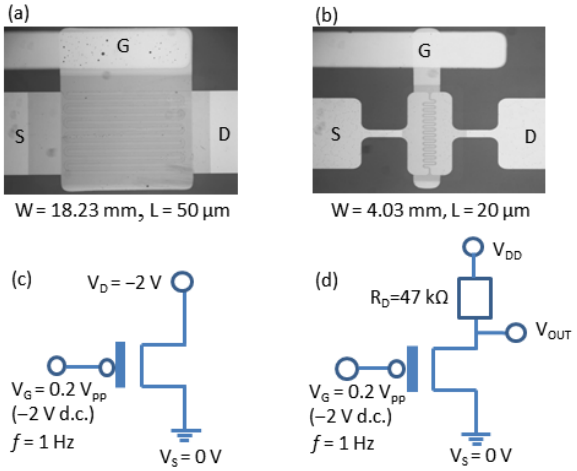

Fig. 1: Wide-gate (a) and narrow-gate (b) transistors, transconductance measurement (c), and transistor common-source amplifier (d).

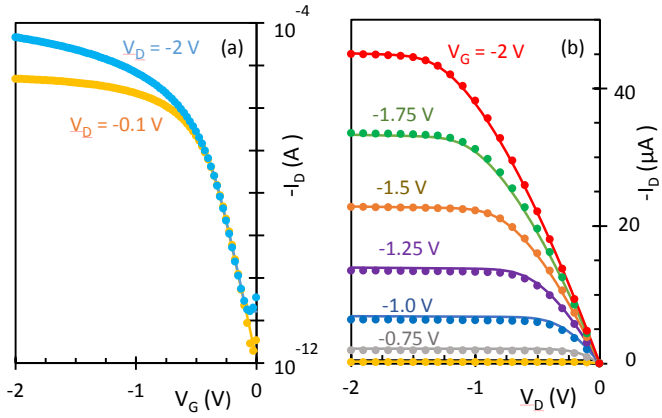

Fig. 2: Transistor transfer (a) and output (b) characteristics. The points are the measured data and solid lines are the model.

The a.c. transistor performance (Fig. 1(c)) and the output from the common-source amplifier (Fig. 1(d)) were simulated and the results are shown in Figs. 3(a) and 3(b) respectively. In addition, the peak-to-peak values of the measured and simulated drain current of six transistors with different W and L are summarized in Table I. The table also shows the comparison of the peak-to-peak output voltages of the transistor amplifier for different V_{DD}. Regarding the a.c. I_D, all simulated peak-to-peak values were slightly greater than the experimental values, resulting in error values ranging from 1.7% to 11.6%. Regarding the output voltage of Fig. 3(b) the error in the peak-to-peak voltage increased with decreasing V_{DD}, resulting in the highest percentage error for V_{DD} = −2 V. Overall, the simulated peak-to-peak output voltages were slightly higher when compared to the measured ones. This may result from the fact that only transfer characteristics in saturation regime (V_{DS} = −2 V) were available for the simulations shown in Fig. 3, while transfer characteristics in both the linear (V_{DS} = −0.1 V) and saturation regimes (V_{DS} = −2 V) were available for the simulations in Fig. 2. Consequently, the error is increased when the transistor operates in the linear regime.

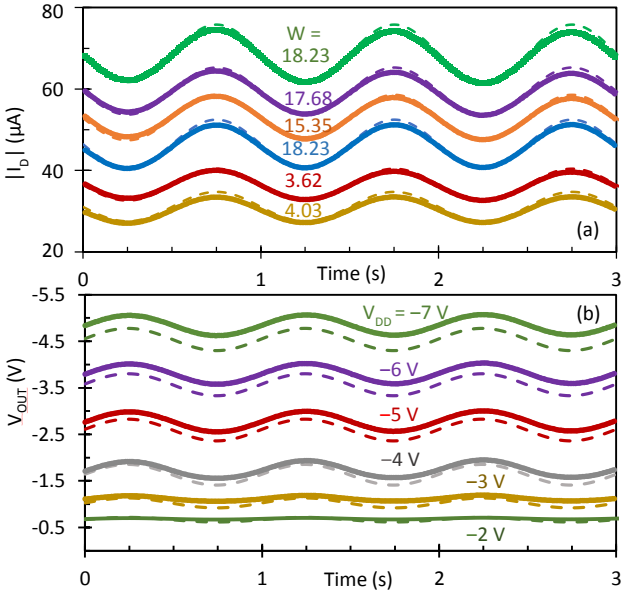

Fig. 3: A.c. drain current of Fig. 1(c) for transistors with various W (a) and output voltage of the transistor amplifier of Fig. 1(d) for various V_{DD} (b). The points correspond to the measured data and dashed lines to the model.

TABLE I. PEAK-TO-PEAK VALUES AND ERROR OF MEASURED AND SIMULATED DATA IN FIGURE 3

	Fig 3(a)					
W (mm)	18.23	17.68	15.35	18.23	3.62	4.03
I_{Dpp} meas (μA)	13.5	11.3	11.0	10.7	7.65	6.46
I_{Dpp} model (μA)	14.1	11.6	11.2	11.8	7.80	7.21
Error (%)	4.3	2.3	1.7	9.5	2.0	11.6
	Fig 3(b)					
V_{DD} (V)	−2	−3	−4	−5	−6	−7
V_{OUTpp} meas (V)	0.04	0.13	0.39	0.45	0.45	0.45
V_{OUTpp} model (V)	0.10	0.21	0.44	0.47	0.47	0.48
Error (%)	148.8	63.0	13.4	3.7	4.1	5.5

In summary, compact modeling was successfully applied to multi-finger OTFTs with high transconductance. While the model reproduces the OTFT d.c. characteristics well, additional work is needed to improve the accuracy of the low-frequency a.c. measurements in the future.

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