# Compact Modeling of Random Telegraph Noise in Nanoscale MOSFETs and Impacts on Digital Circuits

Mulong Luo, Runsheng Wang*, Jing Wang, Shaofeng Guo, Jibin Zou, Ru Huang*
Institute of Microelectronics, Peking University, Beijing 100871, China
*E-mails: ruhuang@pku.edu.cn; r.wang@pku.edu.cn

## Abstract

The complexity of Random Telegraph Noise (RTN) under digital circuit operations makes it difficult to predict its impacts without accurate modeling and simulation. However, properly integrating RTN into circuit simulation is challenging due to its stochastic nature. In this paper, RTN is comprehensively modeled and embedded into BSIM. A circuit simulation methodology based on industry-standard EDA tools is proposed, resolving the stochastic property, the AC effects, and the coupling of RTN and circuits that are crucial for accurate predictions of impacts of RTN. Using the compact model and proposed method, impacts of RTN on RO and SRAM are demonstrated, which ascertains their applicability to different type of circuits.

## Introduction

The random telegraph noise (RTN) in nanoscale CMOS devices has attracted growing attention because of the increasing impacts on circuits as the devices scale down [1-5]. However, properly integrating RTN into industry-standard EDA tools remains a challenge due to the highly stochastic nature, the AC effects, and the bi-directional coupling of RTN. As we have demonstrated, as in Fig. 1 for example, under AC signal excitations, RTN statistics show complicated frequency dependencies [3-5], which makes it very difficult to predict the impact of RTN without accurate simulations. There have been several works dedicated to the state-of-the-art RTN simulation methodology [6-8], however, to our knowledge, there are few works that is able to incorporate all these effects of RTN into circuit simulation.

Therefore, in this paper, RTN statistics is carefully modeled, taking the bias dependency into account. Based on this model, a transient simulation methodology is presented, which is capable of overcoming all these obstacles for integrating RTN into industry-standard EDA tools. Using this proposed method, the impacts of RTN on circuits are demonstrated, which ascertains the high precision and the broad applications in different circuits.

## Compact RTN Modeling and Circuit Simulation Method

To fully simulate the transient behavior of RTN under every possible operation conditions, the time constants and the amplitude of RTN under all biases should be precisely modeled. Based on our understandings [3-5,12] and other proven physics [8-11], the models are listed in Table 1. As depicted in Fig. 2 (a), the time constants are correlated to the surface potential of the transistor, which is a function of the gate and drain bias. For the amplitude model, it is known that the amplitude $\Delta V_{TH}$ or $\Delta I/I$ is a function of $V_{GS}$ [2], however, some factors are ignored in the previous models, e.g. Hole-in-the-inversion-layer model only considers the worst-case scenario. Recent atomistic simulation shows that the widely distributed trap amplitude distributes narrower in the on-state [11]. Based on these observations, a 3-piece amplitude model is adopted, as has been illustrated in Fig. 2(b). In the subthreshold region, $\Delta V_{TH}$ nearly holds the constant value $\Delta V_{TH0}$, in the inversion region, $\Delta V_{TH}$ changes linearly with the gate bias, while in strong inversion, $\Delta V_{TH}$ holds the same value $2\eta_0$. $\eta_0=q/C_{ox}$ is the threshold voltage shift calculated from classical charge sheet model. The drain current fluctuation $\Delta I$ is calculated by timing the transconductance. Using our model the time constants and the amplitude as the 2D functions of $V_{GS}$ and $V_{DS}$ for a certain trap are plotted in Fig. 3. It should be noted that this model can be fully embedded into the BSIM [13] model, with no need to connect a voltage source on the gate of the MOSFET, making it convenient to be used in circuit simulations.

Based on our newly proposed method [12], the flowchart of the simulation is illustrated in Fig. 4. First we initialize every modules in the circuit by setting the initial conditions and trap profiles. Then in time domain analysis, for each trap in each time step, we calculate the capture/emission probability based on the bias at that time and Monte-Carlo decide whether capture/emission will happen, after that the module modify the waveform of RTN based on bias and trapping occupancy. After that SPICE simulator calculates the biases for the rest part of the circuit. The process is repeated until the simulation ends. AC effects and coupling of RTN and circuits are naturally incorporated in this process. The simulation methodology is capable of analyzing RTN in highly noise-sensitive circuits like SRAM, or dynamic property, e.g. jitter, in large scale circuits.

## Results and Discussion

Our approach is demonstrated on the simple cases of Ring Oscillator (RO) and SRAM cells, typical benchmark for VLSI circuits. The devices are 16 nm double-gate bulk FinFETs using BSIM-CMG model in the following demonstrations. In Fig. 5(a) 5-stage RO with RTN is sketched. Due to impact of RTN, the eye-diagram (Fig. 5(b)) and the histogram of delay (Fig. 5(c)) show widely distributions. RO with various values of RTN parameters are simulated. Fig. 6 And Fig. 7 plot the average delay and jitter, defined as the standard deviation of delay, against the trap energy level $E_T$ and time constant $\tau_0$, respectively. Both jitter and delay of RO are sensitive to $E_T$ and $\tau_0$.

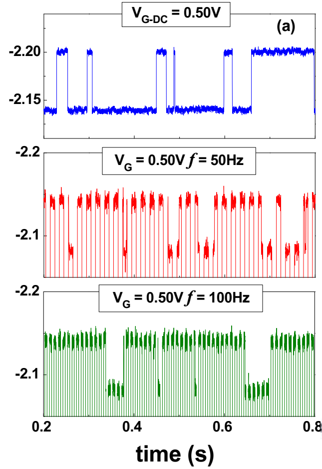
Fig. 8 demonstrate the impact of RTN on the failure probability of SRAM cells. A Non-0-or-1 plateau should be observed, which is believed to be induced by the non-0-or-1 trap occupancy rate of RTN at this supply voltage. Fig. 9 plots the simulation results of SRAM read-after-write failure probabilities with different trap energy levels. The plateau in results affirms the power of the methodology.

## Conclusion

A compact model of RTN for digital circuit simulation is presented. Using this model, a methodology for benchmark RTN in circuit is proposed, resolving the obstacles in simulation. Using this methodology, the impacts of RTN on RO and SRAM are demonstrated, which shows the strong capability for studying the impact of RTN on various circuits.

**Acknowledgement:** This work was partly supported by the National Basic Research Program of China (No.2011CBA00601), NSFC ((61106085 and 60625403), and National S&T Major Project (2009ZX02035-001)

978-1-4799-2217-8/14/$31.00 ©2014 IEEE



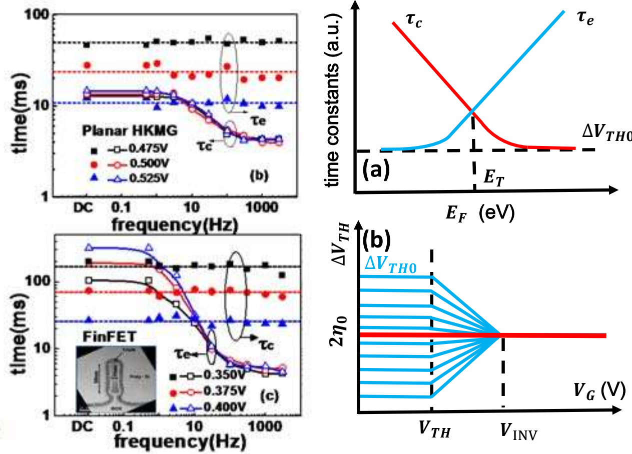




FIGURE 1. RTN statistics are found exhibiting complex frequency dependence. (a) The typical measured data of DC and AC RTN. The measured time constants have evident frequency dependence in (b) planar high-k/metal-gate (HKMG) devices and (c) multi-gate FinFETs.[3-5]

FIGURE 2. Schematic of the (a) time constants models and (b) the amplitude of RTN used for simulation.

**1.Trap time constants dependence:**

$\tau_c = \tau_0[1+\exp(-(E_T\text{-}E_f)/k_BT)]$

$\tau_e = \tau_0[1+\exp((E_T\text{-}E_f)/k_BT)]$

**2.Trap amplitude dependence:**

**(1)Subthreshold region ($V_{GS} \le V_{TH}$)**

$\Delta V_{TH} = \Delta V_{TH0}$

**(2)Inversion region ($V_{TH} < V_{GS} < V_{INV}$)**

$\Delta V_{TH} = \Delta V_{TH0} + (V_{GS} - V_{TH}) \times (2\eta_0 - \Delta V_{TH0})/(V_{INV} - V_{TH})$

**(3)Strong inversion region ($V_G \ge V_{TH}$)**

$\Delta V_{TH} = 2\eta_0$

**3.$\eta_0 = q/C_{ox}$**

**4.Drain current shift:**

$\Delta I = g_m \Delta V_{TH}$

TABLE 1: Compact RTN models used in this work

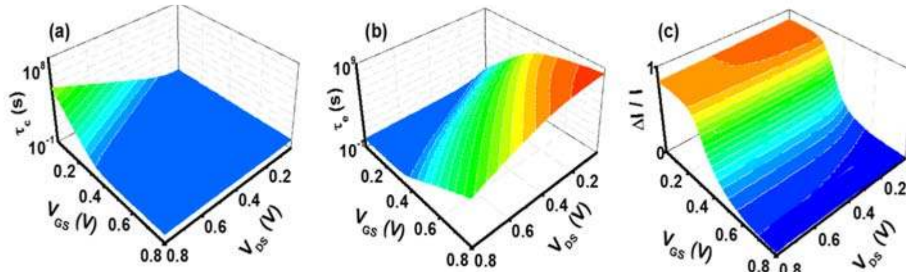



FIGURE 3. Plots of the dependences of (a)capture time constant $\tau_c$ (b) emission time constant $\tau_e$ (c)amplitude ΔI/I of RTN on gate and drain bias using the model in this work.

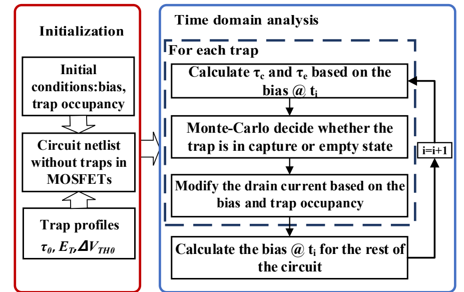



FIGURE 4. Flowchart of the circuit simulation in time domain.

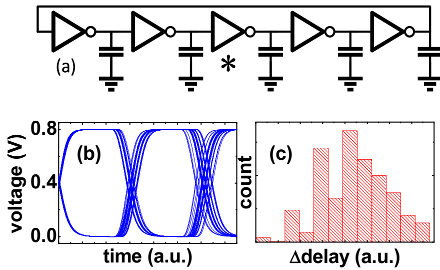



FIGURE 5. (a) 5-stage RO with RTN on the NMOS of one stage (denoted with an asterisk) (b) eye-diagram of the RO (c) histogram of the delay induced by RTN

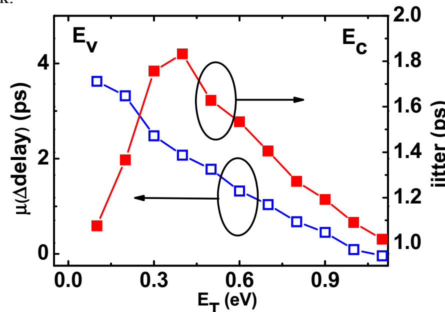



FIGURE 6. Delay shift and jitter of RO induced by RTN as a function of trap energy level.

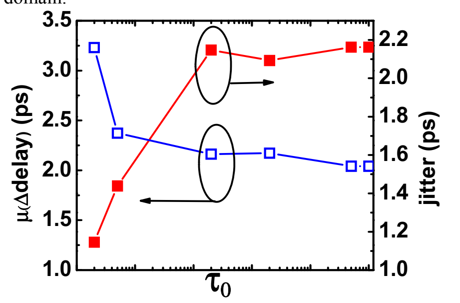



FIGURE 7. The impact of trap time constants of RTN on the delay and jitter of RO.

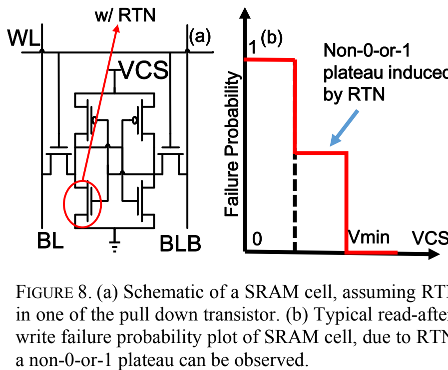



FIGURE 8. (a) Schematic of a SRAM cell, assuming RTN in one of the pull down transistor. (b) Typical read-after-write failure probability plot of SRAM cell, due to RTN, a non-0-or-1 plateau can be observed.

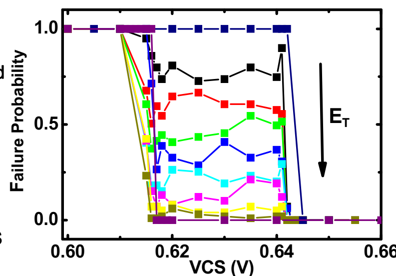



FIGURE 9. Read-after-write failure probability of SRAM against the supply voltage for RTN with different trap energy level.

## REFERENCES


[1] H. Miki, et al., ***IEDM** 2012*, p.450 [2] K. P. Cheung, et al., ***VLSI-TSA**, 2012*, p.1. [3] R.Wang, et al., ***VLSI-TSA** 2012*, p.1. [4] J.Zou, et al., ***VLSI** 2012*, p.139 [5] J. Zou, et al., ***VLSI** 2013*, p.187 [6] K. Aadithya, et al., ***DATE** 2011*, p.1. [7] Y. Ye, et al.,***ICCAD** 2010*, p.709. [8] G.Wirth ***Microelectron. Reliab***., vol. 52, p.2955, 2012 [9] T. Grasser, ***Microelectron. Reliab***., vol.52, p.39., 2012. [10] M. Kirton, et al., ***Adv. Phys.***, vol. 38, p.367., 1989. [11] J. Franco, et al.,***IRPS** 2012*, 5A.4.1 [12] R. Wang, et al.,***IEDM** 2013*,33.5

[13] www-device.eecs.berkeley.edu/bsim/