

Compact Modeling of Short Channel Double-Gate MOSFETs

Huaxin Lu, Xiaoping Liang, Wei Wang, and Yuan Taur

University of California, San Diego, La Jolla, CA, U.S.A., hlu@ucsd.edu

ABSTRACT

Compact models of short channel effect in symmetric and asymmetric double gate MOSFETs are developed by solving two-dimensional (2-D) Poisson's equation as a boundary value problem in the subthreshold region. The subthreshold current is obtained through the 2-D analytic potential distribution function. Threshold voltage rolloff, drain induced barrier lowering (DIBL) and subthreshold slope degradation as a function of channel length are extracted from the subthreshold current expression. The short channel effect model is validated by 2-D numerical simulation and incorporated into the analytical potential model for DG MOSFETs.

Keywords: analytic potential model, compact model, double gate MOSFETs, short channel effect

1 INTRODUCTION

DG MOSFETs have been recognized as one of the options to further extend CMOS scaling when planar bulk MOSFETs have reached its practical scaling limits [1]. Short channel effect, as an indicator of device scalability, is the predominant factor that limits how far the DG MOSFET can be scaled. A number of authors have investigated on analytical models for short channel effect in DG MOSFETs. Among numerous models that have been proposed, the 3-D modeling method [2], although physical, is too complicated for compact modeling. Another approach assumes a parabolic potential function in the vertical direction, which results in large error when one of the thicknesses is much larger than the other [3]. One more elaborate method approximates quasi-Fermi potential by a 1-D δ function, making it incapable of modeling DIBL effect [4]. In this paper, a comprehensive physics-based compact short channel effect models including threshold voltage rolloff, DIBL and subthreshold slope degradation are developed and incorporated in the analytic potential model for symmetric and asymmetric DG MOSFETs [5]. As the model solves the Poisson's equation in both silicon and insulator regions, it can apply to arbitrary silicon and insulator thickness including high-k gate dielectrics, which has not been properly modeled by previous work.

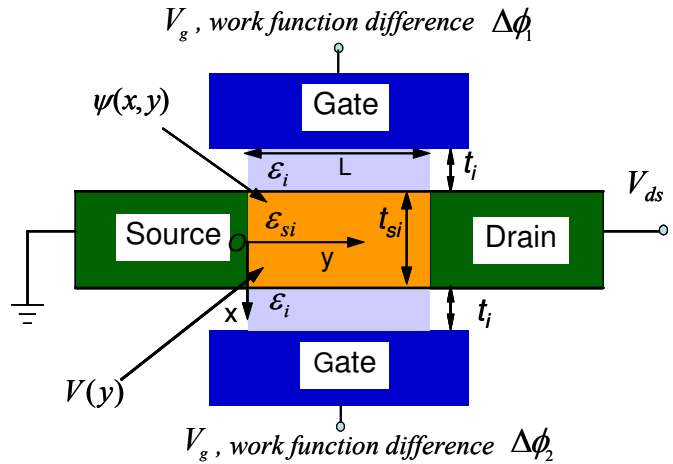


Fig.1. Schematic diagram of a double-gate MOSFET. $\Delta\phi_{1,2}$ are the work function difference between the top/bottom gate electrode and intrinsic silicon. $\Delta\phi_1 = \Delta\phi_2$ for a symmetric DG MOSFET, $\Delta\phi_1 \neq \Delta\phi_2$ for an asymmetric DG MOSFET.

2 SHORT CHANNEL EFFECT MODELS IN DG MOSFETs

2.1 Full 2D potential and subthreshold current solution

For an undoped DG MOSFET in the subthreshold region, the mobile charge and fixed charge are negligible as they have little impact on the threshold voltage [6]. Therefore, Poisson's equation becomes Laplace equation in both the silicon and insulator region

$$\frac{\partial}{\partial x} \left(\varepsilon \frac{\partial \psi}{\partial x} \right) + \frac{\partial}{\partial y} \left(\varepsilon \frac{\partial \psi}{\partial y} \right) = 0 \quad (1)$$

where $\psi(x,y)$ is defined as the electrostatic potential at (x,y) with respect to Fermi potential of the n+ source, ε is the permittivity of silicon or the insulator.

Using the superposition method and neglecting high order terms, the 2-D potential expression in the subthreshold region has been solved by X. Liang [7]

$$\psi(x,y) = \frac{\Delta\phi_1 - \Delta\phi_2}{t_{si} + 2t_i\varepsilon_{si}/\varepsilon_i} x + V_g - \frac{\Delta\phi_1 + \Delta\phi_2}{2} + \frac{b_1 \sinh[\pi(L-y)/\lambda_1] + c_1 \sinh(\pi y/\lambda_1)}{\sinh(\pi L/\lambda_1)} \cos(\pi x/\lambda_1) \quad (2)$$

where V_g is the gate voltage, E_g is band gap of silicon, L is the gate length, $\Delta\phi_1$ and $\Delta\phi_2$ are work function difference between the two gates and intrinsic silicon. Without loss of generality, we assume $\Delta\phi_2 \geq \Delta\phi_1$. Other parameters are listed as follows

$$b_1 = B (E_g / 2q + \frac{\Delta\phi_1 + \Delta\phi_2}{2} - V_{g0}) \quad (3)$$

$$c_1 = B (E_g / 2q + V_{ds} + \frac{\Delta\phi_1 + \Delta\phi_2}{2} - V_{g0})$$

$$B = \frac{2\lambda_1^2 \tan(\pi t_i / \lambda_1) \sin(\pi t_{si} / 2\lambda_1)}{\pi^2 t_i [t_{si} / 2 + t_i \sin(\pi t_{si} / \lambda_1) / \sin(2\pi t_i / \lambda_1)]} \quad (4)$$

where

$$V_{g0} = \frac{E_g}{4q} + \frac{\varepsilon_{si} t_i / \varepsilon_i}{t_{si} + 2\varepsilon_{si} t_i / \varepsilon_i} \Delta\phi_2 + \frac{t_{si} + \varepsilon_{si} t_i / \varepsilon_i}{t_{si} + 2\varepsilon_{si} t_i / \varepsilon_i} \Delta\phi_1 \quad (5)$$

λ_1 is the scale length that can be solved from the following equation

$$\tan(\pi t_i / \lambda_1) \tan(\pi t_{si} / 2\lambda_1) = \varepsilon_i / \varepsilon_{si} \quad (6)$$

To avoid the complexity of solving the above implicit equation in compact model, an explicit expression can be developed as a function of the ratio $r = t_{si} / t_i$ to facilitate the speed of simulation. For instance, when the insulator is silicon dioxide ($\varepsilon_i = 3.9$),

$$\lambda_1 = (r^4 + 23.98r^3 + 219.8r^2 + 96.18r + 15.98)^{1/4} t_i \quad (7)$$

Once the analytical potential is solved, $I_{ds} - V_g$ curves in the subthreshold region can be derived with the analytical solution. Current continuity equation can be written as

$$I_{ds}(y) = -\mu W \frac{dV(y)}{dy} Q_i(y) \quad (8)$$

where

$$Q_i(y) = \int_{-t_{si}/2}^{t_{si}/2} n(x, y) q dx = \int_{-t_{si}/2}^{t_{si}/2} n_i q e^{q[\psi(x, y) - V(y)] / kT} dx \quad (9)$$

is the inversion charge per gate area. Current continuity requires I_{ds} to be independent of y . Therefore, integration of (8) with respect to y from 0 to L yields [8]

$$I_{ds} = \frac{\mu W (kT / q) [1 - \exp(-qV_{ds} / kT)]}{\int_0^L \frac{dy}{\int_{-t_{si}/2}^{t_{si}/2} n_i q e^{q\psi(x, y) / kT} dx}} \quad (10)$$

2.2 Threshold voltage rolloff and DIBL model [9]

Threshold voltage ΔV_t is extracted from the parallel shift of $I_{ds} - V_g$ curves of short channel device with respect to the long channel device at the same current level normalized to W/L . The constant current level is chosen at gate voltage $E_g/4q$ below the threshold voltage such that the device is biased in the deep subthreshold region. The following equation is used to extract the threshold voltage shift

$$I_{ds} L(\text{short channel}) = I_{ds} L(\text{long channel}) \times e^{\frac{q}{kT}(-\Delta V_t)} \quad (11)$$

The subthreshold drain current expression (10) contains a double integral in the denominator which cannot be carried out analytically. Thus the 2-D potential function $\psi(x, y)$ needs to be simplified to derive ΔV_t .

The drain current is largely controlled by the point of maximum electron energy barrier (minimum potential) at y_c in the channel direction. In the vertical direction, the drain current is controlled by the maximum electron density (maximum potential) at x_c . $x_c = 0$ for a symmetric DG and $x_c \neq 0$ for the asymmetric case; y_c is obtained by solving $\partial\psi(x, y) / \partial y|_{y=y_c} = 0$. As the spatial variation in y direction is much more important to include than that in x direction [10], we take Taylor expansion of $\psi(x, y)$ in the y direction at (x_c, y_c) ,

$$\psi_{Taylor}(x, y) = \psi(x_c, y_c) + \frac{1}{2}(y - y_c)^2 \frac{\partial^2 \psi}{\partial y^2}(x_c, y_c) \quad (12)$$

where

$$x_c = \begin{cases} \frac{2\lambda_1}{\pi} \sin^{-1} \left[\frac{\lambda_1 (\Delta\phi_1 - \Delta\phi_2) e^{\pi L / 2\lambda_1}}{2\pi \sqrt{b_1 c_1} (t_{si} + 2\varepsilon_{si} t_i / \varepsilon_i)} \right] & \text{for } C \leq 1 \\ -\frac{t_{si}}{2} & \text{for } C > 1 \end{cases} \quad (13)$$

$$C = \frac{\lambda_1}{2\pi} \frac{t_{si} + 2\varepsilon_{si} t_i / \varepsilon_i}{\sqrt{b_1 c_1} \sin(\pi t_{si} / 2\lambda_1)} e^{\pi L / 2\lambda_1} \quad (14)$$

and

$$y_c = \frac{L}{2} - \frac{\lambda_1}{2\pi} \ln\left(\frac{c_1}{b_1}\right) \quad (15)$$

In order to analytically extract ΔV_t , we compromise the full 2-D potential distribution (2) by a 1-D parabolic potential distribution (12). Substituting (12) into the extraction equation (11) and solving for ΔV_t result in

$$\Delta V_t = -2\sqrt{b_1 c_1} e^{-\pi L / 2\lambda_1} + \frac{kT}{q} \ln \left\{ \frac{\sqrt{\pi}}{2D_1 L} \left[\text{erf}(D_1(L - y_c)) + \text{erf}(D_1 y_c) \right] \right\} \quad (16)$$

where

$$D_1 = \left(\frac{\pi^2 q \sqrt{b_1 c_1} e^{-\pi L / 2\lambda_1}}{\lambda_1^2 kT} \right)^{1/2} \quad (17)$$

and function erf is the error function defined as

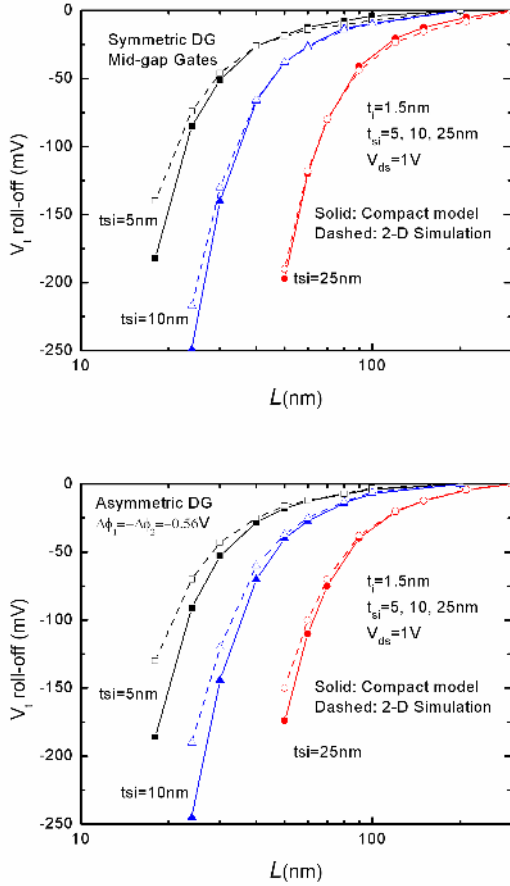


Fig.2. Threshold voltage roll-offs for symmetric and asymmetric DG MOSFETs with $t_i=1.5\text{nm}$ and $t_{si}=5,10,25\text{nm}$, compared with 2-D ISE simulation

$$\text{erf}(x) = \frac{2}{\sqrt{\pi}} \int_0^x e^{-u^2} du \quad (18)$$

The integral in the error function can be eliminated in SPICE by replacing (18) with an explicit fitting function

$$\text{erf}(x) \approx \frac{2}{\pi} \tan^{-1} \left[\frac{\pi}{2} (x + 0.5x^2 + 0.1x^3 + 1.2x^4) \right] \quad (19)$$

Fig.2 compares V_t rolloff computed by the compact model and 2-D numerical simulation as a function of gate length L . Different silicon film thicknesses are considered in both symmetric and asymmetric MOSFETs. The overall agreement is good except when the channel length is extremely short (24nm) where the omission of high order terms in the potential solution causes larger deviations.

As can be seen from (3) and (16), DIBL effect is incorporated in the threshold voltage rolloff model through V_{ds} -dependent parameter c_1 . The DIBL effect is calculated in Fig. 3 in comparison with ISE simulation result.

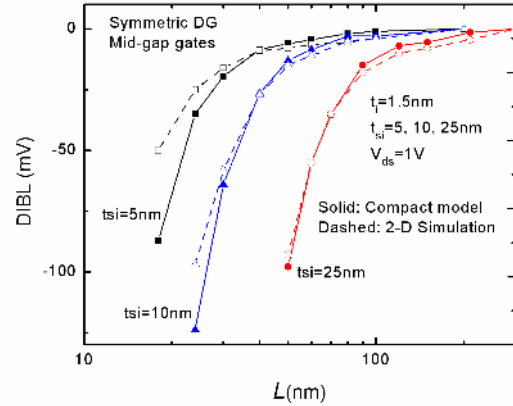


Fig. 3 DIBL effect for symmetric DG MOSFETs compared with 2-D numerical simulation

2.3 Subthreshold slope degradation model

In order to extract the subthreshold slope from (10), we further simplify the current expression by approximating the potential $\psi(x, y)$ with a constant potential value at the minimum potential point (x_c, y_c) . The subthreshold slope for DG MOSFETs can be extracted:

$$S \approx \left\{ 1 - 2B \left[1 + \frac{1}{8} \left(\frac{V_{ds}}{E_g/2q + V_{ds}/2 - V_{g0}} \right)^2 \cos(\pi x_c / \lambda_1) \exp(-\pi L / 2\lambda_1) \right] \right\}^{-1} \quad (20)$$

$\times 60 \text{ mV/decade}$

Fig. 4 shows that the analytical subthreshold slopes for symmetric and asymmetric DG MOSFET are in good agreement with 2D numerical simulation results for $L > 1.5\lambda_1$. It is shown that the subthreshold slope for asymmetric DG is better than that for symmetric DG, especially for $L < 2\lambda_1$. This could be due to the fact that for symmetric DG, the minimum potential is located at the center of the film, while for asymmetric DG, it is closer to one gate. Therefore the minimum potential in the asymmetric DG is more controlled by the gate than by the source/drain.

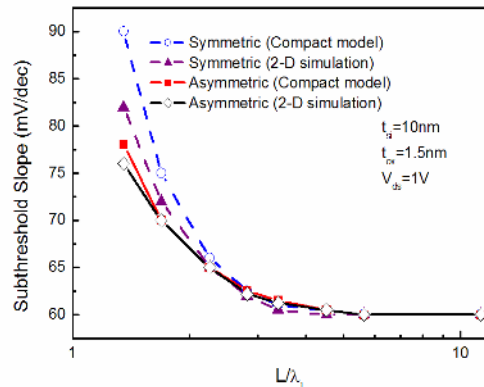


Fig.4 Analytical solutions of the subthreshold slopes for symmetric and asymmetric DG MOSFETs compared with 2-D numerical simulation results.

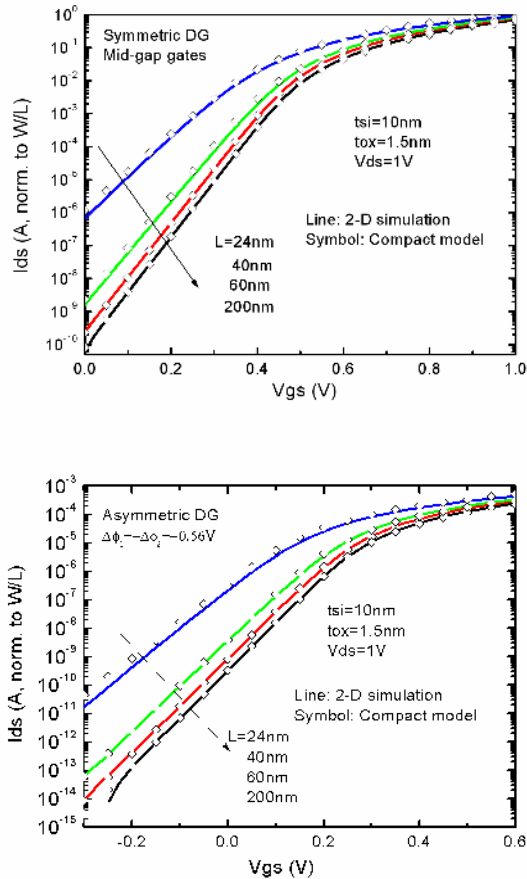


Fig.5 I_{ds} - V_g curves for symmetric DG MOSFETs ($\epsilon_f=3.9\epsilon_0$) calculated from the analytical model (solid curves), compared with 2-D numerical simulation results (dashed curves).

3 MODEL IMPLEMENTATION

The short channel effect models have been implemented in the analytic potential model in SPICE3. The analytic potential model is a long channel core model for symmetric and asymmetric MOSFETs. With the implementation of the short channel effect models, the SPICE simulated drain current curves plotted in Fig. 5 show close agreement with the 2-D numerical simulation result by ISE for both symmetric and asymmetric DG MOSFETs.

4 CONCLUSIONS

In conclusion, compact models for short channel effect including threshold voltage rolloff, DIBL and subthreshold slope degradation are developed for symmetric and asymmetric DG MOSFETs based on the full 2-D potential distribution and subthreshold current expression. The models are implemented in the analytic potential model for

DG MOSFETs in SPICE3 and reproduce the drain current in close agreement with simulation results.

REFERENCES

- [1] International Technology Roadmap for Semiconductors: 2005 <http://public.itrs.net/>
- [2] G. Pei, V. Narayanan, Z. Liu, and E. C. Kan, "3D analytical subthreshold and quantum mechanical analyses of double-gate MOSFET", IEDM 2001.
- [3] K. Suzuki, Y. Tosaka, and T. Sugii, "Analytical threshold voltage model for short channel n+-p+ double-gate SOI MOSFET's", *Trans. Electron Devices*, vol.43, pp.732-738, May 1996.
- [4] Q. Chen, E. M. Harrell, and J. D. Meindl, "A physical short-channel threshold voltage model for undoped symmetric double-gate MOSFETs", *IEEE Trans. Electron Devices*, vol.50, pp.1631-1637, July 2003.
- [5] H. Lu and Y. Taur, "An analytic potential model for symmetric and asymmetric double gate MOSFETs", To be published in *IEEE Trans. Electron Devices*, May, 2006.
- [6] H.-S. P. Wong, D. J. Frank, and P. M. Solomon, "Device design considerations for double-gate, ground-plane, and single-gated ultra-thin SOI MOSFETs at the 25 nm channel length generation," *IEDM Tech. Dig.*, p. 407, 1998.
- [7] X. Liang and Y. Taur, "A 2-D analytical solution for short channel effects in double-gate MOSFETs," *IEEE Trans. Electron Devices*, Vol.51, no.9, pp.1385, 2004.
- [8] Y. Taur and T. H. Ning (1998) *Fundamentals of modern VLSI device*, Cambridge University Press.
- [9] X. Liang, "Analytical Modeling of Short Channel Effect in Double-Gate MOSFETs", Ph.D. thesis, University of California, San Diego.
- [10] Y. Taur, X. Liang, W. Wang, and H. Lu, "A continuous, analytic drain-current model for DG MOSFETs," *IEEE Electron Device Lett.*, vol. 25, pp. 107-109, Feb. 2004.