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Compact Modeling of Surface Potential, Drain Current and Terminal Charges in Negative Capacitance Nanosheet FET including Quasi-Ballistic Transport

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ABSTRACT In this article, we propose a compact model for Negative Capacitance Nanosheet Field Effect Transistor (NC-NSFET) including quasi-ballistic transport for sub-7nm technology node. The model captures the electrical characteristics of NC-NSFET for different ferroelectric thicknesses. Further, it captures the reverse short channel effects of NCFET for different channel lengths with a single set of parameters. Also, we build a model for terminal charges of NC-NSFET using the core model and the earlier developed inner fringing charge model. Using our physics-based model, we find that quasi ballistic transport worsens the capacitance matching in NCFET compared to drift-diffusion only case. We validate the compact model for the drain current and the terminal charges with the TCAD results. The proposed compact model is computationally efficient and implemented in the Verilog-A code to enable SPICE circuit simulations. Finally, we demonstrate this by applying our model for NC-NSFET based CMOS inverter and SRAM circuit implementations in SPICE.

INDEX TERMS Negative capacitance, MFIS, ferroelectric, nanosheet, FinFET, nanowire, quasi-ballistic transport, short channel effects.

I. INTRODUCTION

Beyond 7nm technology node, owing to significantly large short channel effects (SCEs), the state-of-the-art FinFET devices may have to be eventually replaced by the geometries with a superior gate controllability such as nanosheet and nano-wire FETs [1]–[3]. Moreover, the recent discovery of negative capacitance effect originating from the ferroelectric layer present in the gate stack of NCFET can further augment the subthreshold integrity and even provide a larger ON state current than the conventional FETs [4]–[7]. The fringing field effect in a short channel NCFET has been found to significantly lower the steady-state leakage of the device, which can help in continuing Dennard's scaling for the CMOS devices, i.e., increasing the frequency of the processor with every new technology node [8]–[10]. Thus, ferroelectric NC based gate all around FET is expected to be a suitable candidate for futuristic ultra-scaled channel devices. To enable large-scale circuit design with such devices, a computationally efficient compact model is essential to evaluate the design quality and circuit performance. In this work, we develop a Verilog-A implementable compact model for sub-7nm NC-NSFET using the Landau-Khalatnikov (L-K) equation for the ferroelectric layer. We include the drift diffusive as well as ballistic transport in our model, which is inevitable at such small dimensions [11]. In addition to our previous work [12], we develop a terminal charge model in this article using the

TABLE 1. Device design parameters of NSFET and NC-NSFET.

Device Parameters	Values	Ref
Gate Length (L)	12 nm	[3]
Nanosheet Thickness ($T_{\rm NS}$)	5 nm	
Nanosheet Width ($W_{\rm NS}$)	50 nm	
Spacer Length ($L_{\rm SP}$)	5 nm	
Spacer Dielectric Constatnt (k)	4	
Interfacial EOT ($T_{\rm OX}$)	0.9 nm	
Ferroelectric Coefficient (a)	-1.03×10^9 m/F	[14]
Ferroelectric Coefficient (b)	3.5×10^{10} m^5/C^{2}F	
Coupling Coefficient (g)	1×10^{-4} cm^3/F	[15]

core model and inner fringing charge model, which is based on the capacitive network approach [8].

The paper is organized as follows. In Section II, we discuss the framework for the simulation of NC-NSFET, which we later require for the validation of our compact model in Section III. In Section III, we explain the compact modeling flow and its validation with the TCAD results. In Section IV, we study the static noise margin of CMOS inverter and 6-T SRAM circuits. Finally, we conclude this work in Section V.

II. TCAD SIMULATION FRAMEWORK

To validate the compact model, we simulate a sub-7nm NC-NSFET in the Sentaurus 3D TCAD simulator [13]. The simulated structure of NC-NSFET is shown in Fig. 1(a). the cross section of the NC-NSFET is shown in Fig. 1(b), which describes the doping profile in the channel. For the device simulation, we incorporate the Fermi Dirac statistics, ballistic mobility model, quantum confinement effect, SRH, and Auger recombination models. The baseline Nanosheet FET (NSFET) in the Sentaurus TCAD with gate length (L_G) of 12nm is first calibrated with the experimental data [3] for both $V_{\rm ds} = 50$mV and $V_{\rm ds} = 0.7$V, as shown in Fig. 2. The other device parameters for the NSFET are shown in black color in Table 1. For the simulation of NC-NSFET, we keep the geometry and the metal gate work function same as the calibrated NSFET, with an additional ferroelectric layer of thickness $T_{\rm FE}$ on the top of the interfacial oxide layer of the baseline NSFET. For the ferroelectric layer, we use the L-K equation with the parameters shown in purple color in Table 1.

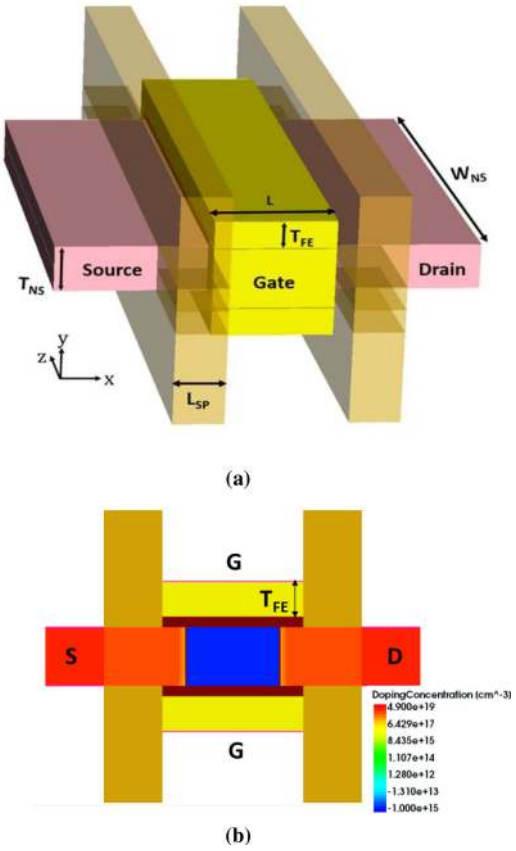

FIGURE 1. (a) Simulated 3D device structure of Negative Capacitance Nanosheet Field Effect Transistor (NC-NSFET) in Sentaurus TCAD. The device parameters of baseline NSFET and NC-NSFET are listed in Table 1. (b) Cross section of NC-NSFET along the *x*-axis, which shows the doping profile in the channel.

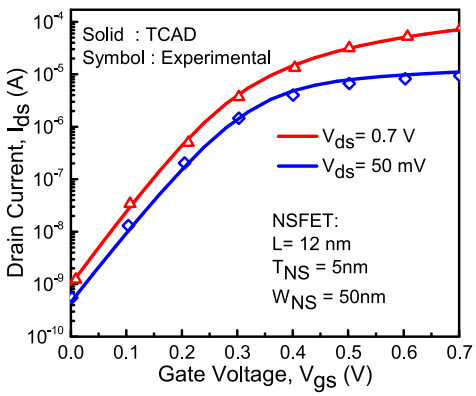

FIGURE 2. The calibration of $I_{\rm ds} - V_{\rm gs}$ characteristics of baseline NSFET for both $V_{\rm ds} = 50$mV and $V_{\rm ds} = 0.7$V with experimental results [3] in Sentaurus 3D TCAD tool.

III. MODEL DEVELOPMENT AND VALIDATION

A. SURFACE POTENTIAL

To accurately model the potential in the channel, we need to solve 2-D Poisson's equation for an undoped channel which is given by

$$\frac{\partial^2 V(x,y)}{\partial x^2} + \frac{\partial^2 V(x,y)}{\partial y^2} = \frac{q}{\varepsilon_s} n(x,y) \tag{1}$$

where V is the potential in the channel, x is a direction along the channel, and y is a direction that is perpendicular to the channel, as shown in Fig. 1(a), q is the electronic charge, ε_s is the permittivity of the silicon material, and n is carrier density in the channel. However, it is very challenging to solve 2-D Poisson's equation to get potential profile while developing a computationally efficient compact model. Therefore, to

simplify the 2-D Poisson's equation given in (1), we assume a parabolic potential in the y-direction [11] which is given as

$$V(y) = Ay^2 + B \tag{2}$$

where, the coefficients A and B are evaluated by applying potential boundary conditions in the y-direction of the channel. The procedure to obtain reduced form of Poisson's equation is given in [11]. Therefore, using (2) in (1), we will get the reduced form of the Poisson's equation along the channel (i.e., only in the x-direction) for NC-NSFET as given in

$$\frac{1}{\kappa}\frac{\partial^2\psi_C}{\partial^2 x} + \frac{V_{\rm gs} + V_{\rm fb} + V_{\rm FE} - \psi_C}{\zeta} = \frac{q}{\varepsilon_s}n(x) \tag{3}$$

where ψ_C is the center potential, $V_{\rm gs}$ is the applied gate voltage with respect to the source terminal, $V_{\rm fb}$ is the flat band voltage, $\kappa = 1 + \varepsilon_{\rm ins}T_{\rm NS}/4\varepsilon_s T_{\rm ins}$ is an intermediate parameter, $\varepsilon_{\rm ins}$ is a permittivity of the interfacial oxide layer, $T_{\rm NS}$ is a body thickness of the nanosheet, $T_{\rm ins}$ is the interfacial oxide thickness, $\zeta = \varepsilon_s T_{\rm ins}T_{\rm NS}\kappa/2\varepsilon_{\rm ins}$ is another intermediate parameter, and $V_{\rm FE}$ is voltage drop across the ferroelectric layer which can be expressed in terms of gate charge density (Q) using Landau-Devonshire theory [16] as,

$$V_{\rm FE} = \alpha_f Q + \beta_f Q^3 \tag{4}$$

where, $\alpha_f = 2aT_{\rm FE}$ and $\beta_f = 4bT_{\rm FE}$ are the Landau coefficients of the ferroelectric material. The values of a and b are listed in Table 1.

To get the charge density in the channel, we sum the carrier densities injected from the source side and the drain side [17] as

$$n(x) = n_{\rm s-d}(x) + n_{\rm d-s}(x) \tag{5}$$

where, $n_{\rm s-d}(x)$ is the carrier density at any position x in the channel, which is injected from the source side towards the drain side [11]. The source side injected carrier density ($n_{\rm s-d}(x)$) is calculated as the sum of carriers injected ballistically ($n_{\rm b-s}$) and through the drift-diffusive transport ($n_{\rm dd-s}$), which is given as

$$n_{\rm s-d}(x) = n_{\rm b-s}(x) + n_{\rm dd-s}(x) \tag{6}$$

Similarly, the carrier density injected from drain side is expressed as,

$$n_{\rm d-s}(x) = n_{\rm b-d}(x) + n_{\rm dd-d}(x) \tag{7}$$

where $n_{\rm b-d}$ is the ballistic carrier density injected from drain side and $n_{\rm dd-d}$ is the drift-diffusive carrier density injected from the drain side.

Now, we derive the expressions for $n_{\rm b-s/d}(x)$ and $n_{\rm dd-s/d}(x)$ in terms of S and λ from [17] as

$$n_{\rm b-s} = n_s(1-S)^{L/\lambda} \tag{8}$$

$$n_{\rm dd-s}(x) = n_s\frac{S}{1-S}\gamma^{x/\lambda} = n_{0s}\gamma^{x/\lambda} \tag{9}$$

$$n_{\rm b-d} = n_d(1-S)^{L/\lambda} \tag{10}$$

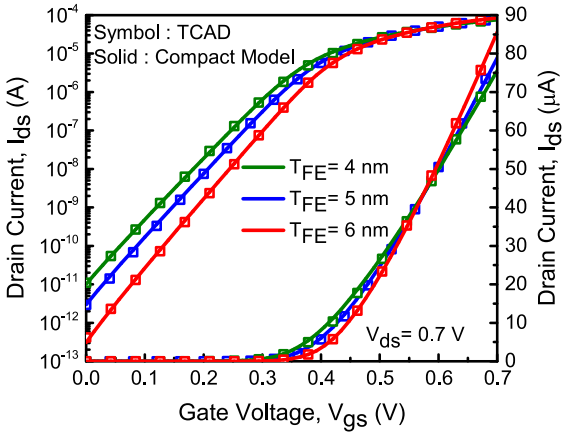

FIGURE 3. Validation of $I_{ds} - V_{gs}$ characteristics for different ferroelectric thickness (T_{FE}) at V_{ds} = 0.7V. NC-NSFET shows better SS and higher threshold voltage as we increase the T_{FE}.

$$n_{\rm dd-d}(x) = n_d\frac{S}{1-S}\gamma^{(L-x)/\lambda} = n_{0d}\gamma^{-x/\lambda} \tag{11}$$

where, $\gamma = 1 - S$ and S denotes the charge density getting scattered at every λ interval in the channel. Note that each charge density component is expressed in terms of n_s and n_d, the charge density available at source and drain end, respectively. The n_s and n_d are calculated from the core model of our previous double gate-NCFET model [18].

Now, to obtain the potential profile in the channel, we solve the reduced Poisson's equation (3) in conjugation with the current continuity as

$$\underbrace{n_{\rm b-s/d}v_b}_{Ballistic} + \underbrace{\mu n_{\rm dd-s/d}\frac{\partial\psi_C}{\partial x}}_{Drift} + \underbrace{\mu\phi_t\frac{\partial n_{\rm dd-s/d}}{\partial x}}_{Diffusion} = Const. \tag{12}$$

where v_b is the ballistic velocity of the carrier, μ is the mobility of the carrier in drift-diffusive transport, and ϕ_t is the thermal voltage.

After differentiating (12) with respect to x, we will get

$$\mu\frac{\partial n_{\rm dd-s/d}}{\partial x}\frac{\partial\psi_C}{\partial x} + \mu n_{\rm dd-s/d}\frac{\partial^2\psi_C}{\partial x^2} + \mu\phi_t\frac{\partial^2 n_{\rm dd-s/d}}{\partial x^2} = 0 \tag{13}$$

We have assumed continuity for each component, i.e., $n_{\rm s-d}(x)$ and $n_{\rm d-s}(x)$ separately to get potential profile due to injection from the carrier density from source to drain and drain to source, respectively.

Now, using (1), (6), and (13), we solve for the potential profile ψ_{C1} due to the injection of carriers from the source side.

$$\alpha\frac{\partial\psi_{C1}}{\partial x} + \frac{\partial^2\psi_{C1}}{\partial x^2} + \phi_t\alpha^2 = 0 \tag{14}$$

where, $\alpha = \ln(\gamma)/\lambda$ is an intermediate parameter, and ψ_{C1} is expressed as

$$\psi_{C1} = \frac{M_{1s}}{\kappa'} - \frac{N_{1s}\gamma^{3x/\lambda}}{3\alpha+\kappa'} - \frac{N_{2s}\gamma^{2x/\lambda}}{2\alpha+\kappa'} - \frac{N_{3s}\gamma^{x/\lambda}}{\alpha+\kappa'} + C_1 e^{-\kappa' x} \tag{15}$$

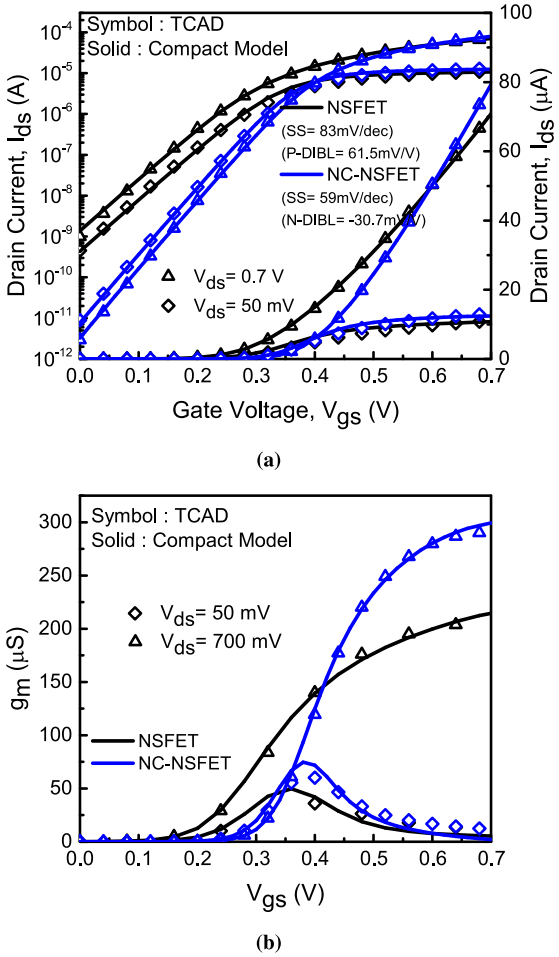

FIGURE 4. (a) Comparison and validation of $I_{ds} - V_{gs}$ of both NSFET and NC-NSFET (T_{FE} = 5nm) for both V_{ds} = 50mV and V_{ds} = 0.7V with the TCAD results. NC-NSFET exhibits N-DIBL, steep SS, and higher I_{ON} than NSFET. (b) Comparison and validation of g_m of both NSFET and NC-NSFET for both V_{ds} = 50mV and V_{ds} = 0.7V with the TCAD results. Due to NC effect, NC-NSFET shows higher g_m than NSFET.

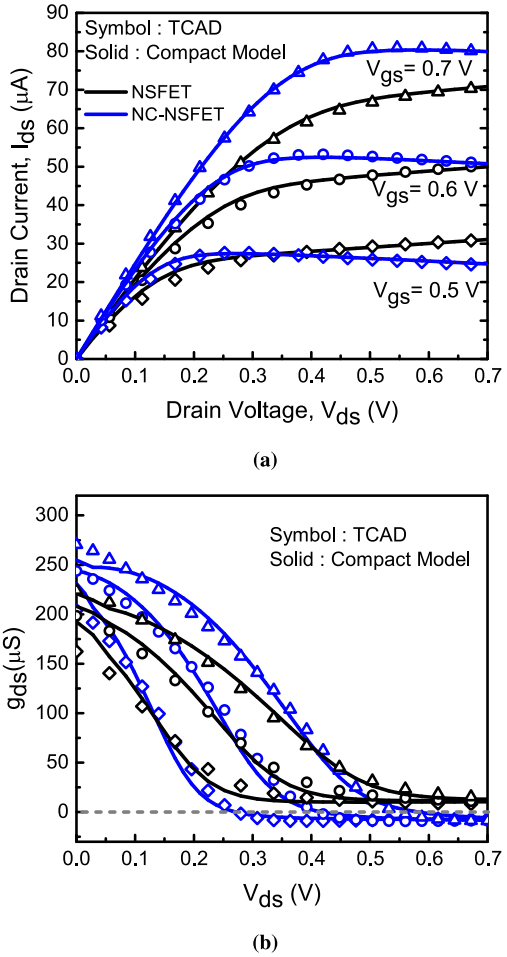

FIGURE 5. (a) Comparison and validation of $I_d - V_d$ of both NSFET and NC-NSFET at different V_{gs} with the TCAD results. NC-NSFET possesses NDR effect due to N-DIBL effect. (b) Validation of g_{ds} of both NSFET and NC-NSFET with the TCAD results. Due to NDR effect negative g_{ds} is observed in NC-NSFET.

where, C_1 is an integration constant and $\kappa' = \kappa/\alpha\zeta$ is another intermediate parameter and

$$M_{1s} = -\kappa'\left(V_{gs} - V_{fb}\right) + \frac{\kappa}{\alpha}\left(\frac{q}{\varepsilon_s} + \frac{\alpha_f}{\zeta}\right)n_{b-s} - \kappa'\beta_f(n_{b-s})^3 - \phi_t\alpha \quad (16)$$

$$N_{1s} = \kappa'\beta_f n_{0s}^3 \quad (17)$$

$$N_{2s} = 3\kappa'\beta_f n_{b-s}n_{0s}^2 \quad (18)$$

$$N_{3s} = n_{0s}\left(3\kappa'\beta_f n_{b-s}^2 + \frac{\kappa}{\alpha}\left(\frac{q}{\varepsilon_s} + \frac{\alpha_f}{\zeta}\right)\right) \quad (19)$$

Similarly, to get expression for potential profile (ψ_{C2}) due to the drain side charge injection, we solve (1), (7) and (13), simultaneously, as

$$\alpha\frac{\partial\psi_{C2}}{\partial x} + \frac{\partial^2\psi_{C2}}{\partial x^2} - \phi_t\alpha^2 = 0 \quad (20)$$

$$\psi_{C2} = -\frac{M_{1d}}{\kappa'} - \frac{N_{1d}\gamma^{-3x/\lambda}}{3\alpha+\kappa'} - \frac{N_{2d}\gamma^{-2x/\lambda}}{2\alpha+\kappa'} - \frac{N_{3d}\gamma^{-x/\lambda}}{\alpha+\kappa'} + C_2 e^{\kappa' x} \quad (21)$$

where C_2 is an integration constant and

$$M_{1d} = -\kappa'\left(V_{gs} - V_{fb}\right) + \frac{\kappa}{\alpha}\left(\frac{q}{\varepsilon_s} + \frac{\alpha_f}{\zeta}\right)n_{b-d} - \kappa'\beta_f(n_{b-d})^3 + \phi_t\alpha \quad (22)$$

$$N_{1d} = \kappa'\beta_f n_{0d}^3 \quad (23)$$

$$N_{2d} = 3\kappa'\beta_f n_{b-d}n_{0d}^2 \quad (24)$$

$$N_{3d} = n_{0d}\left(3\kappa'\beta_f n_{b-d}^2 + \frac{\kappa}{\alpha}\left(\frac{q}{\varepsilon_s} + \frac{\alpha_f}{\zeta}\right)\right) \quad (25)$$

The final center potential profile ψ_C is obtained through the superposition of ψ_{C1} and ψ_{C2} as given by

$$\psi_C = \psi_{C1} + \psi_{C2} \quad (26)$$

Now, using the boundary conditions along the y -direction, we get the surface potential (ψ) in terms of ψ_C and applied gate bias (V_{gs}) which is expressed as

$$\psi = \frac{\psi_C + (\kappa - 1)\left(V_{gs} - V_{fb} - \alpha_f n(x) - \beta_f n(x)^3\right)}{\kappa} \quad (27)$$

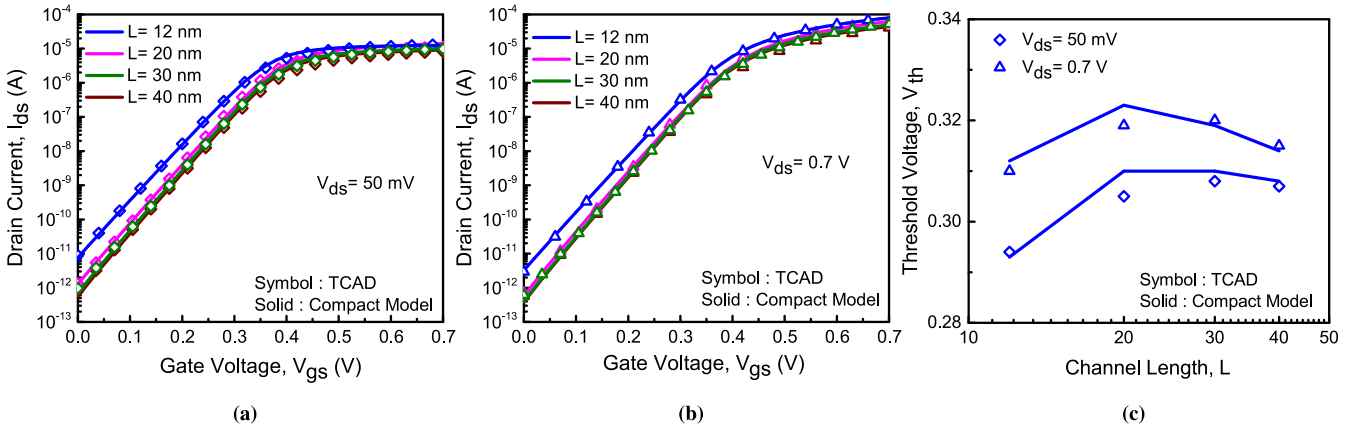

FIGURE 6. **(a) Validation of $I_{ds} - V_{gs}$ of NC-NSFET for different channel lengths at $V_{ds} = 50$mV with the TCAD results. SS and V_t- roll up effect is captured using single set of parameters. (b) Validation of $I_{ds} - V_{gs}$ of NC-NSFET for different channel lengths at $V_{ds} = 0.7$V with the TCAD results. N-DIBL is captured using single set of parameters. (c) Validation of threshold voltage shift for different channel lengths at $V_{ds} = 50$mV and $V_{ds} = 0.7$V. The V_t-roll up and N-DIBL effect are clearly observed in NC-NSFET.**

The C_1 and C_2 are the integration constants which are solved using the boundary conditions, i.e., $\psi(x = 0) = 0$ and $\psi(x = L) = V_{ds}$.

B. DRAIN CURRENT

Now, to obtain the total current, we sum the current due to the ballistic transport(I_b) and current caused by drift-diffusive transport(I_{dd}) which can be written as

$$I_{total} = I_b + I_{dd} \tag{28}$$

The ballistic current (I_b) can be expressed as given in [11]

$$I_b = qT_{NS}W_{NS}\left(n_{b-s}v_{b(x=0)} - n_{b-d}v_{b(x=L)}\right)\left[\frac{1 - e^{P\frac{V_{ds}}{\phi_t}}}{1 + e^{-P\frac{V_{ds}}{\phi_t}}}\right] \tag{29}$$

where, W_{NS} is the nanosheet width, P is parameter, and $v_{b(x)}$ is ballistic velocity of the carrier which is given in [11] as

$$v_b(x) = \sqrt{\frac{q\phi_t + 2q\psi(x)}{m_{eff}}} \tag{30}$$

where m_{eff} is the effective mass of the carrier.

The drift-diffusive current in terms of surface potential and effective drift-diffusive carrier density ($n_{dd,eff}(x)$) is given by

$$I_{dd} = \frac{q\mu_{eff}T_{NS}W}{L}\int_0^L n_{dd,eff}(x)\frac{d\psi(x)}{dx}dx \tag{31}$$

where, $n_{dd,eff}(x) = n_{dd-s}(x) - n_{dd-d}(x)$.

Now, the short channel effects (SCE) arising due to the fringing electric field in NCFET such as negative DIBL (N-DIBL), V_t-roll up and the sub-threshold slope improvement with a reduction in channel length [8]–[10] are captured using the capacitive network approach which we earlier developed for the double gate NCFET [8]. The model for confinement effect is essential for the sub-7nm technology node which we have incorporated in our compact model using same set of equations which are available in BSIM-CMG code [19].

Next, we have validated the obtained drain current from our model with the TCAD data. We have validated our model for different ferroelectric thicknesses (T_{FE}) as shown in Fig. 3. The model accurately captures the drain current characteristics. With increase in the T_{FE}, negative capacitance effect improves sub-threshold slope (SS) and the ON current I_{ON} due to the better capacitance matching effect. However, we observe a hysteresis in I_{ds}-V_{gs} characteristics for $T_{FE} > 6$ nm (not shown in Fig. 3).

Next, we have validated the I_{ds}-V_{gs} characteristics obtained for both NC-NSFET ($T_{FE} = 5$nm) and NSFET at $V_{ds} = 50$ mV and $V_{ds} = 0.7$ V as shown in Fig. 4(a). In contrast to the baseline NSFET, NC-NSFET exhibits steep sub-threshold slope (SS), high ON current, and N-DIBL, which can be clearly observed in Fig. 4(a). The I_{ds}-V_{gs} calculated from the proposed compact model agrees well with the TCAD data as shown in Fig. 4(a). The model is further validated with the derivative of the drain current (g_m) as shown in Fig. 4(b)).

In Fig. 5(a), we compare and validate the I_{ds}-V_{ds} characteristics for both NSFET and NC-NSFET. Due to the N -DIBL effect, the Negative differential resistance (NDR) effect is observed in the TCAD data and is very well captured by our model for the NC-NSFET. Further, the model is validated with the derivative of the I_{ds}-V_{ds} characteristics (g_{ds}), where the negative g_{ds} is captured in the NDR region for NC-NSFET in Fig. 5(b).

The I_{ds}-V_{gs} characteristics for different channel lengths for NC-NSFET at $V_{ds} = 50$ mV are shown in Fig. 6(a). Drain current for different channel lengths are accurately captured by our model with a single global set of parameters. The increase in threshold voltage with a decrease in channel length (V_t - roll up effect) can be observed from $L = 40$ nm to L = 30nm in Fig. 6(c). However, the conventional SCEs start to dominate at very short channel lengths [8]. We have modeled these conventional SCEs using the same set

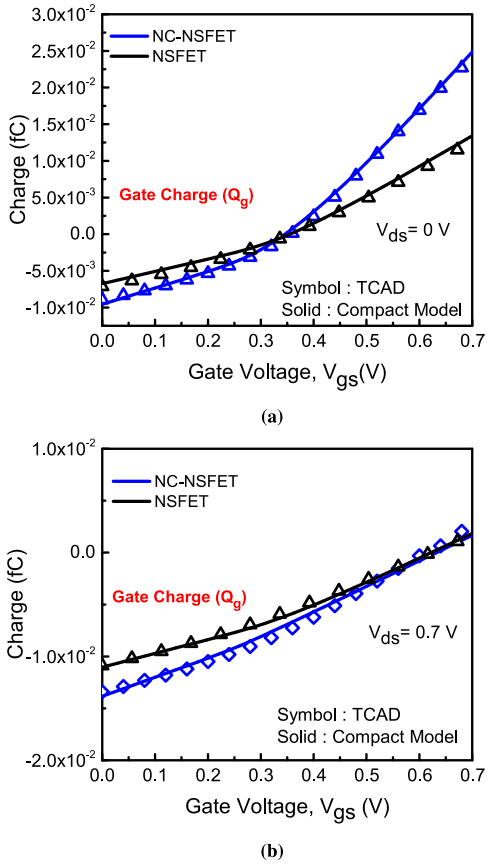

FIGURE 7. **(a) Comparison and validation of gate terminal charge Q_G for both NSFET and NC-NSFET (T_{FE} = 5nm) at V_{ds} = 0V. The amplification effect in NC-NSFET on fringing charges and channel charge density leads to more negative and more positive Q_G at low V_{gs} and high V_{gs} regime, respectively. (b) Comparison and validation of gate terminal charge Q_G for both NSFET and NC-NSFET (T_{FE} = 5nm) at V_{ds} = 0.7V. The dominance of fringing charge near drain end due to the high drain for all V_{gs} regime and amplification effect over the fringing charge in NC-NSFET leads to more negative Q_G than the NSFET.**

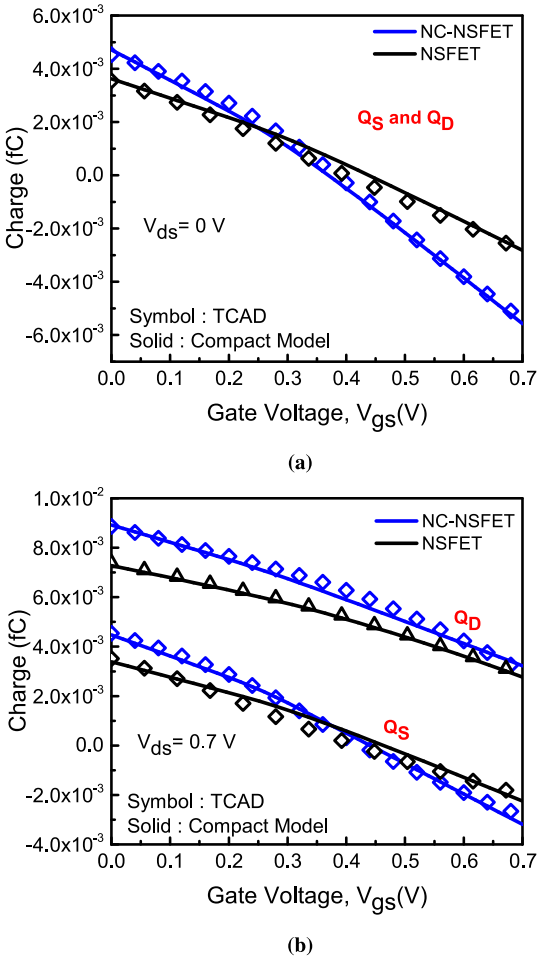

FIGURE 8. **(a) Comparison and validation of gate terminal charge Q_S and Q_D for both NSFET and NC-NSFET (T_{FE} = 5nm) at V_{ds} = 0V. The amplification effect in NC-NSFET on fringing charges and channel charge density leads to more positive and more negative Q_S/Q_D at low V_{gs} and high V_{gs} regime, respectively. (b) Comparison and validation of gate terminal charge Q_S and Q_D for both NSFET and NC-NSFET (T_{FE} = 5nm) at V_{ds} = 0.7V. The dominance of fringing charge near drain end due to the high drain for all V_{gs} regime and amplification effect over the fringing charge in NC-NSFET leads to more positive Q_D than the NSFET. However, the behaviour for Q_S is same as the earlier case, since the source terminal is still at zero potential.**

equations which are available in the BSIM-CMG [19] model. Further, I_d-V_g characteristics for different L at $V_{\rm ds} = 0.7$ V is shown in Fig. 6(b). The threshold voltage dependent on the drain voltage (N-DIBL) is also captured through a single set of parameters as shown in Fig. 6(c).

C. TERMINAL CHARGES

The gate terminal charge (Q_G) is obtained by integrating the carriers present ($n(x)$) in the channel over the channel length (L) as

$$Q_G = qW \int_0^L n(x)dx \tag{32}$$

where, $W = 2 \times (W_{\rm NS} + T_{\rm NS})$ and $n(x) = n_{\rm s-d}(x) + n_{\rm d-s}(x)$. After solving integration, we get the Q_G as

$$Q_G = qW\left(n_{0\rm s}\left(\frac{\gamma^{L/\lambda}}{\alpha} - \frac{1}{\alpha}\right) + n_{\rm b-s}L - n_{0\rm d}\left(\frac{\gamma^{-L/\lambda}}{\alpha} - \frac{1}{\alpha}\right) + n_{\rm b-d}L\right) \tag{33}$$

The drain terminal charge density (Q_D) can be obtained from the carrier density injected from the drain side into the channel. The expression for Q_D is written as

$$Q_D = -qW \int_0^L n_{d-s}(x)dx \tag{34}$$

After solving above equation, we get

$$Q_D = -qW\left(n_{\rm b-d}L - n_{0\rm d}\left(\frac{\gamma^{-L/\lambda}}{\alpha} - \frac{1}{\alpha}\right)\right) \tag{35}$$

Similarly, the source terminal charge density is obtained from the carrier density injected from the source into the channel. The expression for Q_S is written as

$$Q_S = -qW \int_0^L n_{s-d}(x)dx \tag{36}$$

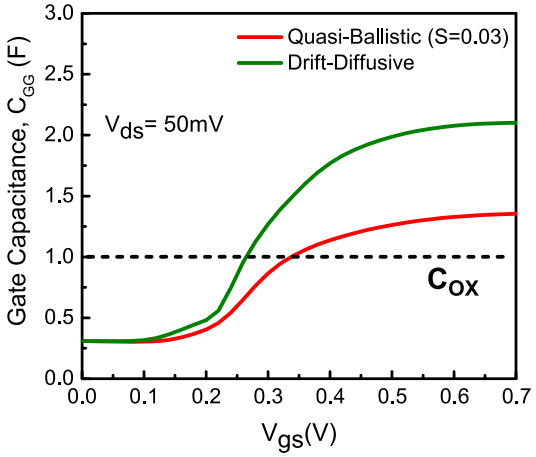

FIGURE 9. Gate capacitance (C_{GG}) of the NC-NSFET for drift-diffusive and quasi-ballistic transport case. The matching effect becomes poor for quasi-ballistic case.

After solving above equation, we get

$$Q_S = -qW\left(n_{b-s}L + n_{0s}\left(\frac{\gamma^{L/\lambda}}{\alpha} - \frac{1}{\alpha}\right)\right) \tag{37}$$

The fringing charge plays an important role in advanced technology node devices. Therefore, we need to model this accurately at such advanced technology node. To obtain these fringing charges, we use the capacitive network approach [8]. We have validated the terminal charges with the TCAD results as shown in Fig. 7 and Fig. 8. In Fig. 7(a), the model for Q_G is validated with TCAD result at $V_{ds} = 0$V for both NSFET and NC-NSFET. The higher Q_G is observed at high V_{gs} in NC-NSFET due to the NC effect as compared to the baseline NSFET. However, the fringing charge is dominant in NC-NSFET at low V_{gs} regime, due to the amplification effect as compared to the baseline NSFET as shown in Fig. 7(a). In Fig. 7(b), we have validated the Q_G at $V_{ds} = 0.7$V. At high $V_{ds} = 0.7$V, the fringing charge significantly dominates near at drain side due to high drain bias and therefore, more negative gate charge is observed in NC-NSFET compared to NSFET for all V_{gs} regime.

Next, we have validated the source and drain terminal charges as shown in Fig. 8. Fig. 8(a) shows the validation of Q_S and Q_D for both NSFET and NC-NSFET at $V_{ds} =$ 0V. From the capacitive network [8], we have modeled the fringing charge for source terminal as

$$Q_{sfr} = C_{fc}(V_{bi} - \psi_C) + C_{fs}(V_{bi} - \psi_S) \tag{38}$$

Similarly, the fringing charge for drain terminal is given by

$$Q_{dfr} = C_{fc}(V_{bi} + V_{ds} - \psi_C) + C_{fs}(V_{bi} + V_{ds} - \psi_S) \tag{39}$$

To obtain total source and drain terminal charge, we add (38) to (37) and (39) to (35), respectively. The source and drain terminals contribute the same charges, since both terminals are at the same potential. At $V_{ds} = 0$V, the amplification on fringing charge in the sub-threshold regime increases the Q_S and Q_D in NC-NSFET than the NSFET. Similarly, the

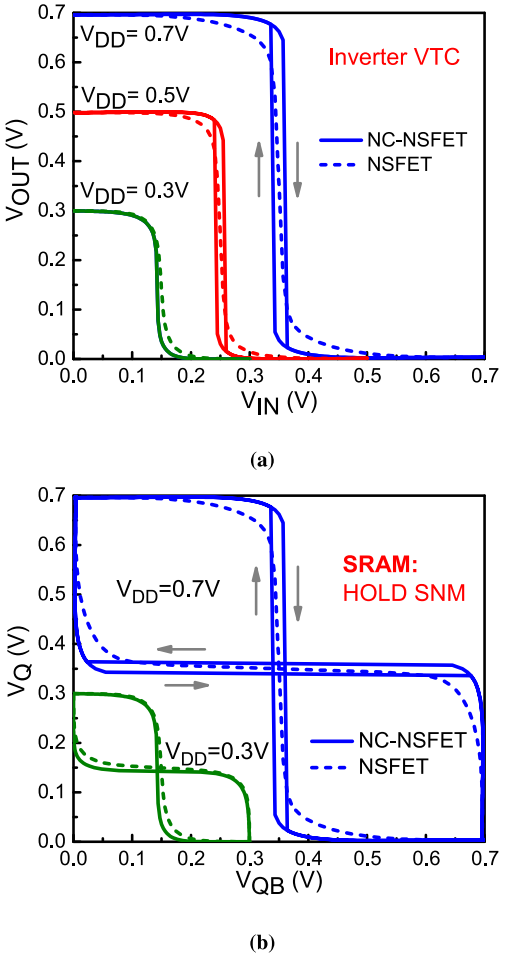

FIGURE 10. (a) CMOS Inverter VTC for both NSFET and NC-NSFET (forward and reverse sweep) case for different V_{DD} obtained from the compact model. The hysteresis width of the VTC reduces for lower V_{DD}. (b) Hold SNM butterfly curve for 6T-SRAM cell $V_{DD} = 0.7$V and $V_{DD} = 0.3$V obtained from the compact model. The hold SNM is better for NC-NSFET for both V_{DD} cases.

amplification effect on the channel charge density in NC-NSFET contributes more charges in the channel than the NSFET. Fig. 8(b) shows the validation of Q_S and Q_D at $V_{ds} = 0.7$V. the similar behaviour for Q_S is observed, since the source terminal is still at zero potential. However, due to the high drain bias, the fringing contributes to the channel for all V_{gs} regime and the amplification on fringing charges near the drain side leads to more contribution of drain terminal charges compared to the baseline NSFET.

Fig. 9 shows the gate capacitance (C_{GG}) for drift diffusive and quasi-ballistic transport cases at source side. The channel charge density is higher in the case of drift-diffusive transport compared to the quasi-ballistic transport, since to carry same amount of current quasi-ballistic transport requires less amount of charges at same bias condition [11]. Therefore, the gate capacitance in quasi-ballistic case is lower than the drift-diffusive case which worsens the capacitance matching and in turn reduces the voltage amplification effect of the NC.

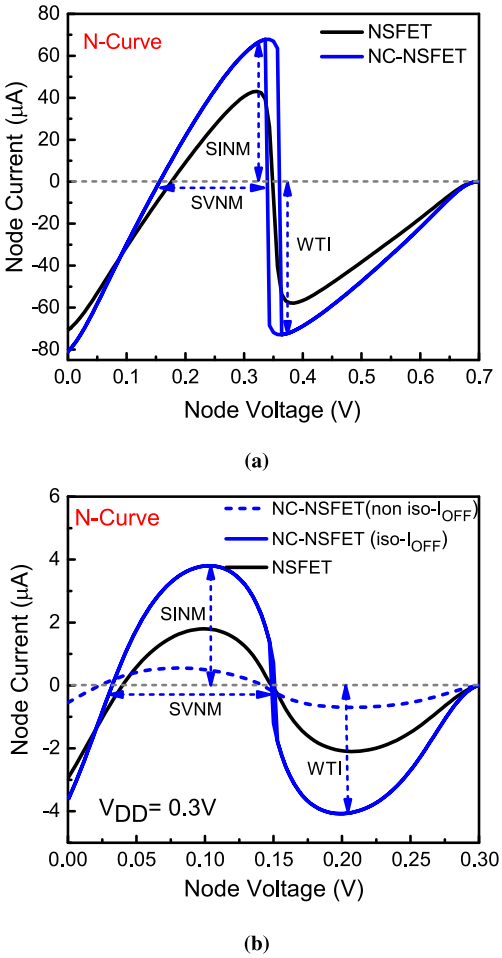

FIGURE 11. **(a) Noise curve for NSFET and NC-NSFET obtained from the compact model to determine read stability and write ability of SRAM cell at $V_{DD} = 0.7$ V, which is better in case of NC-NSFET. (b) Noise curve to determine the read stability and write ability of SRAM cell at $V_{DD} = 0.3$ V obtained from the compact model. The read stability and write ability are improved in iso-I_{OFF} case of NC-NSFET.**

IV. CMOS INVERTER AND 6-T SRAM CIRCUIT SIMULATIONS

The model is implemented in Verilog-A and is used to simulate circuits in the SPICE simulator. The voltage transfer characteristics (VTC) of the inverter for different V_{DD} for both NSFET and NC-NSFET, are shown in Fig. 10(a). Due to the negative differential resistance (NDR) present in I_{ds}-V_{ds} characteristics (see Fig. 5(a)), a hysteresis is observed in the inverter VTC of NC-NSFET [20] for forward and reverse sweeps. The steep inverter VTC of NC-NSFET also result in improved noise margins for forward and reverse sweeps. The hysteresis width of inverter VTC of NC-NSFET decreases as V_{DD} is reduced as shown in Fig. 10(a) and gets completely diminished for $V_{DD} = 0.3$ V. Further, the improved noise margins of the NC-NSFET based CMOS inverter reflect in 6-T SRAM operations too due to the back to back connected inverters. The hold static noise margin (SNM) of SRAM cell for both NSFET and NC-NSFET are compared for $V_{DD} = 0.3$ V and $V_{DD} = 0.7$ V in Fig. 10(b). The butterfly curve shows NC-NSFET based SRAM has a higher HOLD SNM in both forward and reverse sweep than the NSFET case.

Fig. 11 show noise-curve (n-curve) to determine SRAM cell stability (read stability and write ability), which provides both current and voltage information for read and write operations. Fig. 11(a) shows n-curve for $V_{DD} = 0.7$ V. The node current shows hysteresis due to the NDR effect. The static voltage noise margin (SVNM) of NC-NSFET is better in forward as well as in reverse sweep than the NSFET case. Further, the maximum current conducted by the cell before flipping its state, i.e., static current noise margin (SINM) is larger in the case of NC-NSFET. Therefore, read stability in case of the NC-NSFET is improved. Further, the improved maximum negative current, i.e., write trip current (WTI) for NC-NSFET shows a better write ability of the cell. Fig. 11(b) shows n-curve for $V_{DD} = 0.3$ V where the node current in NC-NSFET case is lower than the NSFET case which is due to a lower drain current of NC-NSFET than the NSFET in this case (see Fig. 4(a)). This degrades the read stability of NC-NSFET compared with the NSFET as shown by dotted line. However, if the OFF currents of NC-NSFET and NSFET are matched by work function tuning (iso-I_{OFF} case), the NC-NSFET exhibits a higher drain current which improves the read stability than the NSFET case at $V_{DD} = 0.3$ V.

V. CONCLUSION

We have developed a compact model for NC-NSFET including quasi ballistic transport for sub-7nm technology node using the L-K model of ferroelectric material. We have demonstrated that the quasi-ballistic transport can reduce the voltage amplification effect in very short channel NCFETs. Further, we have modeled the terminal charges for NC-NSFET. Finally, we have implemented our model in Verilog-A to simulate inverter and SRAM circuits and compared their static noise margin in conventional SPICE simulator.

REFERENCES

[1] Y. M. Lee *et al.*, "Accurate performance evaluation for the horizontal nanosheet standard-cell design space beyond 7nm technology," in *Proc. IEEE Int. Electron Devices Meeting (IEDM)*, San Francisco, CA, USA, 2017, pp. 1–4.

[2] S. Kim, M. Guillorn, I. Lauer, P. Oldiges, T. Hook, and M. Na, "Performance trade-offs in FinFet and gate-all-around device architectures for 7nm-node and beyond," in *Proc. IEEE SOI-3D-Subthreshold Microelectron. Technol. Unified Conf. (S3S)*, Rohnert Park, CA, USA, 2015, pp. 1–3.

[3] N. Loubet *et al.*, "Stacked nanosheet gate-all-around transistor to enable scaling beyond finfet," in *Proc. Symp. VLSI Technol.*, Kyoto, Japan, 2017, pp. T230–T231.

[4] S. Salahuddin and S. Datta, "Use of negative capacitance to provide voltage amplification for low power nanoscale devices," *Nano Lett.*, vol. 8, no. 2, pp. 405–410, 2008, doi: 10.1021/nl071804g.

[5] K. S. Li *et al.*, "Sub-60mv-swing negative-capacitance FinFet without hysteresis," in *Proc. IEEE Int. Electron Devices Meeting (IEDM)*, Washington, DC, USA, Dec. 2015, pp. 1–4, doi: 10.1109/IEDM.2015.7409760.

[6] J. Zhou *et al.*, "Ferroelectric HfZrOx Ge and GeSn PMOSFETs with Sub-60 mV/decade subthreshold swing, negligible hysteresis, and improved Ids," in *Proc. IEEE Int. Electron Devices Meeting (IEDM)*, San Francisco, CA, USA, Dec. 2016, pp. 1–4, doi: 10.1109/IEDM.2016.7838401.

[7] Z. Krivokapic *et al.*, "14nm ferroelectric FinFET technology with steep subthreshold slope for ultra low power applications," in *Proc. IEEE Int. Electron Devices Meeting (IEDM)*, San Francisco, CA, USA, Dec. 2017, pp. 1–4, doi: 10.1109/IEDM.2017.8268393.

[8] A. D. Gaidhane, G. Pahwa, A. Verma, and Y. S. Chauhan, "Modeling of inner fringing charges and short channel effects in negative capacitance MFIS transistor," in *Proc. IEEE Electron Devices Technol. Manuf. Conf. (EDTM)*, Singapore, 2019, pp. 282–284.

[9] G. Pahwa, A. Agarwal, and Y. S. Chauhan, "Numerical investigation of short-channel effects in negative capacitance MFIS and MFMIS transistors: Subthreshold behavior," *IEEE Trans. Electron Devices*, vol. 65, no. 11, pp. 5130–5136, Nov. 2018.

[10] G. Pahwa, A. Agarwal, and Y. S. Chauhan, "Numerical investigation of short-channel effects in negative capacitance MFIS and MFMIS transistors: Above-threshold behavior," *IEEE Trans. Electron Devices*, vol. 66, no. 3, pp. 1591–1598, Mar. 2019.

[11] A. Dasgupta, A. Agarwal, S. Khandelwal, and Y. S. Chauhan, "Compact modeling of surface potential, charge, and current in nanoscale transistors under quasi-ballistic regime," *IEEE Trans. Electron Devices*, vol. 63, no. 11, pp. 4151–4159, Nov. 2016.

[12] A. D. Gaidhane, G. Pahwa, A. Dasgupta, A. Verma, and Y. S. Chauhan, "Compact modeling of negative capacitance nanosheet FET including quasi-ballistic transport," in *Proc. 4th IEEE Electron Devices Technol. Manuf. Conf. (EDTM)*, Penang, Malaysia, 2020, pp. 1–4.

[13] *Sentaurus Device User Guide,Version O-2018.06*, Synopsys, Mountain View, CA,USA, 2018.

[14] M. Hoffmann *et al.*, "Direct observation of negative capacitance in polycrystalline ferroelectric HfO_2," *Adv. Funct. Mater.*, vol. 26, no. 47, pp. 8643–8649, 2016.

[15] P. Marton, I. Rychetsky, and J. Hlinka, "Domain walls of ferroelectric $BaTiO_3$ within the Ginzburg–Landau–Devonshire phenomenological model," *Phys. Rev. B*, vol. 81, Apr. 2010, Art. no. 144125. [Online]. Available: https://link.aps.org/doi/10.1103/PhysRevB.81.144125

[16] A. Devonshire, "XCVI. Theory of barium titanate," *London Edinburgh Dublin Philos. Mag. J. Sci.*, vol. 40, no. 309, pp. 1040–1063, 1949, doi: 10.1080/14786444908561372.

[17] A. Dasgupta, A. Agarwal, and Y. S. Chauhan, "An improved model for quasi-ballistic transport in MOSFETs," *IEEE Trans. Electron Devices*, vol. 64, no. 7, pp. 3032–3036, Jul. 2017.

[18] A. D. Gaidhane, G. Pahwa, A. Verma, and Y. S. Chauhan, "Compact modeling of drain current in double gate negative capacitance mfis transistor," in *Proc. 4th IEEE Int. Conf. Emerg. Electron. (ICEE)*, Bengaluru, India, 2018, pp. 1–5.

[19] Y. S. Chauhan *et al.*, *FinFET Modeling for IC Simulation and Design: Using the BSIM-CMG Standard*. Amsterdam, The Netherlands: Academic, 2015.

[20] T. Dutta, G. Pahwa, A. R. Trivedi, S. Sinha, A. Agarwal, and Y. S. Chauhan, "Performance evaluation of 7-nm node negative capacitance FinFET-based SRAM," *IEEE Electron Device Lett.*, vol. 38, no. 8, pp. 1161–1164, Aug. 2017, doi: 10.1109/LED.2017.2712365.