Compact silicon-micromachined wideband 220 – 330 GHz turnstile orthomode transducer

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***Abstract*—This paper reports on a turnstile-junction orthomode transducer (OMT) implemented by silicon micromachining in the 220 – 330 GHz band. Turnstile OMTs are very wideband and allow for co-planar ports, but require accurate and complex geometries which makes their fabrication challenging at higher frequencies. The compact 10 mm x 10 mm x 0.9 mm OMT-chip presented in this paper is the first micromachined full-band OMT in any frequency range, and only the second turnstile OMT implemented above 110 GHz. The measured insertion loss (0.3 dB average, 0.6 dB worst-case) and the cross-polarization (60 dB average, 30 dB worst-case) over the whole waveguide band represent the best performance of any wideband OMT, regardless of design or fabrication technology, in the 220 – 330 GHz band. The return loss with 22 dB average (16 dB worst-case) is comparable or better than previous work. The paper discusses design considerations and compromises of this complex 9 layer silicon micromachined device, including the influence of sidewall slopes, underetching, and post-bonding misalignment between the chips. It is shown that for a device which is very sensitive to geometrical variations, such as a turnstile OMT, it is necessary to anticipate and compensate for any fabrication imperfections in the design to achieve high RF performance.**

***Index Terms*—OMT, orthomode transducer, turnstile, silicon micromachining, DRIE, MEMS, millimeter wave, mmW, terahertz, THz**

I. Introduction

THERE is an increasing interest in millimeter-wave (mmW) receivers for remote sensing in earth and space observation missions [1]. These receivers require orthomode transducers (OMTs) to discriminate between the two orthogonal polarizations present in the receiving antenna. At mmW frequencies fabrication of OMTs becomes challenging due to their complex geometries and small waveguide dimensions.

The Bøifot [2] and turnstile junction [3] are the most commonly used OMT designs, due to their twofold symmetrical geometry that allows broadband operation up to a theoretical 60% fractional bandwidth (FBW) [4]. This is achieved by avoiding the excitation of higher order TE_{11} and TM_{11} modes in the common square waveguide port. However, the twofold symmetry increases the fabrication complexity of the required recombination networks.

An approach to simplify the fabrication of OMTs for the mmW frequency range is to use onefold symmetrical geometries which allows for simpler split block fabrication at the cost of a reduced operational bandwidth [5]–[7]. Reck and Chattopadhyay [6] have used high precision CNC-milling to implement an asymmetrical side-arm OMT working from 500 – 600 GHz. Although they achieved good RF performance, it was difficult to achieve good isolation levels due to the misalignment between the metal blocks. Recently, the same authors have used silicon micromachining to implement a similar OMT geometry with improved fabrication accuracy compared to the CNC milled version [7]. Silicon micromachining has the advantages of very accurate features and batch (high-volume) manufacturing capability, but it also suffers from design geometry limitations in the out-of-plane-direction. The micromachined device achieved superior RF performance in terms of insertion loss and cross polarization.

However, many applications require full waveguide-band operation (40% FBW), requiring the use of the more complex twofold symmetrical OMT concepts. Bøifot OMTs have been broadly used at frequencies above 100 GHz since they only require a single recombination network, in contrast to the more complex turnstile OMTs. Therefore, Bøifot OMTs have been fabricated in a split-block configuration by high-precision machining for broadband applications, as shown by different publications in the 125 to 500 GHz frequency bands [8]–[11].

Wollack and Grammer [8] implemented a classical Bøifot OMT in a split-block configuration by electric-discharge-machining, manufacturing the septum as a separate piece patterned by photolithography, with the shorting posts made of copper-stainless steel wire. The OMT in [9] was also fabricated in a split-block configuration by CNC-milling, implementing the septum with a separately machined copper sheet, and replacing the shorting pins with a stepped impedance transformer. Alternatively, Navarrini *et al.* [10] and Asayama and Kamikura [11] avoided the use of a septum by using reverse-coupling and double-ridged architectures respectively, which, however, limited the operation bandwidth to 30% FBW. While these four works [8]–[11] reported excellent RF performance at very high frequency (up to 500 GHz), the fabrication and delicate assembly of such high-precision machined parts is very challenging and expensive. The resulting components were heavy and bulky solid metal blocks with the need of thin septums for full band performance.

Turnstile OMTs are characterized by a more complex architecture, since a recombination network is needed for each polarization. A well-known approach for the fabrication of such an OMT is to divide it into four split-blocks which intersect along the common waveguide port axis [3]. The only implementation of a turnstile OMT above 110 GHz was reported for the 200 – 270 GHz frequency band [12]. Five iden-

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tical OMTs were manufactured in a four-block configuration using different metals and different machining techniques, and even though some of the OMTs showed good performance, several alignment and gap issues were described in the paper that required manual filling of the metal gaps to achieve the reported performance.

Some alternative techniques for the implementation of turnstile OMTs have also been developed, using electroforming or wire erosion, but have only been used at lower frequencies, i.e. in the W-band [13], [14]. Virone *et al.* [14] divided the OMT geometry in several layers, with simple 2D geometries on each layer defined by wire erosion on metal plates. These plates were stacked, resulting in a very compact design, with high performance, and with the possibility of batch fabrication and integration. However, this manufacturing technique would be difficult to scale down for higher frequencies due to the thin metal sheets required.

The turnstile OMT presented in this paper is designed for full-band operation in the WM864 band, 220 – 330 GHz, and is, to the best of our knowledge, the first broadband OMT implemented by micromachining, and only the second attempt (besides [12]) to implement a turnstile OMT at frequencies above 110 GHz. Preliminary return loss measurement results with open-ended and shorted common-port configurations, for validating the fabrication approach, were shown in [15]. In the present paper, full characterization results including insertion loss, return loss for both polarizations, and the cross-polarization levels are presented for the first time. The paper discusses design decisions and limitations of the micromachined implementation of the turnstile OMT. Furthermore, the paper investigates the influence of predictable fabrication imperfections by micromachining, which were compensated when optimizing the design. Finally, an alignment-error analysis on the cross polarization is carried out, based on the measured chip-to-chip alignment errors of two fabricated prototype devices.

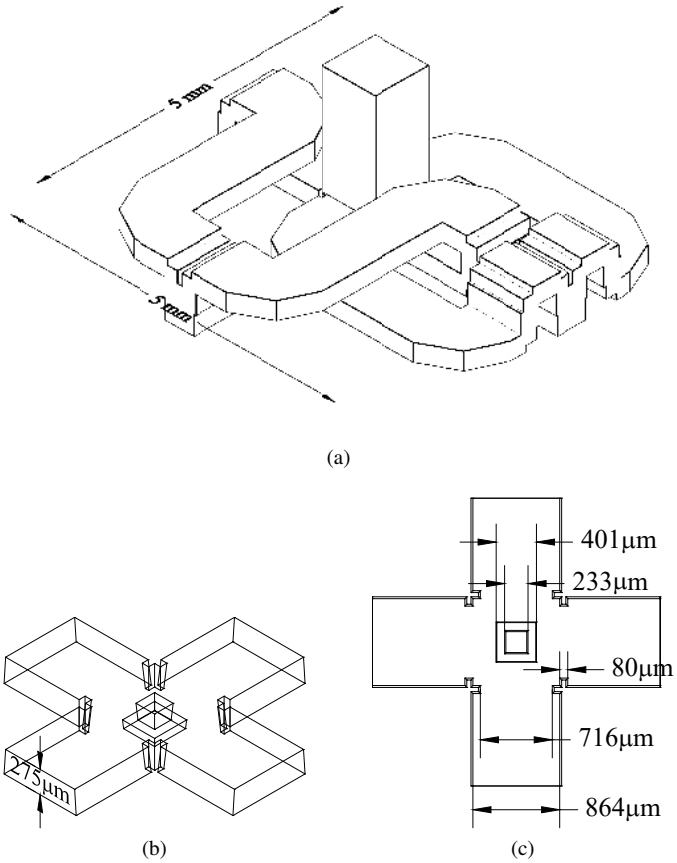


Fig. 1. 3D drawings of the micromachined turnstile OMT implementation: (a) complete OMT design, (b) perspective view of turnstile junction, and (c) top view of turnstile junction including all design parameters. The design model considers the predicted side-wall slopes and underetching characteristic for deep-silicon etching.

II. Design

The design of turnstile orthomode transducers has been extensively discussed in the literature [3], [16]. Therefore, this section focuses on the design considerations of such components at mmW frequencies for implementation by silicon micromachining, i.e. the design decisions taken to achieve optimum performance for a reasonable fabrication complexity.

A three silicon-on-insulator (SOI) chip stack with three individually-etched silicon sub-layers is chosen to implement the OMT, as shown in Fig. 1 and Fig. 2. This 9-layer structure was found to be the minimum complexity for implementing the multiple recombination networks with high RF performance. This fabrication complexity is acceptable since only three silicon etch steps per wafer are required. These sub-layers are of different thicknesses, as shown in Fig. 2, but the sub-components of the device have been designed and optimized so that the individual layers of each chip have the same thickness for all three chips, which allows one to use an identical fabrication procedure for all three wafers or even to co-fabricate all chips on the same wafer. A further design constraint considered was the in-plane waveguide height of 275 µm as compared to a full-height waveguide of 432 µm, which is determined by the handle layer thickness of the SOI wafer, and which was chosen as a compromise between waveguide performance and etching performance. This also implies that the scatterer post was limited to a maximum height of 275 µm. Except for minimum feature sizes, there are no design constraints for the in-plane geometries.

Fig. 2 shows how each polarization is re-routed either in Chip 1 or in Chip 3, while Chip 2 is used to implement the impedance transformers for the E-plane power combiners and the out-of-plane bends and acts as a separation between the waveguide channels in Chip 1 and Chip 3. An exploded view of the three-chip stack is shown in Fig. 3.

As a first design step, CST Microwave Studio was used for the design of the individual sub-components of the OMT. As optimization criteria, a target return loss of 25 dB for the whole band was set for all sub-components to prevent reflections when cascading the components in the full device.

The turnstile junction was designed as an 864 µm x 864 µm square waveguide with four 275 µm x 864 µm reduced-height waveguide ports, and a two-step square scatterer post in the centre, as shown in Fig. 1 (b). The post acts as a tuning stub

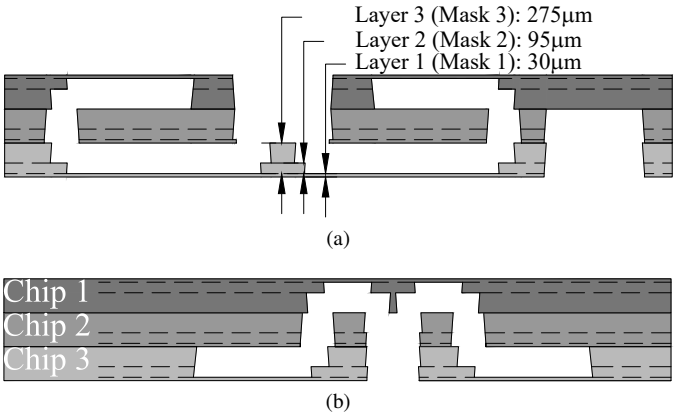


Fig. 2. Cross section views of (a) the turnstile junction and E-plane bends, and (b) E-plane power combiner. The design model considers the predicted side-wall slopes characteristic for deep-silicon etching.

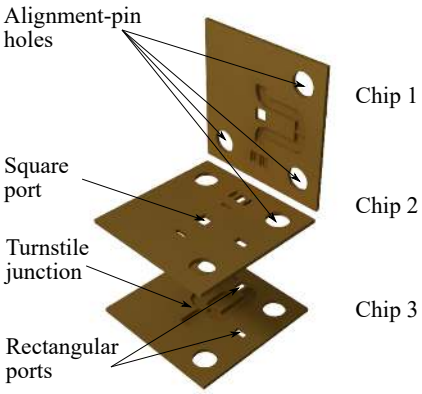


Fig. 3. Exploded view of the three-chip stack forming the OMT component.

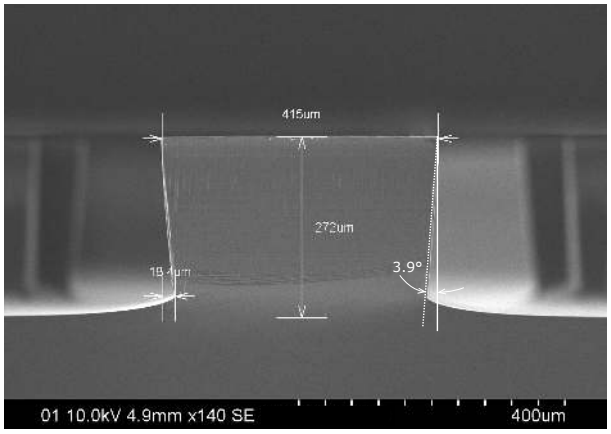


Fig. 4. Cross-section SEM picture of the turnstile post, after the first etch in a test wafer, showing a 3.9° sidewall angle.

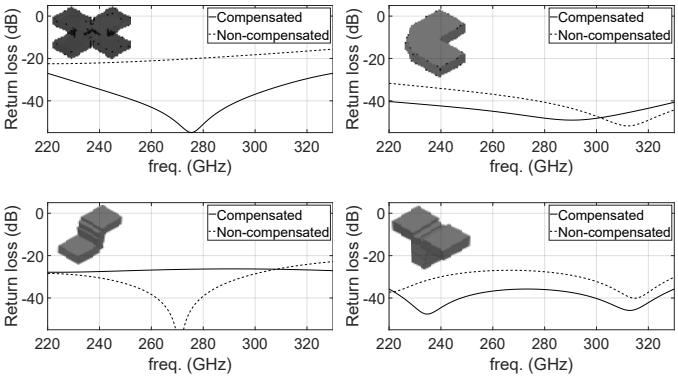


Fig. 5. Simulated return loss of (a) individual components, and (b) both polarization ports of the overall OMT, shown for the design taking into account ("Compensated") and not taking into account ("Non-compensated") the fabrication imperfections.

to achieve the required matching, and the step height was optimized to 95 µm. Due to the height limitation for the post, optimized inductive irises, as shown in Fig. 1, were added to each rectangular waveguide to further improve the return loss. Fig. 1 (c) shows the final dimensions of the turnstile junction.

When designing a micromachined device of high complexity in general, and specifically for a turnstile OMT requiring high geometrical accuracy, it is important to consider the predictable fabrication imperfections, which impact, in particular, the return loss between the sub-components. These comprise the mask underetching and the side-wall sloping caused by the deep-silicon etching of the, from a micromachining perspective, very large open areas of the 864 µm wide waveguides. The expected underetching was estimated from test fabrication runs of similar geometries and was compensated for in the photolithographical mask design. The side-wall slopes were included in the optimization of the simulation model with a 4° angle, as shown in the drawings of the model in Fig. 1 and Fig. 2. The cross-section SEM image in Fig. 4 of the fabricated turnstile junction shows a 3.9° sidewall angle, very close to the predicted one.

Fig. 5 (a) shows the simulated return loss for the individual sub-components, i.e. the central turnstile junction, the H-plane bends, the E-plane bends, and the E-plane power combiner, along with the overall return loss for both polarization channels shown in Fig. 5 (b). Some of the components were re-optimized after cascading them to form the complete OMT. The figure shows the influence of the fabrication imperfections: the "compensated" traces show the simulation results for geometries optimized by taking into account the predictable fabrication imperfections, whereas the "non-compensated" traces show the simulation results of optimized designs using

ideal waveguides whose geometries were modified by the predicted fabrication imperfections.

In comparison to conventional E-plane split micromachined waveguides [7], the H-plane split approach based on SOI-wafers [17] provides well-defined sharp corners between the lateral walls of the waveguides and the bottom layers, which is important for accurately defining the small features necessary for this turnstile OMT design. In addition, this H-plane split approach has the advantage of a nanometre-scale surface roughness of the wider sides of the waveguides, which drastically decreases the insertion loss, without any post-processing surface-smoothening techniques [17]. As shown in this paper, this multi-level H-plane split approach allows for the implementation of micromachined waveguide components of high design complexity, including out-of-plane bends for horizontal to vertical waveguide transitions, vertically stepped transitions for impedance matching, and complex and well-matched recombination networks.

III. Fabrication

Deep reactive ion etching (DRIE) of silicon-on-insulator (SOI) wafers has already proven to be an accurate fabrication technology for low-loss waveguides at millimeter-wave frequencies [17]. The SOI wafers utilized in this work are made of a 275 µm thick silicon handle layer, bonded to a 30 µm silicon device layer with a 3 µm buried oxide (BOX) layer in between, as shown in Fig. 6. The handle layer is used to define the waveguide channels, the BOX acts as an etch stop, and the device layer forms the bottom wall of the waveguide.

The detailed process flow is shown in Fig. 6 for the bottom-most chip containing the turnstile junction. The wafers are first thermally oxidized to form a 2 µm silicon dioxide hard-mask layer on both sides of the wafer. The frontside and the first backside mask patterns are transferred to these layers by photolithography and dry etching of the oxide layer. An additional 2 µm silicon dioxide film is deposited on the handle wafer using plasma enhanced chemical vapour deposition (PECVD) to form the third hard mask which allows etching of two different levels from the backside, and is subsequently patterned with a third mask.

The deep silicon etching of all three layers is performed in an Applied Materials Centura Etch tool, based on an advanced Bosch process. The selectivity of the process over the silicon oxide mask is over 150:1, allowing the etching of deep trenches with a high resolution since a relatively thin mask is required. All oxide etching steps are performed in a SPTS Advanced Oxide Etch tool. First, the device layer is etched down to the BOX layer with Mask 1. Then the handle layer is etched with Mask 3 to form the waveguide channels. After this etching step the remainder of Mask 3 is removed with plasma etching to expose Mask 2, followed by the last silicon etching step, this time not through the whole handle layer, but only to a depth of 180 µm. This process allows accurate definition of the height of both steps, since they are totally independent, and etching time variations for the second step will not change the depth of the first one. This, and the resulting uninterrupted sidewalls, are significant advantages over

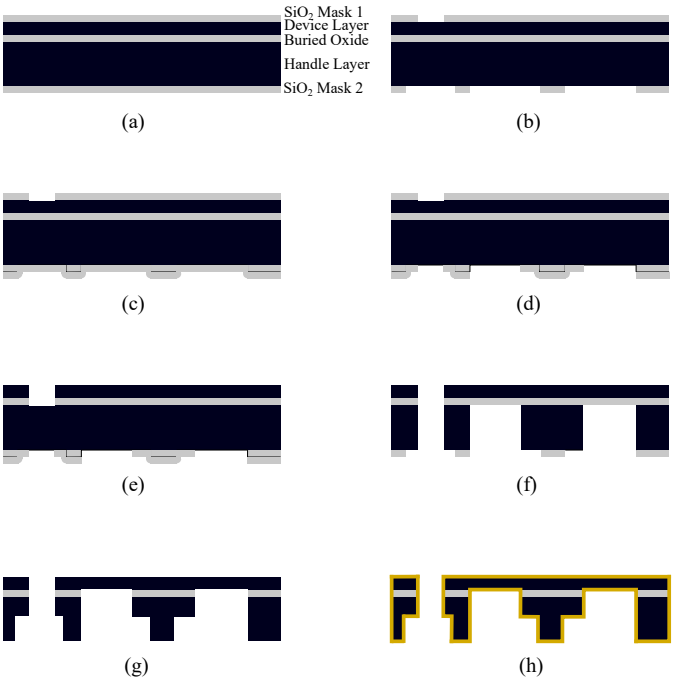


Fig. 6. Fabrication process flow for the turnstile junction of the OMT. (a) SOI wafer. (b) Pattern SiO_2 masks. (c) PECVD deposition of SiO_2 Mask 3. (d) Pattern SiO_2 Mask 3. (e) DRIE through Mask 1. (f) DRIE through Mask 3. (g) DRIE through Mask 2. (h) Gold sputtering.

subsequent accumulated multi-step deep-etching techniques, as utilized in [7], but requires longer etching times as well as high etching selectivity to the masks and etch stop layers. Fig. 7 shows a scanning electron microscope (SEM) image of the turnstile junction before and after the second etching step of the handle layer.

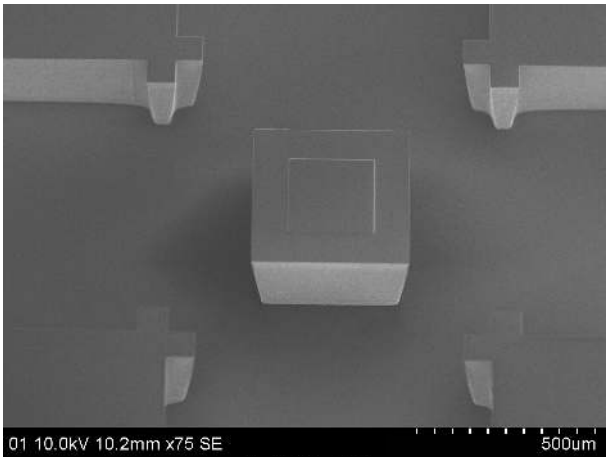
Finally, the individual chips are cleaned in oxygen plasma and metallized with a 2 µm thick gold layer in a sputtering tool. The skin depth at the lowest frequency of operation for gold is 160 nm, less than one tenth of the metal layer thickness. The SEM photographs in Fig. 8 show chips 1 and 3 after metallization, containing the turnstile junction, recombination networks, and waveguide ports.

The OMTs are then assembled by stacking the three chips in a custom-made holder for alignment and thermal-compression bonded at 250 °C for 1 hour. One of the E-plane U-bends from the recombination networks can be seen in Fig. 9. This cross-section was obtained by dicing one of the assembled OMT prototypes with a diamond saw and SEM imaging. The debris observed in the image was caused by the dicing process, but we could still analyse the bonding interface between the chips. No visible gaps that would impact on the performance of the micromachined waveguides were observed.

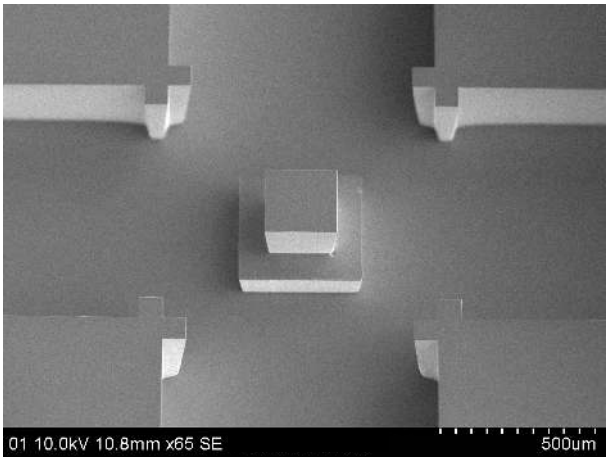
A fabricated and assembled OMT device, mounted on a waveguide flange, is shown in Fig. 10. The size of the OMT including alignment pins is half of the waveguide flange.

IV. Measurement Setup

To facilitate the connection of the waveguide parts for full characterization of the RF performance, two different chip sizes with identical OMTs were implemented: a 10 mm x

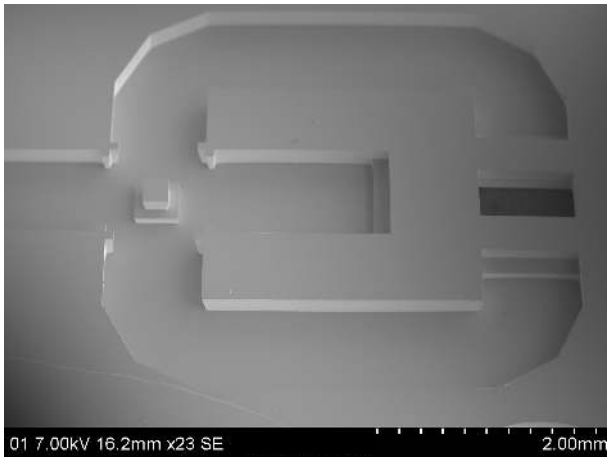


(a)

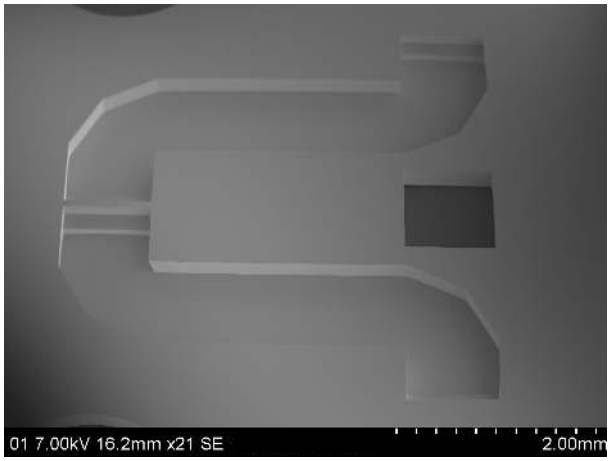


(b)

Fig. 7. SEM picture of turnstile junction (a) after the first etching step in the handle layer, and (b) after the second etching step in the handle layer.



(a)



(b)

Fig. 8. SEM picture of the metallized chips (a) turnstile junction, and (b) square port and E-plane power combiner.

10 mm chip which allows for connection to the rectangular ports only, and a full-flange sized 20 mm x 20 mm chip, shown in Fig. 11 (d), also allowing the connection to the square port. The first solution enables the basic measurements of the return loss by leaving the square port open, and also allows for a first estimation of the insertion loss and the cross-polarization level by shorting that port. The second chip layout provides access to all three ports of the OMT, but requires the use of two additional, custom-made micromachined test fixture chips for routing the waveguide ports of the OMT to the standard waveguide ports of the frequency extenders of a vector network analyser (VNA).

The first test fixture chip is a rectangular to square waveguide transition for independent characterization of each channel of the OMT. The second test fixture, shown in Fig. 11 (a), is a 40 mm x 20 mm large chip that routes one of the rectangular ports in the OMT to one of the VNA extenders, and loads the other port with a matched absorber, as described in [18]. This second test fixture enables the characterization of the insertion loss and of the return loss for each channel while loading the isolated port, as well as measurement of the cross-polarization level while loading the direct port.

All devices are designed with elliptical alignment holes, as described in [19], to ensure repeatable and accurate alignment between the silicon micro-machined chips and the CNC-milled standard test ports, superior to conventional alignment holes.

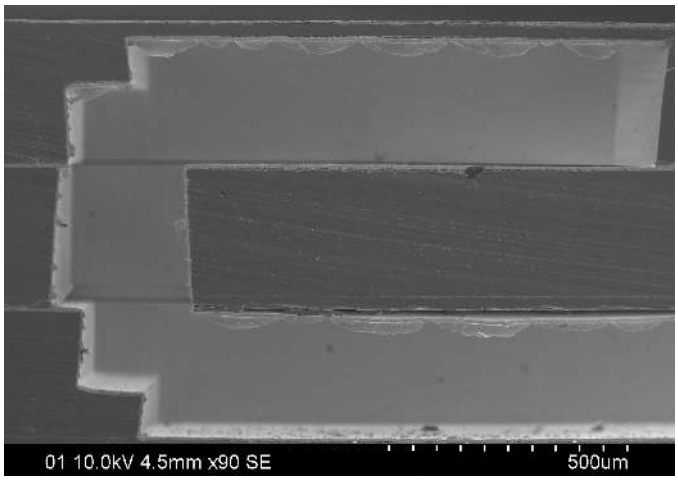


Fig. 9. Cross-section SEM image of an assembled U-bend routing the signal from Chip 1 to Chip 3.

A Rohde & Schwarz ZVA-24 VNA with ZC330 frequency

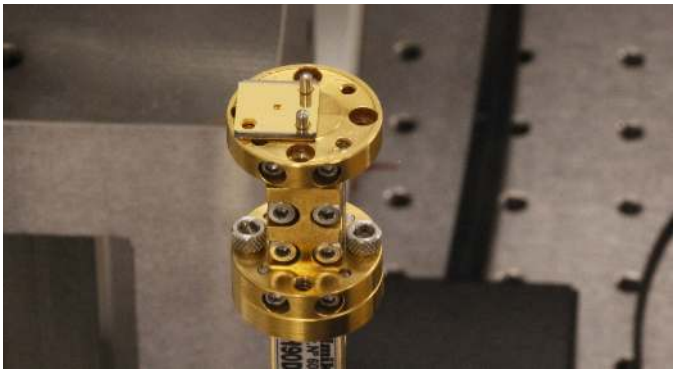
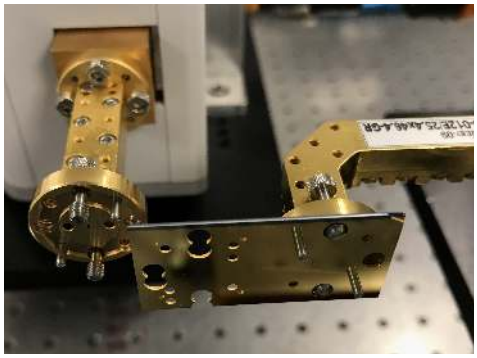


Fig. 10. Fabricated and assembled OMT device on a standard waveguide flange. The OMT design fits into a 5 x5 mm^2 area, and the overall chip size including alignment-pin holes is 10 x10 mm^2.



(a)

(b)

Fig. 11. Measurement setup: (a) silicon micromachined test fixture for routing the device ports to the extender flanges, and (b) OMT chip with all output ports designed for full-scale waveguide flange connection.

extenders was used for the RF characterization of the component. The reference planes for the measurements were set in the waveguide test ports using a through-open-short-match (TOSM) 2-port calibration. Two OMT prototypes were fabricated in two separate batches and characterized, the results of which are presented and discussed in this section. The results are also compared in Table I with prior art OMTs at mmW frequencies, which were identified to be the most representative high frequency OMT results to date.

The reflection measurements for both polarizations are shown in Fig. 12 for both devices and compared to the simulated data. The measured return loss is better than 16 dB for both polarizations over the whole waveguide band, with an average value of 22 dB, and is in excellent agreement with simulation data. Fig. 13 shows the insertion loss for both OMTs, better than 0.6 dB for the whole band. The average insertion loss value is better than 0.3 dB for both polarizations over the whole waveguide band for any of the two OMTs.

The cross-polarization level for both OMTs is shown in Fig. 14. Due to the nearly-perfect twofold symmetry of the micromachined turnstile junction, the average cross polarization level is above 50 dB for OMT 1, and above 60 dB for OMT 2. However, some spikes are present in both devices which deteriorate the performance to a worst-case level of 20 dB and 30 dB for devices 1 and 2, respectively. These spikes are even visible for OMT 1 as sharp signal drop-outs in the insertion loss shown in Fig. 13. No noticeable S_{21} drop-outs are observed in the measurements of OMT 2, which is in line with the lower level of the spikes in the cross polarization.

The different factors contributing to these spikes were investigated in [20], where most of them are a direct consequence of fabrication imperfections. Some of these factors, such as the symmetry of recombined branches or gaps along waveguide sections are not applicable for the silicon micromachining approach used for this work, due to the photolithographic patterning accuracy and the near-ideal metal bonding process, as discussed in Section III. However, misalignment between the chips in the stack could be a remaining issue, especially for the turnstile junction, which is composed by all three chips.

V. Measurement Results

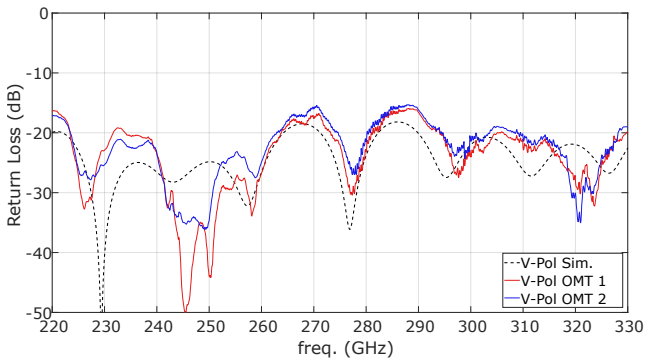
Therefore, the misalignment between all chips for both OMTs was investigated to study its influence on the cross-polarization spikes. Alignments errors lower than 4 µm were measured between all chips using Vernier scales implemented on the corners of each chip. The worst misalignment of 5 µm was found on OMT 1 and is shown in Fig. 15, explaining the worse performance of OMT 1 as compared to OMT 2. To confirm this, both OMTs were re-simulated including the measured alignment errors. It was found that while the return loss performance is not affected by these small misalignments in this frequency range, the cross-polarization can be strongly affected, as shown in Fig. 14. The re-simulated data adjusted by the alignment errors agrees very well with the measured cross-polarization, with the frequency spikes very well matching, despite the re-simulated peak values still being lower than the measured ones. In previous work [21] our group has shown that a misalignment error better than 2 µm is possible for carefully-assembled 3-chip stacks as used in this work, i.e. the already excellent cross-polarization might be possible to improve.

VI. Conclusions

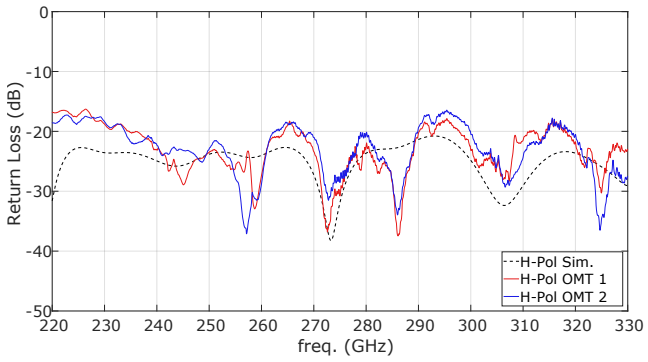
The complete RF characterization of a full-waveguide band, silicon micromachined turnstile OMT in the WM864 band (220 – 330 GHz), is presented for first time in this work. The full-band measured performance for the best OMT prototype

TABLE I
COMPARISON OF MMW OMTS

Reference	Device	Frequency Range FBW	Average Return Loss (Worst-case value)	Average Insertion Loss (Worst-case value)	Average Cross-Polarization (Worst-case value)	Fabrication Technology
[5]	Side-arm	78 – 102 GHz 26% FBW	24 dB (24 dB)	0.4 dB	45 dB (37 dB)	CNC-milling
[6]	Side-arm	500 – 600 GHz 18% FBW	25 dB (20 dB)	3 – 8 dB (8 dB)	25 dB (30 dB)	CNC-milling
[7]	Side-arm	500 – 600 GHz 18% FBW	20 dB (15 dB)	0.6 dB (2 dB)	25 dB (30 dB)	Silicon Micromachining
[8]	Bøifot	200 – 300 GHz 40% FBW	20 dB (15 dB)	0.4 dB (0.75 dB)	50 dB (35 dB)	Electric Discharge Machining
[9]	Bøifot	180 – 270 GHz 40% FBW	25 dB (18 dB)	0.5 dB (0.7 dB)	38 dB (27 dB)	CNC-milling
[11]	Bøifot	125 – 163 GHz 26% FBW	25 dB (20 dB)	0.2 dB (0.4 dB)	30 dB 35 dB	CNC-milling
[10]	Bøifot	385 – 500 GHz 26% FBW	15 dB (10 dB)	2.25 dB (3.25 dB)	12 dB (10 dB)	CNC-milling
[12]	Turnstile	210 – 290 GHz 32% FBW	18 dB (12 dB)	1 dB (1.2 dB)	30 dB (25 dB)	CNC-milling
[13]	Turnstile	75 – 110 GHz 38% FBW	20 dB (16 dB)	0.8 dB (1 dB)	51 dB (45 dB)	Electroforming
[14]	Turnstile	79.9 – 108.1 GHz 30% FBW	25 dB (20 dB)	0.25 dB (0.4 dB)	45 dB (42 dB)	Wire Erosion
This work	Turnstile	220 – 330 GHz 40% FBW	22 dB (16 dB)	0.3 dB (0.6 dB)	60 dB (30 dB)	Silicon Micromachining

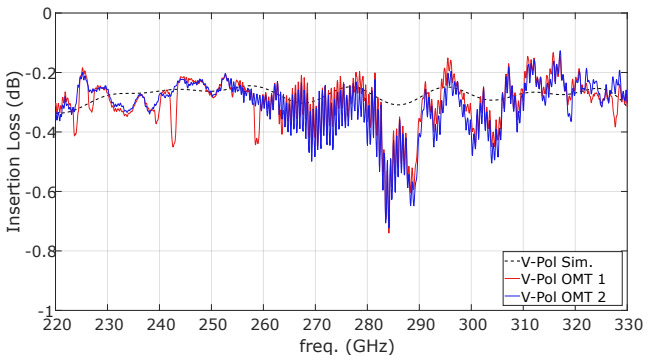


(a)

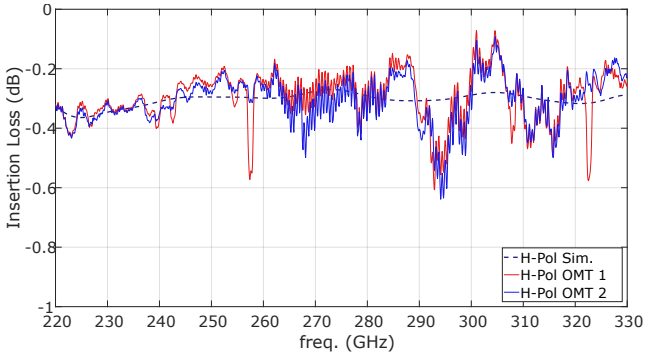


(b)

Fig. 12. Measured vs. simulated return loss for both fabricated OMT prototypes: (a) vertical polarization channel, and (b) horizontal polarization channel.



(a)



(b)

Fig. 13. Measured vs. simulated insertion loss for both fabricated OMT prototypes: (a) vertical polarization channel, and (b) horizontal polarization channel.

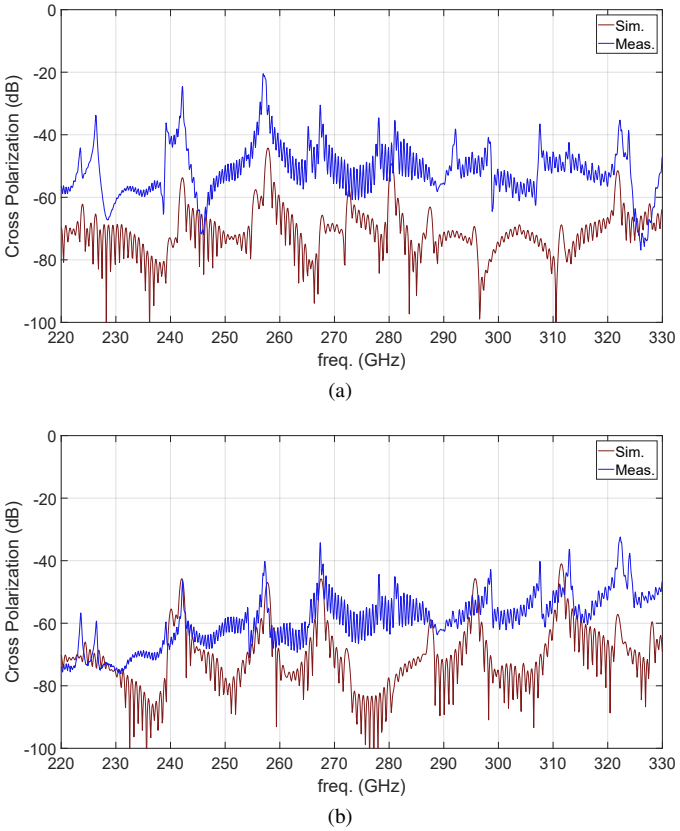


Fig. 14. Comparison of cross polarization levels for both fabricated OMT prototypes with simulated data including the effect of the measured misalignment. (a) OMT 1, and (b) OMT 2.

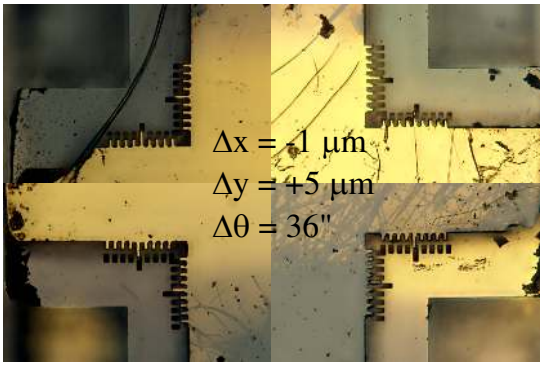


Fig. 15. Chip1-to-Chip2 misalignment for OMT 1 after bonding.

(device 2), with better than worst-case 16 dB return loss (average of 22 dB), 0.6 dB worst-case insertion loss (average of 0.3 dB), and worst-case 30 dB cross polarization (average 60 dB), is better than any previously reported wideband OMT in this frequency range. The design, taking fabrication imperfections into account, uses a three-chip stack with three etched levels each, resulting in a compact 10 mm x 10 mm x 0.9 mm size device, including alignment-pin holes. A chip-misalignment analysis has shown that the imperfections in the cross-polarization are attributed to the chip misalignment, which was up to 5 μm, and the already excellent device performance could be further improved by a more accurate assembly process. The very small volume and footprint of this component, the coplanar output port arrangement, and the ability for low-cost batch fabrication combined with high performance, makes silicon micromachining of turnstile OMTs a promising fabrication technology enabling integration of multi-pixel systems.

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