

Comparative Analysis of CMOS OTA

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Abstract : The Operational Transconductance amplifiers are significant building blocks for different analog circuits and systems which were previously implemented by using OPAMP. Recently, research is going on for implementing OTA circuits which will be highly linear, consumes lesser power and operate at lower supply voltage. Previous OTAs seldom worked over 200MHz whereas, the higher frequency OTA can be used as basic building block in several RF as well as microwave applications. The performance analysis of conventional OTA techniques and suggesting the topology, using advanced process technology that can break the previous frequency barrier is a key objective of this paper. Study and Analysis of different OTA topologies has been done. The appropriate topology is suggested which has a perfect balance between complexity and performance. The research includes analysis and comparison of OTA topologies from the point of view of effect of technology scaling on various performance parameters such as transconductance, supply voltage, Power consumption, dc gain, Frequency range, etc.

Keywords: CMOS, Frequency range, Operational Transconductance Amplifier (OTA), Operational amplifier (OPAMP), Transconductance.

I. Introduction

The operational amplifiers (OPAMP) are basic building blocks in implementing a variety of analog circuits such as amplifiers, filters, integrators, differentiators, summers, oscillators etc. OPAMPs work well for low-frequency applications, such as audio and video systems. For higher frequencies, however, OPAMP designs become difficult due to their frequency limit [1], [2]. At those high frequencies, operational transconductance amplifiers (OTAs) are deemed to be promising to replace OPAMPs as the building blocks. The Operational Transconductance amplifiers (OTA's) are important building blocks for various analog circuits and systems. The best suited component for design of modern OTA is CMOS devices which has less power requirements. CMOS provides the highest analog-digital on-chip integration. As the feature size of CMOS processes reduces, the supply voltage has to be reduced for the reduction of power dissipation per cell. Supply voltage reduction guarantee the reliability of devices as the lower electrical fields inside layers of a MOSFET produces less risk to the thinner oxides, which results from device scaling. However, the reduction in supply voltage leads to degraded circuit performance in terms of available bandwidth and voltage swing. Scaling down the threshold voltage of the MOSFETs reduces the performance loss (degraded bandwidth, low voltage swing etc.) to some extent but there is increase in the static power dissipation. The performance of digital circuits is improved by scaling but the analog cells benefit marginally because minimum size transistors cannot be used due to noise and offset requirements. To date, with much effort dedicated by analog IC researchers and the continuous scaling-down on commercial semiconductor technologies, the reported OTAs can work up to several hundred MHz [4]-[16]. The current trends in continual scaling down of transistor gate lengths and reduction in supply voltage have further added to the design challenges of analog circuits. A direct consequence of this has been performance investigation of transconductance circuits made using advanced CMOS process technology.

As we go on reducing feature size of silicon technology and supply voltage, it results in shrinkage of dynamic range and decrease in linearity of analog circuits [16]. Hence, designing analog circuits with reduced silicon feature size is challenging. When the characteristic lengths of CMOS devices are scaled down, both their channel delays and capacitive parasitic are reduced, which increases the cut off frequencies of the transistors. The CMOS 0.18- μm technology with f_{MAX} up to 40 GHz has been well commercialized [18], and 0.13- μm , 90-nm, 65-nm, and even 45-nm technologies are also available to researchers, all with much higher f_{MAX} than the 0.18- μm technology [19], [20]. Currently, high frequency, high linearity, and low power are the three main concerns of CMOS OTAs. Being a basic building block, OTA also find applications in high frequency domain, such as microwave, where research is still needed [4].

II. Literature Review

Currently, high frequency, high linearity, and low power are the three main concerns of CMOS OTAs. Tradeoffs have to be made among these aspects in designing practical OTAs. The current trends on these aspects are reviewed below.

Bogdan Pankiewicz, Mariusz Madej[3] in their research paper on high frequency OTAs have proposed a CMOS OTA topology for low power supply voltage and VHF continuous time filtering application. The input stage of the proposed circuit is based on CMOS inverters. The proposed amplifier was designed and simulated using the UMC (United Microelectronic Corp., Taiwan) 130 μm process with the 1.2 V supply voltage. The OTA was used in the filter application. SPECTRE simulation results show the cut off frequency of about 800 MHz and the THD less than -40 dB for the output voltage up to 0.5 Vpp.

You Zheng and Carlos E. Saavedra[4] have implemented very high-frequency operational Transconductance amplifier (OTA) with a new Feed forward Regulated Cascode. By the virtue of this topology, the authors have achieved bandwidth of 10 GHz and a large Transconductance of 11 mS. A theoretical analysis of the OTA is also provided in the paper. The fundamental OTA topologies discussed are as in Fig. 1 below.

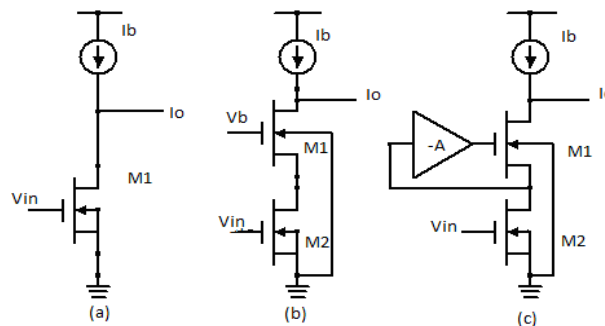


Figure1: OTA Topologies

Fig. (a) Indicates simple Transconductance amplifier where M1 is in saturation & converts input voltage to output current. It suffers from disadvantages such as low output impedance and linearity. Fig. (b) Indicates Cascode transconductor where M1 is in linear region & M2 provides isolation between I/O terminals. Advantages as compare to (a) are improved linearity and output impedance. Fig. (c) is a regulated Cascode feedback topology that make use of negative feedback via amplifier 'A'. Any change in the source voltage is inversely amplified by the amplifier which nullify the effect of voltage change hence Linearity is improved. This topology results in better stability.

Anil Kavala, Kondekar P. N, and Yang Sun [5] have proposed CMOS OTA for ultra-high frequency (UHF) OTA-C filters. It contains a Cascode topology which makes use of two pmos and nmos cascode that results in enhancement of G_m and the linearity. The OTA designed has supply voltage of 1.2V, G_m of 2.15 mS with linearity of 7 dBm. The power consumption of the OTA is 1.1 mW. The paper also explains application of this OTA which is used to design 400 MHz low-pass filter.

N. Raj, R. K. Sharma, A. Jasuja and R. Garg[9] have suggested low-power, low-voltage OTA application which incorporates better linearity and increased output impedance. The OTA uses high output impedance low voltage current mirror to increase its impedance. Instead of gate driven OTA, bulk driven is proposed for improved linearity. The achieved open-loop DC gain is 71.49 dB at unity gain bandwidth (UGB) of 98.16 KHz. The OTA runs at power supply of 0.9 volt which makes OTA to consume power is 285.99 nW. The authors have made use of CMOS 0.18 μm fabrication technology.

Montree Kumngern[10] have presented high frequency full-wave rectifier, which is suitable for CMOS technology implementation. The opamp based rectifiers suffers distortions at crossover & hence not suitable for IC fabrication. The OTA and its application as full-wave rectifier is discussed. An input voltage signal is in the range of milli-volts. Simulated rectifier results based on a 0.5 μm CMOS technology demonstrates very high operating frequency (300 MHz).

Y.L. Li, K.F. Han, X. Tan, N. Yan and H. Min[12] have proposed a new structure for an operational Transconductance amplifier. The proposed structure separates the AC path from the DC path, and achieves a significant boost in Transconductance under the same power and area budget. A folded-Cascode amplifier employing the improved recycling structure was implemented in SMIC standard 0.13 μm CMOS process.

You Zheng, and Carlos E. Saavedra[15] have demonstrated a very high-frequency operational Transconductance amplifier (OTA) with a new Feed forward-regulated cascode topology. The bandwidth achieved is 10 GHz and a Transconductance of 11 mS. A theoretical analysis of result is also performed in the paper. For high-frequency demonstration purposes author has constructed an inductor-less microwave oscillator. The fabricated oscillator operates at 2.89 GHz and it has a significantly larger output voltage swing and better power efficiency. The circuit was implemented in standard 0.18 μm CMOS process.

A comparative Study of Low Voltage OTA Designs was carried out by Deyasini Majumdar [16] in which design of three different OTAs was discussed. These OTAs operate at supply voltages about 3.3V. The

simulations were carried out in Cadence (with Hspice) for Taiwan Semiconductor Manufacturing Corporation’s (TSMC’s) 0.35µm CMOS process.

It may be concluded that as we go on reducing feature size of silicon technology and supply voltage, it results in shrinkage of dynamic range and decrease in linearity of analog circuits [16]. Hence, designing analog circuits with reduced silicon feature size is challenging. As the characteristic lengths of CMOS devices are scaled down, both their channel delays and capacitive parasitic are reduced, which increases the cut off frequencies of the transistors. The CMOS 0.18-µm technology with f_{MAX} up to 40 GHz has been well commercialized [18], and 0.13-µm, 90-nm, 65-nm, and even 45-nm technologies are also available to researchers, all with much higher f_{MAX} than the 0.18-µm technology [19], [20]. These submicron and deep-submicron advanced technologies offer significant potential for various OTAs to be implemented at RF and even microwave frequencies.

III. Circuit Description

The operational trans-conductance amplifier (OTA) is an amplifier whose differential input voltage produces an output current and hence it is a voltage controlled current source (VCCS). There is usually an additional input for a current to control the amplifier's trans-conductance. The OTA is similar to a standard Operational Amplifier in that it has a high impedance differential input stage and it may be used with negative feedback. Opamp is used to drive loads which are resistive or capacitive; whereas OTAs are used to drive purely capacitive loads (small cap. loads).

Low-voltage (LV) and low-power (LP) CMOS circuits have received considerable attention recently due to several reasons: Many of today's integrated circuit (IC) applications such as portable communication, remote computing and wireless communication systems require high performance IC's that operate under low supply voltage and consume low power. With the increasing circuit density in VLSI, the requirement of low cost fabrication demands circuits with low power consumption. The use of scaled down technologies has imposed a reduction of supply voltage [5]. The Operational transconductance amplifier (OTA) is an important building block in analog signal processing applications.

In the ideal OTA, the output current is a linear function of the differential input voltage, calculated as follows:

$$I_{out} = (V_{in+} - V_{in-}) \cdot g_m \tag{i}$$

where V_{in+} is the voltage at the non-inverting input, V_{in-} is the voltage at the inverting input and g_m is the transconductance of the amplifier.

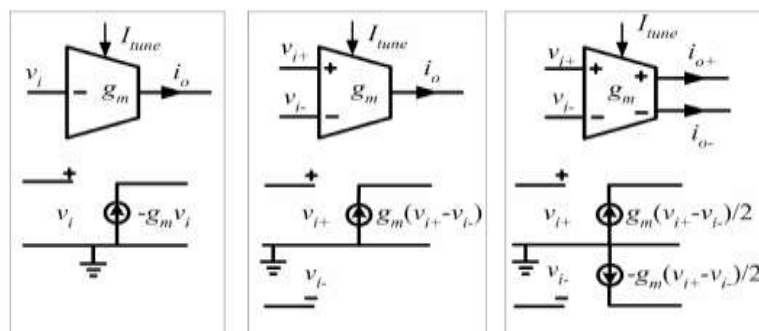
The amplifier's output voltage is the product of its output current and its load resistance:

$$V_{out} = I_{out} \cdot R_{load} \tag{ii}$$

The voltage gain is then the output voltage divided by the differential input voltage:

$$G_{voltage} = \frac{V_{out}}{(V_{in+} - v_{in-})} = R_{load} \cdot g_m \tag{iii}$$

The Transconductance of the amplifier is usually controlled by an input current, denoted as I_{tune} or I_{abc} ("amplifier bias current"). The amplifier's transconductance is directly proportional to this current. This is the feature that makes it useful for electronic control of amplifier gain. CMOS technologies are very convenient for implementing OTAs because their MOSFETs are inherently voltage-controlled current devices. A variety of CMOS OTAs with different topologies have been developed for different purposes so far. According to their input/output topologies, they can be categorized into three types, i.e., single input/output, differential-input single-output, and differential input/output.



(a) single-input/output (b) differential-input single-output (c) differential input/output

Figure 2: Three types of OTAs and their equivalent circuit models.

Fig.3 indicates Differential I/O topology of OTA. In this topology, two current mirrors are used to improve balance between differential paths. The current mirrors have size ratio B to boost output current by B-

times. As v_{i+} increases it results in increase in value of i_{d+} , which is transferred to output side with B-times multiplication. Similarly, the change in i_{d-} , due to current mirror on right side it gets B-times as compare to i_{d-}

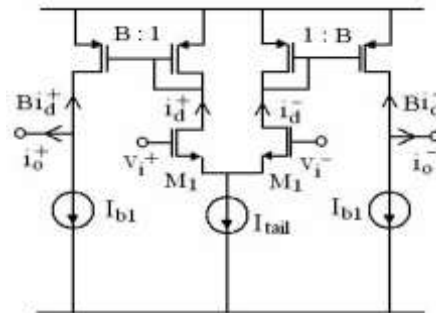


Figure 3: Differential I/O Topology of OTA

3.1 Feed forward Regulated Cascode OTA

Topology which can work at low voltage and higher frequencies is desired. The most important aspect of topology selection is improved Transconductance with better linearity at high frequencies. The simplest topologies illustrated above in Fig.1 and 2 have been used in some RF/microwave circuits. The disadvantage of such topologies is low output impedance, low linearity and less Transconductance. The feedback regulated topologies where the feedback network introduces delay using voltage regulation results in complex circuits. Thus, such topologies are not suitable for OTA design. The topologies using current mirror are also not suitable because they result in different time delays for two paths. The feed forward Cascode topology is preferred because it has a perfect balance between complexity and performance [4].

Fig.4 represents a differential input/output topology which has two pmos cascode and two nmos cascode. The transistors T9-T10 act as DC current source. The circuit arrangement is made in such a way that variation in output voltage is decreased. The topology results in high input output impedance and transconductance. The performance parameters analyzed for various process technologies include Transconductance Gain (G_m), power consumption, frequency range, supply voltage etc.

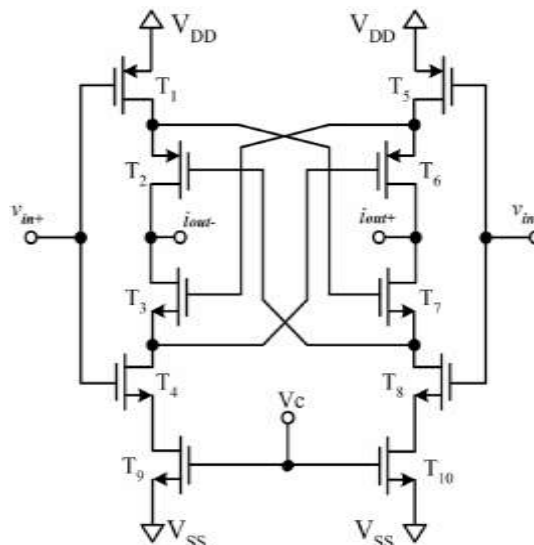


Figure 4: Feed forward Regulated Cascode OTA

IV. Result & Conclusion

The various topologies of OTA are studied analyzed for Transconductance, dc Gain, power consumption, frequency range, supply voltage etc. Basically, the approach is based on using CMOS advanced process technologies with proper topology to optimize the performance parameters of OTA. Some of the comparison parameters of reviewed OTA are listed below.

Table1: Comparison of OTA parameters using different process technologies and supply voltages.

CMOS process Technology used	Transconductance Obtained	Power Consumption	Frequency Range	Supply Voltage
350 nm	0.76 mS	0.696 mW	UGB of 537 MHz	2 V
180 nm	88.5 dB dc gain	1.02 μ W	UGB of 83.88KHz	0.5 V
180 nm	71.49 dB dc gain	0.2859 μ W	UGB of 98.16KHz	0.9 V
180 nm	62 dB dc gain	0.25 mW	UGB of 160 MHz	0.8 V
130 nm	1.56 mS	1.97 mW	Cut off Freq. Of 800MHz	1.2 V
130 nm	2.15mS	1.1 mW	1.2 GHz	1.2 V

It may be concluded from the above table that when the characteristic lengths of CMOS devices are scaled down, both their channel delays and capacitive parasitic are reduced, which increases the cut off frequencies of the transistors. This ultimately results in increased bandwidth of OTA. Also, the choice of topology used result in better performance of OTAs at lower power consumptions and increased bandwidth. In OTA design the high frequency, high linearity and low power are the three main concerns but tradeoffs have to be made among these aspects for designing of practical OTA circuits.

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