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COMPARATIVE EFFICIENCY ANALYSIS BETWEEN A CONVENTIONAL SINGLE-PHASE INVERTER AND AN INVERTER WITH A MINIMALIST ACTIVE POWER DECOUPLING CIRCUIT

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Abstract: *This paper focuses on a comparative analysis between the conventional single-phase H-bridge inverter and an inverter implementing a minimalist active power decoupling method, which is used to eliminate the power ripple of twice the fundamental frequency at the DC link. This method allows minimising the need of large electrolytic DC link capacitors, only two smaller film capacitors being required on the hardware side. The implemented 1 kW inverter makes use of silicon carbide (SiC) MOSFETs, offering the main advantage of high switching frequencies, reduced size and improved efficiency. The performance analysis, including switching and conduction losses and the inverter efficiency, is done through the results obtained from simulations and experiments.*

Key words: *SiC MOSFETs, power decoupling, transformer-less inverter.*

1. Introduction

With countries seeking to decarbonize the energy mix, renewable energy stands out as the most suitable solution. Inverters plays a central role in the conversion of energy from DC to AC power. In inverter designs, the important parameters to consider are reliability, efficiency, cost, size and weight [2]. To minimize downtime during inverter lifetime, and to minimize maintenance cost, it is critical to design for reliability [6], [7], [10], [12].

One of the components that affects the reliability of inverters, mainly in the case of single-phase configurations, is the DC-link electrolytic capacitor [4]. In voltage source converters, the DC link capacitor is used to ensure small DC voltage ripple, to maintain the power balance and to provide short-term energy storage [11]. Due to the low cost and relatively high energy density, the electrolytic capacitor is widely used in power electronics. However, its main drawback consists in the relatively high equivalent series resistance (ESR), which causes a higher thermal stress when ripple current flows through the capacitor, and consequently accelerating the degradation process. Besides the

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current ripple due to the inverter switching, the main current stress of a DC-link capacitor comes from the inherent pulsation with twice the output frequency (e.g. 100 Hz) of the instantaneous power. Therefore, to remove the drawback related to the electrolytic capacitor degradation, intensive investigations of alternative active solutions that makes use of more reliable film capacitors have been done recently [11]. For the same scope, an active power decoupling method for single-phase inverter is proposed in [9], which employs no additional power electronics to eliminate the power ripple of twice the fundamental frequency at the DC-link. Being a simple solution, the analysis presented in this paper will use the topology proposed in [9].

Another major goal today is to reduce the inverter size and cost, while maximising efficiency. In this regard, technologies utilising wide bandgap semiconductors, such as silicon carbide (SiC), provide superior performance than conventional silicon-based semiconductors. SiC-MOSFETs are now commercially available, bringing the main advantages of operating at higher switching frequencies, while exhibiting fewer switching losses, hence higher efficiency, compared to silicon IGBTs [1], [3], [13]. High switching frequencies translate to a reduction in filtering requirements (small inductor). Therefore, the two single-phase inverter topologies analysed in this paper are implemented with SiC-MOSFETs.

2. Modelling and Simulation

Two single-phase inverter topologies are hereinafter analysed, the conventional H-bridge and the inverter proposed in [9] based on a minimalist power decoupling circuit. The modelling of both inverter types was done using PLECS simulation software [14]. Figures 1 and 2 shows the electro-thermal model, developed for the two studied topologies. On the DC-side, the first stage of a PV inverter, which typically consists of a boost converter, was modelled as a generic DC voltage source with a series inductor.

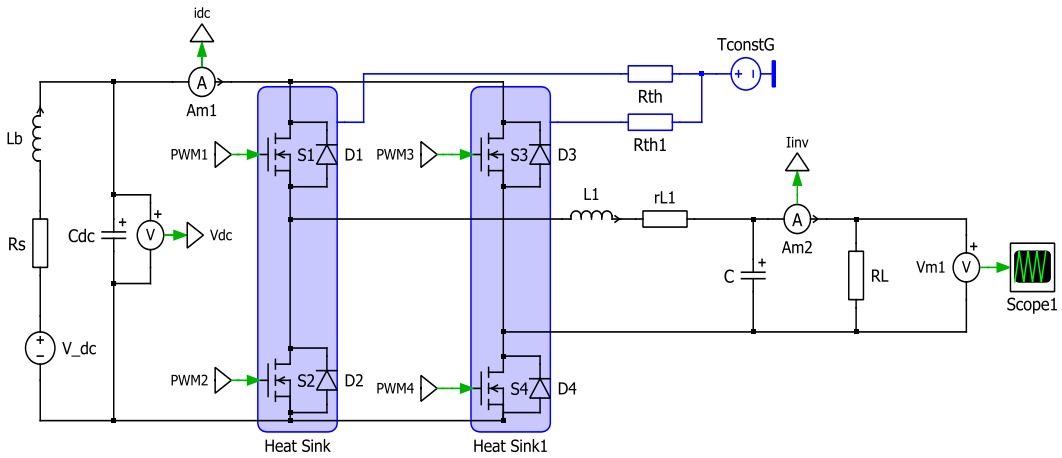

Fig. 1. *PLECS model of H-bridge inverter*

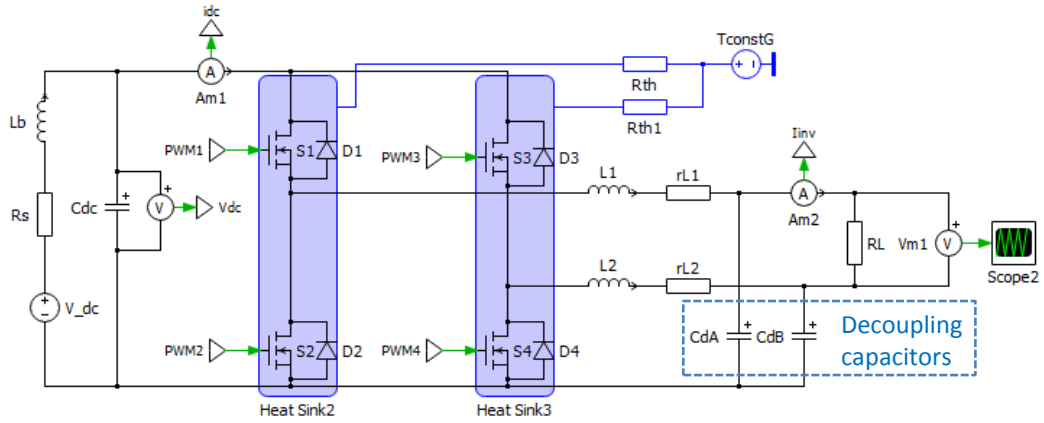

Fig. 2. *PLECS model of studied topology with active power decoupling*

2.1. Controller Implementation

As shown in Figure 3, to provide active power decoupling to the inverter presented in Figure 2, besides the conventional voltage-current cascaded controllers, a decoupling controller was added to cancel the even-order current harmonics (i.e. 2nd, 4th and 6th mainly) at the DC-link side. By this way, the pulsating power will be redirected to the two film capacitors, C_{dA} and C_{dB}. The decoupling controller transfer function is given in (1) [9]:

$$G_D(s) = \sum_{j=2,4,6} \frac{2k_{jD}\omega_j}{s^2 + \omega_j^2} \tag{1}$$

where k_{jD} is the gain constant of the j component and ω_j is the pulsation frequency.

The supply of the load with a sinusoidal voltage of constant magnitude is done through a feedback control system based on voltage and current controllers. Both controllers are implemented as proportional-resonant (PR) structures, including additional resonators for harmonics compensation at the main frequencies (i.e. 3rd, 5th, 7th). The transfer functions of the controllers are given as shown by (2) and (3):

$$G_I(s) = k_{pI} + \sum_{j=1,3,5,7\ldots} \frac{2k_{iIj}s}{s^2 + \omega_j^2} \tag{2}$$

$$G_V(s) = k_{pV} + \sum_{j=1,3,5,7\ldots} \frac{2k_{iVj}s}{s^2 + \omega_j^2} \tag{3}$$

where k_{pI}, k_{pV} are the proportional gain constants of the current and voltage controllers, k_{iI}, k_{iV} are the integration gain of the current and voltage controllers and ω_j is the pulsation frequency.

At resonance frequency (ω_j), the PR controller gives a high gain, which eliminates steady state error at that frequency. The controller gain is tuned to achieve good

stability margins and good transient response. Figure 3 shows the inverter control for the inverter with active power decoupling.

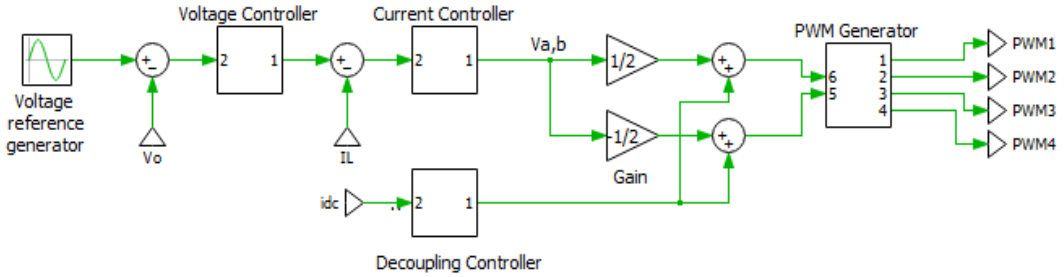

Fig. 3. *Inverter control for the inverter with active power decoupling*

2.2. Thermal Modelling and Inverter Losses

The thermal modelling of the MOSFETs and the associated cooling system was done using PLECS software. The model gives the thermal transient behavior from MOSFETs junctions to the ambient. According to the experimental setup conditions, each of the two inverter legs is placed on a heatsink, as shown in Figures 1 and 2. The heat transfer path is modelled using the corresponding thermal impedances (as RC chain).

Inverter losses arises mainly due to the switching and conduction of the four MOSFETs with their antiparallel diodes. Additional losses occur in the snubber circuits and in the filter.

The relationship between the MOSFET junction temperature in steady-state and case temperature is given as follows (4),

$$T_c = T_j - R_{\theta JC} * P_D \, , \tag{4}$$

where T_c and T_j is the case and junction temperature respectively, $R_{\vartheta JC}$ is the thermal resistance (junction to case) and P_D is the power dissipated in the junction.

Based on the conduction and switching characteristics of the SiC MOSFETs and their corresponding body diodes, provided by the manufacturer [15], the power losses were modelled using PLECS software thermal library. For a consistent comparative analysis between simulation and experiment, the thermal circuit (MOSFETs, heatsinks) was modelled as close as possible to match the physical properties of the test boards used for experiments. As shown in the following, the case temperature (which could be measured directly in the experiments) was obtained similar in simulations ($T_c \cong 43$ °C), which proves that the modelling was accurate.

3. Experimental Validation

To validate the simulation, an experimental setup was done using a laboratory test bench for both types of inverters. Figure 4 shows the experimental setup. The setup includes two SiC MOSFET High-Frequency Evaluation Boards [15] as the two legs of the

inverter, and a real time controller dSPACE DS1103 board. For measurements, a Yokogawa WT-1806 power analyser was used. The DC input was provided by a 450 V power supply. The other parameters are listed in Table 1. The inverter efficiency was calculated from the simulation and experimental results as shown in (5):

$$\eta = \frac{P_{out}}{P_{out} + \Delta P_{inv}} \tag{5}$$

where ΔP_{inv} and P_{out} are the total power loss and the output power of the inverter respectively**.**

Inverter Parameters Table 1

Parameter	**Conventional Inverter**	**Inverter with active decoupling method**
Rated output active power	1 kW	1 kW
Rated output frequency	50 Hz	50 Hz
Rated RMS output voltage	230 V	230 V
Output filter Inductances	L = 1 mH	L1 = L2 = 1 mH
Output filter capacitor	4.4 µF	--
DC voltage	450 V	450 V
Decoupling capacitors	--	$C_{dA} = C_{dB} = 60$ µF
Switching frequency	20 kHz - 80 kHz	20 kHz - 80 kHz

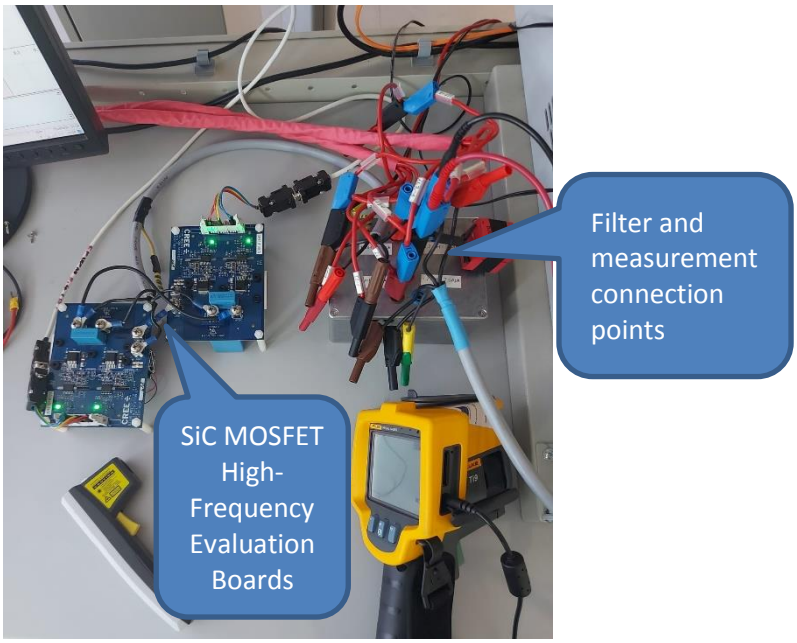

Fig. 4. *Experimental setup*

4. Results and Discussion

This paper's main contribution consists in the comparative efficiency analysis of two inverter topologies, shown in Figures 1 and 2, analysis carried out by means of simulation and experimental tests, as explained in the previous sections. Therefore, this section synthesizes the main obtained results, the focus being on the efficiency analysis at different switching frequencies, as illustrated in Figures 5 to Figure 7. The focus is on the SiC MOSFETs operation and, therefore, the first analysis presented in Figures 5 and 6 (simulation and experiment) includes only the efficiency of the H-bridge in the two inverter topologies (conventional and with active power decoupling). To accurately match the experiment, besides the switching and conduction losses of the MOSFET, snubber circuits losses were also considered in the PLECS simulation.

The efficiency of both inverter types shows an overall decrease as the switching frequency increase due to the increase in the switching losses of the MOSFETs. For the conventional inverter the maximum difference between the simulation and experimental results is 14% while for the inverter with active decoupling method the maximum difference is 10%. These results prove that the developed simulation model is sufficiently accurate and can be used for further investigations to improve the efficiency of the proposed inverter topology.

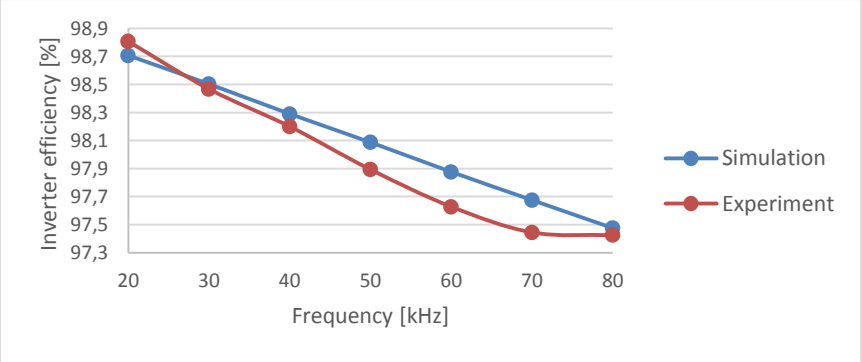

Fig. 5. *Efficiency analysis of the conventional inverter*

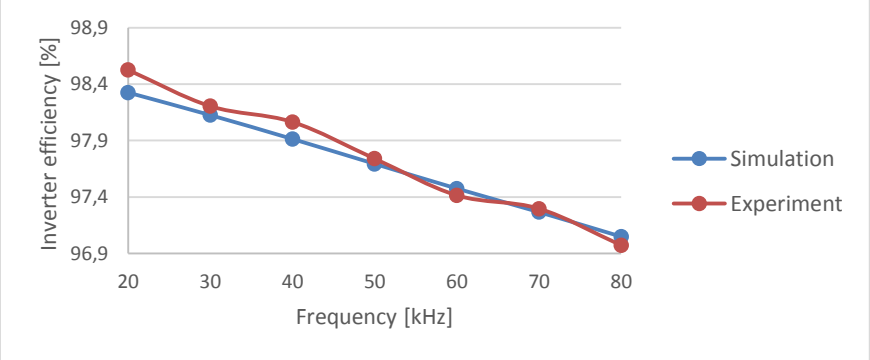

Fig. 6. *Efficiency analysis of the inverter with active power decoupling*

Figure 7 shows the overall (inverter and output filter) measured efficiency for the inverter with active decoupling method and the conventional inverter. The inverter with active power decoupling shows a decrease in the overall efficiency compared to the conventional inverter (1.17% maximum difference at 60 kHz). This is due to the additional losses introduced by the additional components of the active power decoupling circuit and higher current loading of the inverter. However, the reduction in efficiency is compensated by the increase in reliability, as the active decoupling method allows the use of a much smaller electrolytic DC-link capacitor [8]. Moreover, the analysis does not include the additional losses occurring in the large electrolytic DC-link capacitor of the conventional inverter, which will further reduce the efficiency gap between the two solutions. Therefore, the results show that the proposed inverter with power decoupling is a viable replacement solution for the conventional inverter, especially in applications where reliability represents a major concern, as PV systems. Based on the results presented in this paper, the authors have started to extend their study to optimise the solution according to the specific operating conditions of a PV system. Recent results obtained by the authors in [5] show that, by optimizing the output filter, the proposed inverter efficiency can be further improved.

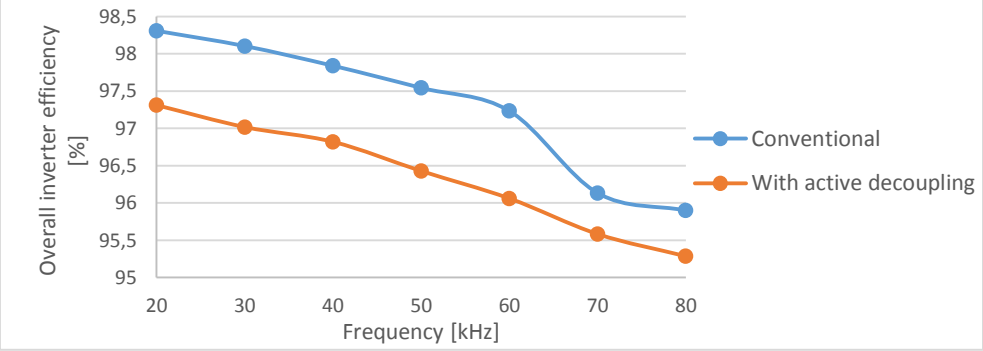

Fig. 7. *Overall efficiency analysis of the two inverter topologies (experimental)*

5. Conclusion

This paper provided a comparative analysis between a 1 kW conventional single-phase inverter and an inverter implementing a minimalist active power decoupling method. To achieve high switching frequencies, wide band SiC MOSFETs were used. The inverter losses were determined at different switching frequencies using power electronics simulation software. The results were further validated experimentally using a laboratory test bench. The efficiency comparison for both types of inverters, based on simulation and experimental results, have shown that the active power decoupling method, which only slightly increases the inverter complexity by the two small film capacitors it requires, is a viable solution to reduce the DC-link capacitor stress. The results have also revealed that the simulation model is accurate enough (a maximum difference of 14% between simulation and experimental results) to be used for further optimisations and losses analyses.

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