Comparative Evaluation of Modulation Algorithms for Neutral-Point-Clamped Converters

Ashish Bendre, *Member, IEEE*, Slobodan Krstic, *Member, IEEE*, James Vander Meer, and Giri Venkataramanan, *Member, IEEE*

***Abstract*—Neutral-point-clamped converters are increasingly applied in industrial drive systems as they allow the use of lower voltage devices in higher voltage applications, provide reduced output voltage total harmonic distortion (THD), and can develop low common mode voltage. Several distinct modulation strategies have been proposed in the past for eliminating the common mode voltage, providing low THD output voltage or reducing the neutral point current ripple. However, each of these strategies improves the performance of the converter on one metric while trading off performance in other metrics. Nearest three vector, radial state, and zero-common-mode types of space-vector modulation techniques are compared using metrics that clearly elucidate the performance tradeoffs. Analytical models, computer simulation results, and experimental verification are presented.**

***Index Terms*—Converter control, harmonics, modeling, modulation, multilevel converters.**

I. Introduction

THREE-LEVEL or neutral-point-clamped (NPC) converters are seeing increased application in industrial high-power drive systems [1], [2]. Several carrier-based and space-vector-based modulation strategies have been proposed for these converters [3], [4]. These classical strategies were designed to provide adjacent state switching action in the converter, which yields the lowest possible output voltage and current total harmonic distortion (THD). However, both of these strategies exhibit significant third harmonic injection into the neutral point of the converter that causes an increase in the required dc-link capacitance of the converter. This adds significant cost and volume penalties for the three-level converter systems when compared to two-level converters where such third harmonic components are absent. Furthermore, the common-mode voltage generated at the terminals contains third harmonic content in addition to the switching frequency harmonics making electromagnetic interference (EMI) filter design challenging. While switching frequency common-mode voltage and the resulting EMI is unavoidable in two-level converters, it can be eliminated in three-level converters by proper choice of states. The classical space-vector and carrier methods do not achieve this as they are exclusively focused on output voltage synthesis.

Several modified space-vector modulators have been presented in the literature before that focus on using redundant state switching to achieve neutral-point regulation [5]–[7], neutral point ripple elimination [8] and common mode elimination [9], [10]. Each of these goals is realized at the expense of a loss of performance in other areas. A comprehensive analysis of the output voltage synthesis, neutral-point current injection, and the common-mode voltage generation for all of the modulators is needed to clarify the tradeoffs involved in modulator selection. The presentation of the available modulator choices for three-level diode-clamped converters and their performance tradeoffs is the primary focus of this paper.

The classical space-vector modulation method for three-level diode-clamped converters, which relies on nearest three vector (NTV) selection [4], is introduced in Section II. Two modified algorithms—a neutral-point ripple elimination algorithm [8] and a common-mode minimization algorithm [9] are discussed in Section III. The state selection effected by the modulators is identified on the switching state diagram of a three-level diode-clamped converter and the three key metrics used for evaluating modulator performance are introduced. Extensive simulations were carried out for the three modulation methods and results from these are presented in Section IV. The three modulation schemes were implemented on a prototype three-level converter to validate the simulation and analysis and to estimate the impact of parasitics and other unmodeled higher order effects. These hardware results are presented in Section V, with special emphasis on the performance metrics developed in Section III. The conclusions derived from this study are summarized in Section VI.

II. Converter Model

A simplified schematic of a three-level NPC converter is shown in Fig. 1. Each phase leg consists of four switching devices and two clamping diodes that limit the voltage excursions across each device to half the input dc-bus voltage.

It is convenient to consider the equivalent circuit model shown in Fig. 2, containing three single-pole triple-throw switches for developing the analysis of the converter operation, harmonic injection, and modulation strategy. Here, each of the three throws for the switches is connected to a dc-bus level: top (V_1), middle (V_0), or bottom (V_{-1}). The switching action

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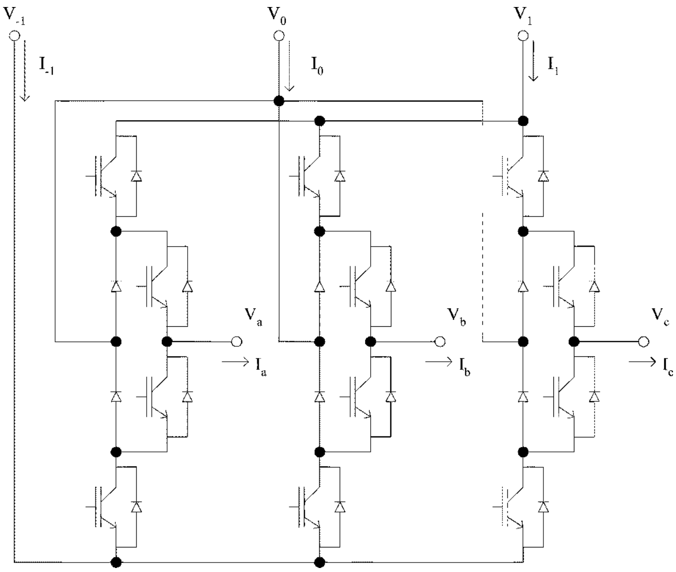

Fig. 1. Simplified schematic of a three-level converter.

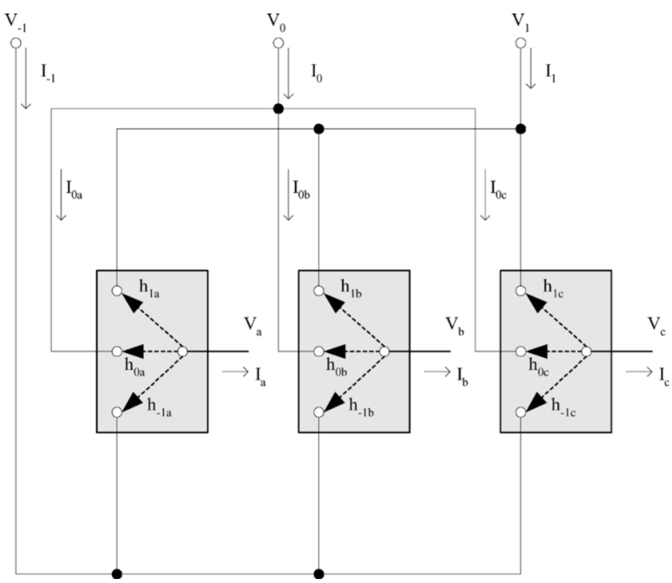

Fig. 2. Single-pole triple-throw switch representation of a three-level converter.

of each of the throws can be represented by their respective switching functions (h_{0a}, h_{1a}, etc.) as shown in the figure. On the dc side, three dc stack currents can be defined as top (I_1), middle (I_0), or bottom (I_{-1}).

The following matrix equations that relate the dc-bus variables to the ac output variables can be written for three-level converters [6]:

$$\begin{pmatrix} V_a(t) \\ V_b(t) \\ V_c(t) \end{pmatrix} = \begin{pmatrix} h_{1a}(t) & h_{0a}(t) & h_{-1a}(t) \\ h_{1b}(t) & h_{0b}(t) & h_{-1b}(t) \\ h_{1c}(t) & h_{0c}(t) & h_{-1c}(t) \end{pmatrix} \begin{pmatrix} V_1 \\ V_0 \\ V_{-1} \end{pmatrix}$$
$$\begin{pmatrix} I_1(t) \\ I_0(t) \\ I_{-1}(t) \end{pmatrix} = \begin{pmatrix} h_{1a}(t) & h_{1b}(t) & h_{1c}(t) \\ h_{0a}(t) & h_{0b}(t) & h_{0c}(t) \\ h_{-1a}(t) & h_{-1b}(t) & h_{-1c}(t) \end{pmatrix} \begin{pmatrix} I_a(t) \\ I_b(t) \\ I_c(t) \end{pmatrix}. \tag{1}$$

The neutral-point current $I_0(t)$ is given by the second row of the second equation of the set in (1). As the switching functions assume values of 0 and 1 at the switching frequency, the neutral-point current contains switching frequency content as well as low-frequency (primarily triplen harmonics) content when traditional space-vector modulators are used [11]. Pertinent low-frequency information can be extracted from (1) by using generalized averaging techniques [6]. For this extraction each element h_{ij} is replaced by its averaged equivalent m_{ij} as follows:

$$m_{ij}(\tau) = \frac{1}{T} \int_{\tau-T}^{\tau} h_{ij}(t) \cdot dt. \tag{2}$$

By further integrating the appropriate high-frequency averaged stack current over a period of the fundamental waveform, the net average neutral point current can be obtained as illustrated below

$$I_0^{\mathrm{AVG}} = \frac{1}{T} \int_0^T \begin{pmatrix} m_{0a}(t)I_a(t) + m_{0b}(t)I_b(t) \\ +m_{0c}(t)I_c(t) \end{pmatrix} dt. \tag{3}$$

In a similar manner, a complete low-frequency harmonic signature of the neutral-point current can be determined by performing a Fourier analysis of the neutral-point current, expressed within the parenthesis in (3). The total low-frequency harmonic content of the neutral-point current can be determined using

$$I_0^{\mathrm{HARM}} = \sqrt{\frac{1}{T} \int_0^T \begin{pmatrix} m_{0a}(t)I_a(t) + m_{0b}(t)I_b(t) \\ +m_{0c}(t)I_c(t) \end{pmatrix}^2 dt - (I_0^{\mathrm{AVG}})^2}. \tag{4}$$

The common-mode voltage is the voltage produced at the output terminals of the converter with reference to the midpoint of the dc bus, which is also the neutral point. This voltage can be expressed in terms of the dc-link voltages as follows:

$$V_{\mathrm{CM}}(t) = \left(\frac{1}{3}\right) \begin{pmatrix} V_1 & V_0 & V_{-1} \end{pmatrix} \times \begin{pmatrix} h_{1a}(t) + h_{1b}(t) + h_{1c}(t) \\ h_{0a}(t) + h_{0b}(t) + h_{0c}(t) \\ h_{-1a}(t) + h_{-1b}(t) + h_{-1c}(t) \end{pmatrix}. \tag{5}$$

The common-mode voltage is a high-frequency phenomenon and averaging techniques cannot be used to model these effects. If the converter is fed from a dc source with a fixed dc voltage V_{DC}, additional constraints are introduced. These can be mathematically expressed by setting $0.5V_{\mathrm{DC}} = V_1 = -V_{-1}$ and using the variable V_0 to describe the neutral-point variation.

III. NTV Modulation

It is known that the switching states for the three-level converter for three-wire loads can be represented on a (g–h) plane as shown in Fig. 3, [4].

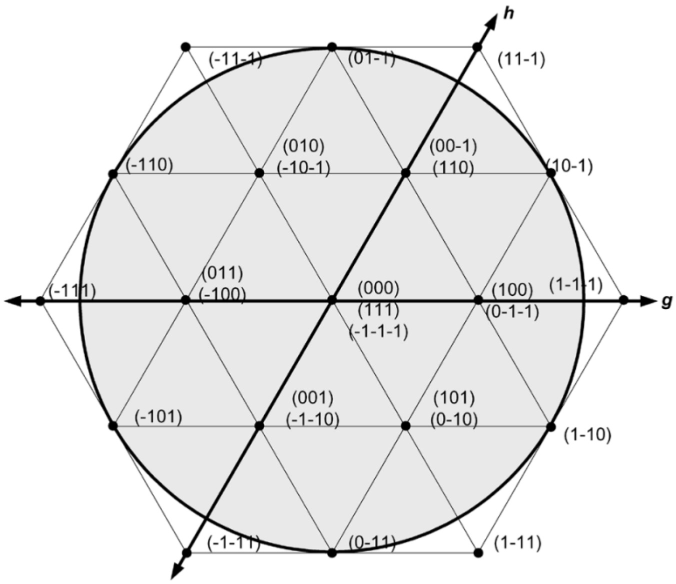

Fig. 3. Switching states of a three-level converter.

A conventional NTV space-vector algorithm will yield nonzero duty cycles for all states on the outer hexagon for suitably high modulation indexes. It may be noted from the figure that switching state redundancies appear on the inner hexagon, where two switching states are available for each position. Furthermore, these redundant states on the inner hexagon may be grouped into two subsets, each representing power transfer from one of the two dc buses constituting the stack. The ratio of distribution of duty cycles between the two possible subsets may be represented by a continuous "sharing function" sf_1^1. It can be shown that for maintaining balanced dc-bus voltages, the long-term average value of the sharing function has to be 0.5 [7].

The NTV algorithm chooses states exclusively based on their proximity to the reference vector position, disregarding any other criterion, which leads to the lowest ripple at the terminals and the best THD. This approach of choosing the NTVs prevents large steps in the pole-to-pole voltage and if the redundant states are chosen appropriately within a switching period, adjacent state switching can be obtained on all three pole voltages as well, minimizing switching events and losses. With this algorithm, if the reference vector magnitude is large enough, all of the states, except the zero states, will be selected as the reference vector traverses through its complete revolution. If the reference vector is small enough, then all the states, except those on the outer hexagon will be chosen. The largest voltage that can be generated at the output of the converter with linear modulation corresponds to the inscribed circle in the hexagon as shown in Fig. 3.

The sectors traversed by the reference vector for a given (sufficiently large) value of modulation depth are shown in Fig. 4. Within each sector, averaged duty cycles can be derived for each of the three positions that form the three vertices of the sector, with the remaining positions assigned zero duty cycles. Expressions can be written for the averaged throw functions within each sector as a summation of duty cycles of states that connect the appropriate dc bus to the proper pole.

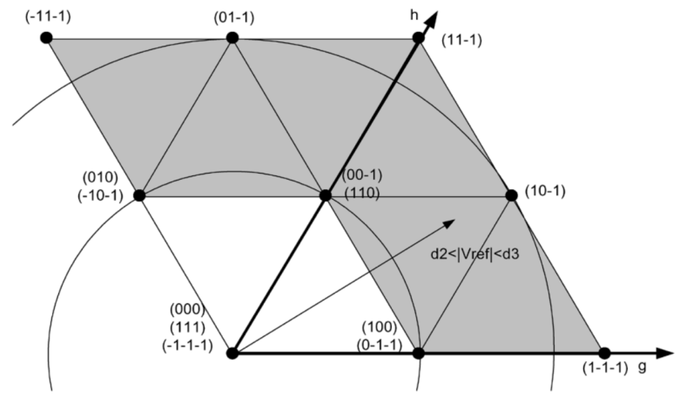

Fig. 4. Sectors swept during 120° excursion of the reference.

For example, in the sector formed by [(1-1-1), (10-1), (100, 0-1-1)]

$$\begin{aligned} \mathrm{m_{0a}}(t) &= d^{0-1-1}(t) \\ \mathrm{m_{0b}}(t) &= d^{100}(t) + d^{10-1}(t) \\ \mathrm{m_{0c}}(t) &= d^{100}(t). \end{aligned} \tag{6}$$

Furthermore, from the second row of the second equation of (1), the neutral-point current $\mathrm{I_o}(\mathrm{t})$ can be written as follows:

$$\begin{aligned} I_0(t) = d^{0-1-1}(t)I_a(t) + d^{100}(t)I_b(t) \\ + d^{10-1}(t)I_b(t) + d^{100}(t)I_c(t). \end{aligned} \tag{7}$$

Noting that the duty cycles of states (0-1-1) and (100) are equal, with sharing function $= 0.5$, this equation can be written as follows:

$$I_0(t) = d^{0-1-1}(t)(I_a(t)+I_b(t)+I_c(t))+d^{10-1}(t)I_b(t). \tag{8}$$

For balanced three-phase currents, this further reduces to

$$I_0(t) = d^{10-1}(t)I_b(t). \tag{9}$$

It can be shown that this condition occurs in every sector, where the neutral-point current is equal to the product of one of the phase currents and the duty ratio of states

$$d^{ijk}, \quad \text{where } i \neq j \neq k \quad \text{and} \quad i,j,k \in \{-1,0,1\}. \tag{10}$$

Thus, within each sector an expression for the stack currents can be written explicitly, leading to piecewise-linear functions that describe their average time-domain behavior. From this, the low-frequency variation of the dc stack and the harmonic spectrum of the three stack currents can also be evaluated. The dc component of the neutral-point current is zero for equal sharing between redundant states. It is also observed that the dominant harmonic in the neutral-point current is the third harmonic of the fundamental output frequency. The total low-frequency harmonic content of the neutral-point current determined using (4) is plotted as a three-dimensional surface function of the modulation index and power factor as shown in Fig. 5.

IV. Radial State Space-Vector Modulator

It has been shown that switching states where the three throws comprising the ac terminals are connected to three different stack levels of the dc bus are the primary cause of

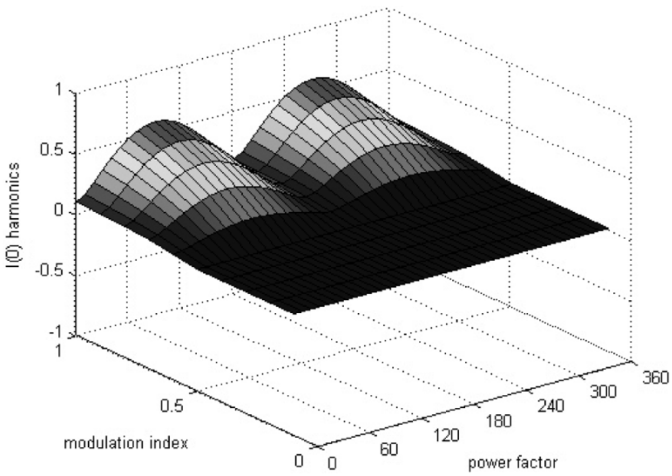

Fig. 5. Three-dimensional surface plot of total neutral-point current harmonic content numerically evaluated using averaged modeling with classical SVM using (4).

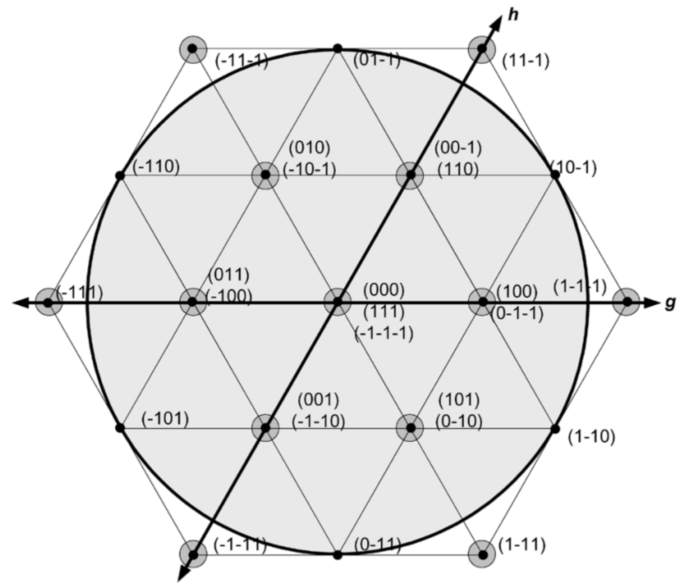

Fig. 6. Allowed switching states using RSS algorithm.

increased harmonic content in the dc-bus currents [11]. Based on this knowledge, a radial state space-vector modulation strategy (RSS) that redistributes the duty cycles of these states has been developed [8]. This strategy completely eliminates the low-frequency harmonic content of the neutral-point current in a three-level diode-clamped converter. The dc-link capacitors can be significantly smaller as they only have to support the high-frequency switching ripple of the converter.

It can be deduced that identical line-to-line voltages can be generated if the duty cycle of these states is distributed equally over the two states that are adjacent to it, but lie on radii emanating from the zero state, For example, in the sector in Fig. 4, the duty cycles can be modified as follows:

$$\begin{aligned} d_{\mathrm{RSS}}^{1-1-1}(t) &= d_{\mathrm{NTV}}^{1-1-1}(t) + \frac{d_{\mathrm{NTV}}^{10-1}(t)}{2} \\ d_{\mathrm{RSS}}^{11-1}(t) &= d_{\mathrm{NTV}}^{11-1}(t) + \frac{d_{\mathrm{NTV}}^{10-1}(t)}{2} \\ d_{\mathrm{RSS}}^{10-1}(t) &= 0 \end{aligned} \tag{11}$$

where d_{RSS} refers to the duty cycles of the RSS modulator while d_{NTV} refers to the duty cycles generated by the NTV modulator. From (11) and (8), the neutral-point current is reduced to zero in the sector of Fig. 4. Similar alterations to duty cycles can be carried out for all the other sectors, eliminating the low-frequency harmonics in the neutral-point current leaving only switching harmonics. The states that are used by the RSS modulation are shown circled in Fig. 6.

It can be noted that the dc-bus utilization using RSS modulation is identical to the NTV modulator, as the hexagons and the inscribed circles are identical. However, the adjacent switching behavior of the NTV modulator is somewhat compromised as six intermediate states are removed from the available choices. The low-frequency harmonic content of the neutral-point current determined using (4) is plotted as a three-dimensional surface function of the modulation index and power factor in Fig. 7 and is seen to be identically zero.

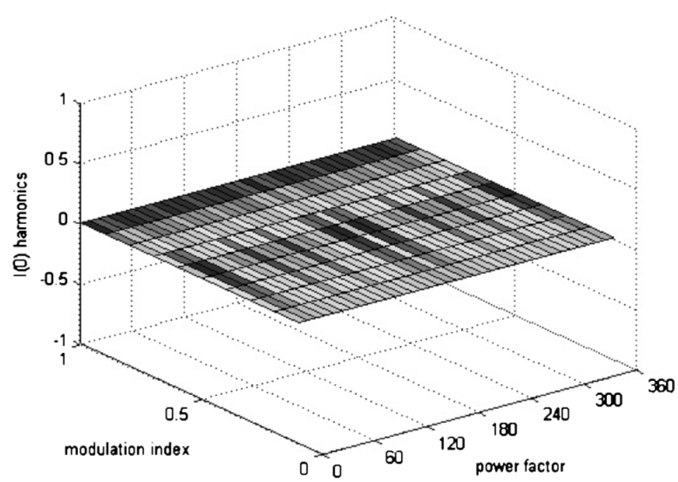

Fig. 7. Three-dimensional surface plot of total neutral-point current harmonic content numerically evaluated using averaged modeling with RSS modulation using (4).

V. Zero Common-Mode Voltage Modulator

From Fig. 3 and (4) the common-mode voltages associated with the various states in the diagram can be calculated and are shown in the second column of Table I. It is seen that seven states in the three-level converter switching diagram generate common-mode voltage that is dependent only on V_0, which is a measure of the unbalance between the dc buses.

The common-mode voltage generated for $V_{\mathrm{DC}} = 1$ p.u. and perfectly balanced dc buses $(V_0 = 0)$ is shown in the third column of Table I. The seven states with low common-mode voltage are highlighted in Table I and identified in the switching state diagram of Fig. 8.

If only these states are used and all the remaining states are excluded from the three-level converter switching strategy, no common-mode voltage will be generated. Clearly, the peak

TABLE I
COMMON-MODE VOLTAGE FOR SWITCHING STATES

State	CM voltage	CM voltage V_{DC}~1pu V_0~0
-1-1-1	$-\frac{V_{DC}}{2}$	$-\frac{1}{2}$
-1-10	$-\frac{1}{3}V_{DC}+\frac{1}{3}V_0$	$-\frac{1}{3}$
-1-11	$-\frac{1}{3}\frac{V_{DC}}{2}$	$-\frac{1}{6}$
-10-1	$-\frac{1}{3}V_{DC}+\frac{1}{3}V_0$	$-\frac{1}{3}$
-100	$-\frac{1}{6}V_{DC}+\frac{2}{3}V_0$	$-\frac{1}{6}$
-101	$\frac{1}{3}V_0$	0
-11-1	$-\frac{1}{3}\frac{V_{DC}}{2}$	$-\frac{1}{6}$
-110	$\frac{1}{3}V_0$	0
-111	$\frac{1}{3}\frac{V_{DC}}{2}$	$+\frac{1}{6}$
0-1-1	$-\frac{1}{3}V_{DC}+\frac{1}{3}V_0$	$-\frac{1}{3}$
0-10	$-\frac{1}{6}V_{DC}+\frac{2}{3}V_0$	$-\frac{1}{6}$
0-11	$\frac{1}{3}V_0$	0
00-1	$-\frac{1}{6}V_{DC}+\frac{2}{3}V_0$	$-\frac{1}{6}$
000	V_0	0
001	$\frac{1}{6}V_{DC}+\frac{2}{3}V_0$	$+\frac{1}{6}$
01-1	$\frac{1}{3}V_0$	0
010	$\frac{1}{6}V_{DC}+\frac{2}{3}V_0$	$+\frac{1}{6}$
011	$\frac{1}{3}V_{DC}+\frac{1}{3}V_0$	$+\frac{1}{3}$
1-1-1	$-\frac{1}{3}\frac{V_{DC}}{2}$	$-\frac{1}{6}$
1-10	$\frac{1}{3}V_0$	0
1-11	$\frac{1}{3}\frac{V_{DC}}{2}$	$+\frac{1}{6}$
10-1	$\frac{1}{3}V_0$	0
100	$\frac{1}{6}V_{DC}+\frac{2}{3}V_0$	$+\frac{1}{6}$
101	$\frac{1}{3}V_{DC}+\frac{1}{3}V_0$	$+\frac{1}{3}$
11-1	$\frac{1}{3}\frac{V_{DC}}{2}$	$+\frac{1}{6}$
110	$\frac{1}{3}V_{DC}+\frac{1}{3}V_0$	$+\frac{1}{3}$
111	$\frac{V_{DC}}{2}$	$+\frac{1}{2}$

attainable voltage magnitude will be limited to the inscribed circle in the hexagon created by these six zero common-mode (ZCM) states as shown in Fig. 8. The bus utilization achieved by the ZCM voltage modulator can be geometrically shown to be 86.6% of the utilization of the NTV modulator. Furthermore, it can be noted that the state selection is no longer carried out on an adjacent state basis, which leads to higher ripple and harmonic distortion in the output voltage and current. As the common-mode voltage is directly proportional to the neutral-point voltage, any neutral-point current harmonics will be observed in the output common-mode voltage.

Four metrics: pole-to-pole voltage, neutral-point current, common-mode voltage, and dc-bus utilization can be used to rate the performance of the three modulation strategies.

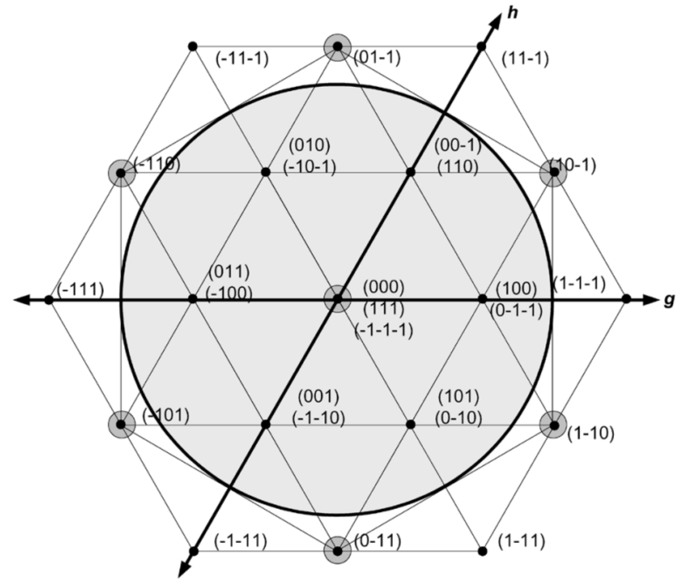

Fig. 8. ZCM modulator states.

TABLE II
PARAMETERS FOR THREE-LEVEL INVERTER SYSTEM SIMULATION

Parameter	Value
Filter Inductance	1mH
Filter capacitance	30μF
Load Resistance	18.2 Ω
DC Link Voltage	750 V
DC bus capacitance	180 μF
Switching frequency	5 kHz
Modulation level	0.78
Output voltage (l-l rms)	412 V
Deadtime	3μs
Output frequency	60Hz

VI. SIMULATION RESULTS

Extensive MATLAB Simulink models of three-level inverter systems were developed for analyzing the effects of NTV, RSS, and ZCM space-vector modulation on neutral-point current, common-mode voltage, and output pole–pole voltage. The parameters used for the simulation model of the three-level converter system are shown in Table II. To facilitate the comparison of results for the various modulators, a modulation index of 0.78 (412 V_{L-L} rms) in the linear modulation region of the ZCM modulator is used.

A. Output Voltage

Figs. 9 and 10 show the time-domain waveforms and the spectral content of the pole-to-pole voltage of the converter for all three modulators. Adjacent state switching is observed always for NTV modulation and never for ZCM modulation. It is lost during segments of the cycle for RSS modulation. This is reflected in the spectral plots, which show that the harmonic content at the switching frequency to be nonexistent for the NTV modulator, moderate for the RSS modulator, and very high for the ZCM modulator.

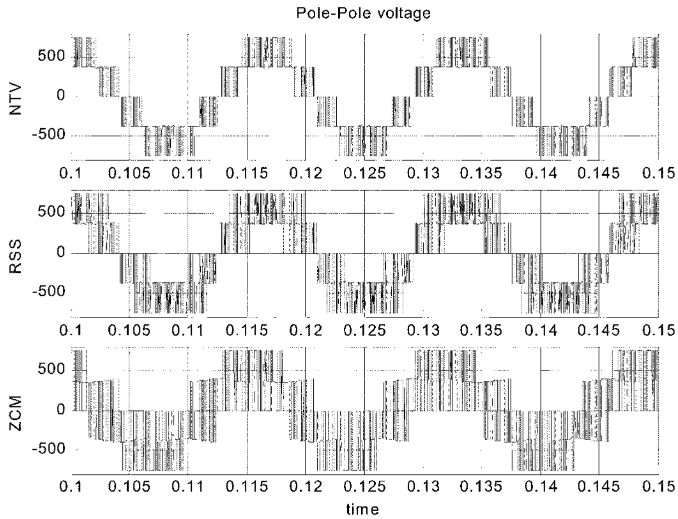

Fig. 9. Simulation results showing time-domain pole–pole voltage waveforms for NTV, RSS, and ZCM modulators, respectively.

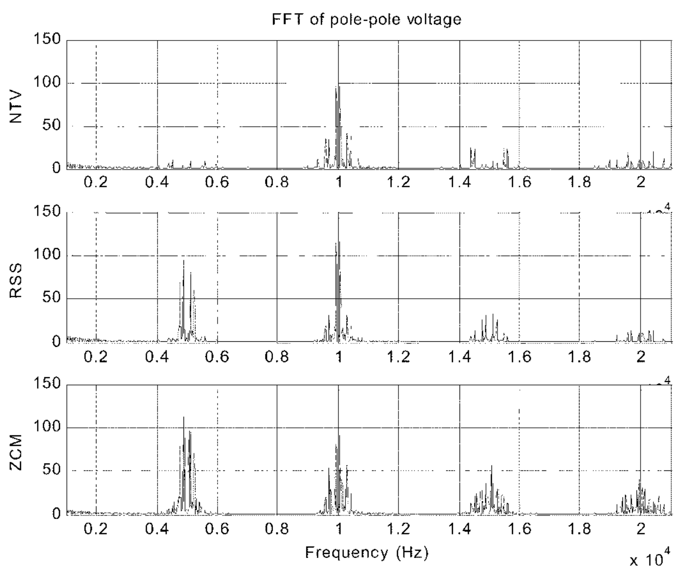

Fig. 10. Simulation results showing frequency-domain spectrum of pole–pole voltage for NTV, RSS, and ZCM modulators, respectively.

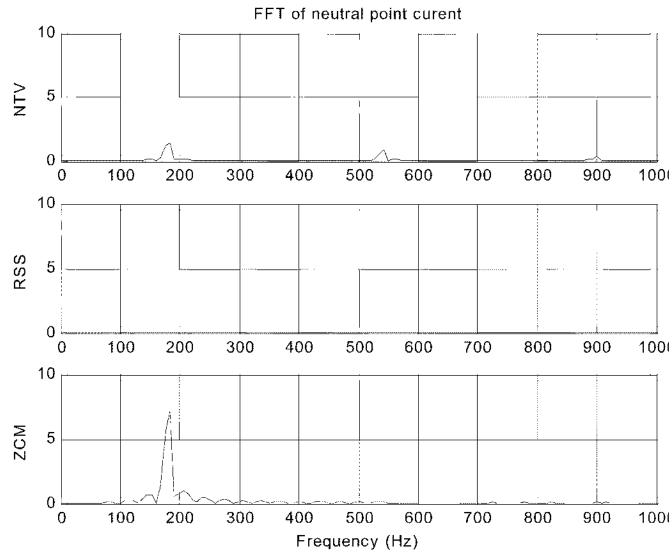

Fig. 11. Simulation results showing frequency-domain neutral-point current waveforms for NTV, RSS, and ZCM modulators, respectively.

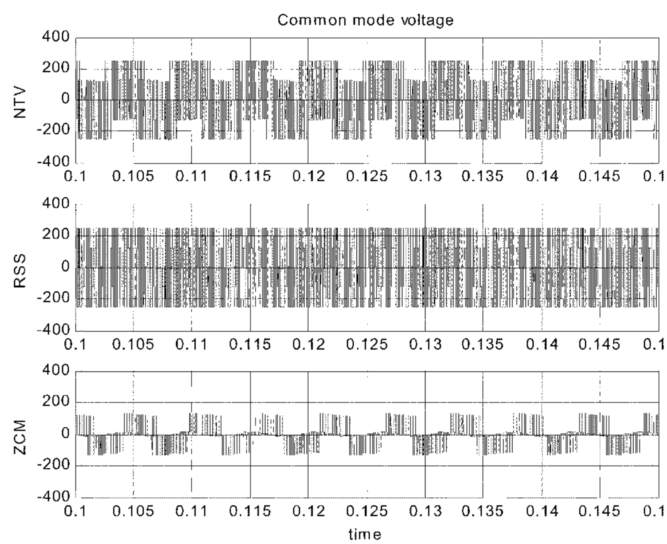

Fig. 12. Simulation results showing time-domain common-mode voltage waveforms for NTV, RSS, and ZCM modulators, respectively.

B. Neutral-Point Current

Fig. 11 shows the neutral-point current spectra for the three modulation strategies, respectively. The ZCM modulator shows a very high neutral-point current at the third harmonic of the fundamental. The NTV modulator produces much lower levels of this low-frequency harmonic current, while the RSS modulator completely eliminates it.

C. Common-Mode Voltage

Figs. 12 and 13 show the waveforms of the common-mode voltage and its spectra for the three modulation strategies, respectively. It can be observed that the ZCM modulator produces very low common-mode voltage, when compared to the other two strategies. In fact, if the deadtime effects are ignored, the common voltage generated is identically zero. The RSS modulator produces slightly more common-mode voltage at the switching frequency than the NTV modulator, as can be observed from the figures.

VII. Experimental Results

A hardware prototype was built to verify the analysis and simulation results obtained using the various modulators discussed previously. The prototype used nine dual insulated gate bipolar transistors (IGBT) devices and nonpolar film capacitors interconnected with laminated bus planes to create a three-phase three-level inverter power platform. A schematic of the power section of the prototype is shown in Fig. 14. A listing of the key parameters of the hardware prototype may be found in Table III.

Experimental measurements of time-domain waveforms and spectral content of the pole-to-pole voltage for the NTV, RSS,

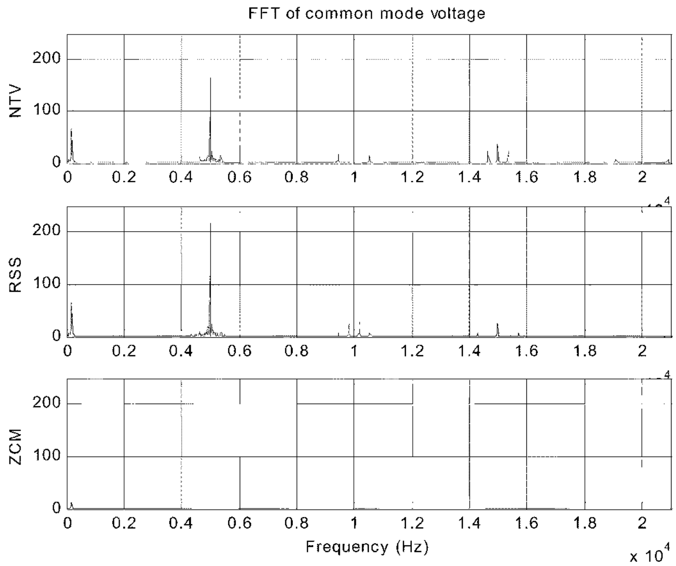

Fig. 13. Simulation results showing frequency-domain spectrum of common-mode voltage for NTV, RSS, and ZCM modulators, respectively.

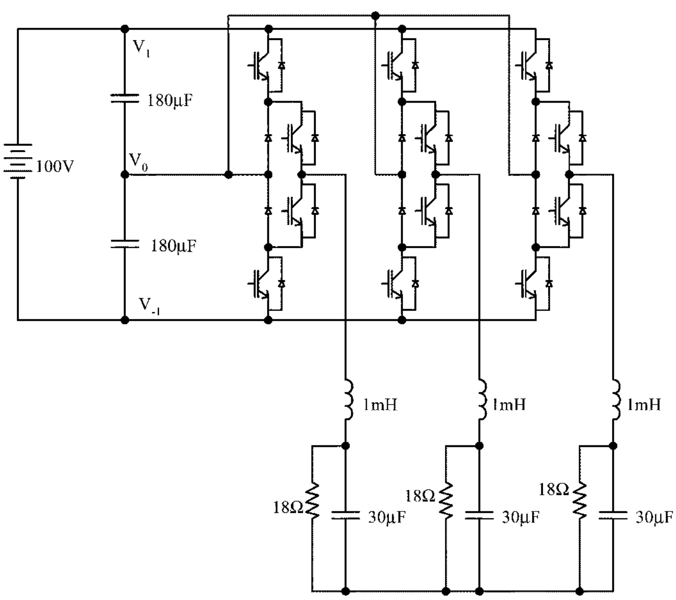

Fig. 14. Schematic of the power section of the prototype.

TABLE III
PARAMETERS FOR THREE-LEVEL INVERTER SYSTEM EXPERIMENTS

Parameter	Value
Filter Inductance	1mH
Filter capacitance	30μF
Load Resistance	18.2 Ω
DC Link Voltage	100 V
DC bus capacitance	90 μF
Switching frequency	5 kHz
Modulation level	0.78
Output voltage (l-l rms)	55 V
Deadtime	3μs
Output frequency	60Hz

and ZCM modulators are shown in Figs. 15–17, respectively. The NTV modulator features the most desirable harmonic spectrum consisting of switching frequency content at higher frequencies.

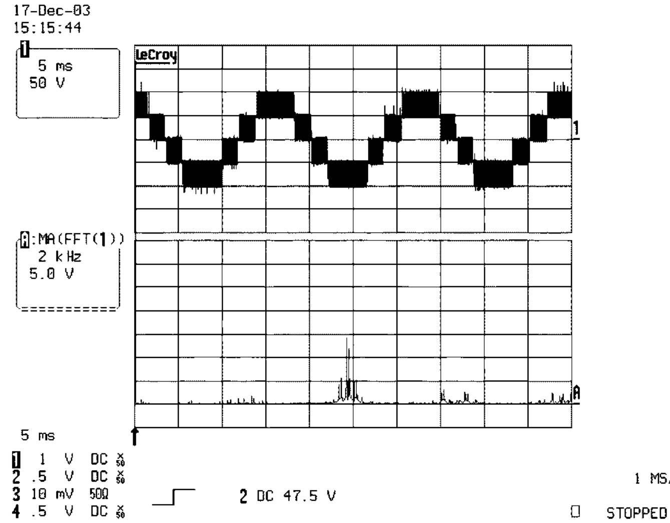

Fig. 15. Pole-to-pole voltage (50 V/div) and its spectrum (2 kHz/div) for NTV modulation.

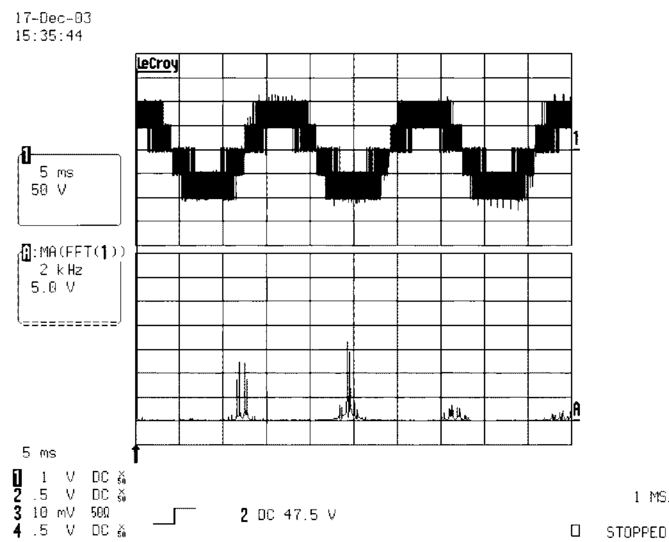

Fig. 16. Pole to pole voltage (50 V/div.) and its spectrum (2 kHz/div.) for RSS modulation.

Experimental measurements of time-domain waveforms and spectral content of neutral-point current for the NTV, RSS, and ZCM modulators are shown in Figs. 18–20, respectively. The RSS modulator features the most desirable performance consisting of negligible low-frequency neutral currents.

Experimental measurements of time-domain waveforms and spectral content common-mode voltage for the NTV, RSS, and ZCM modulators are shown in Figs. 21–23, respectively. The ZCM modulator features the most desirable performance in this case.

An excellent qualitative match can be observed between the analytical predictions, simulation results, and measured data. Each modulator achieves its primary function very well, with significant degradation in performance with respect to the other metrics. A qualitative comparison of the performance of the three modulators based on the experimental observations is presented in Table IV.

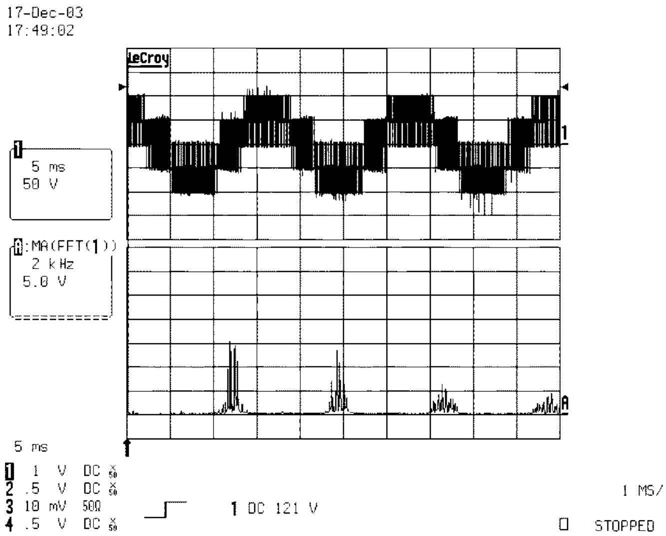

Fig. 17. Pole-to-pole voltage (50 V/div) and its spectrum (2 kHz/div) for ZCM modulation.

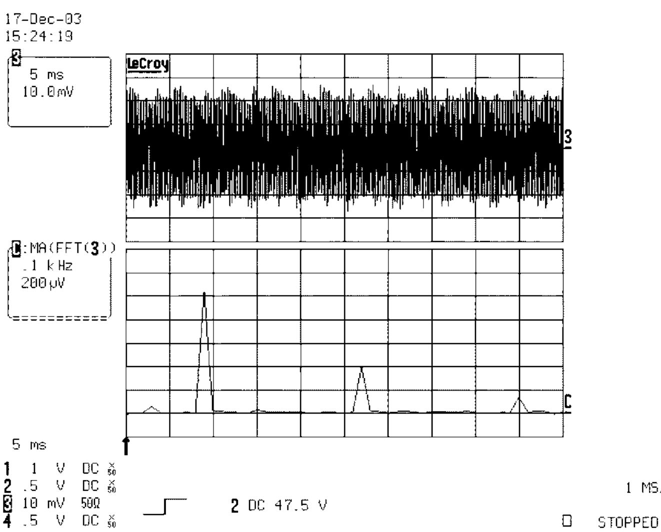

Fig. 18. Neutral-point current (2 A/div) and its spectrum (100 Hz/div) for NTV modulation.

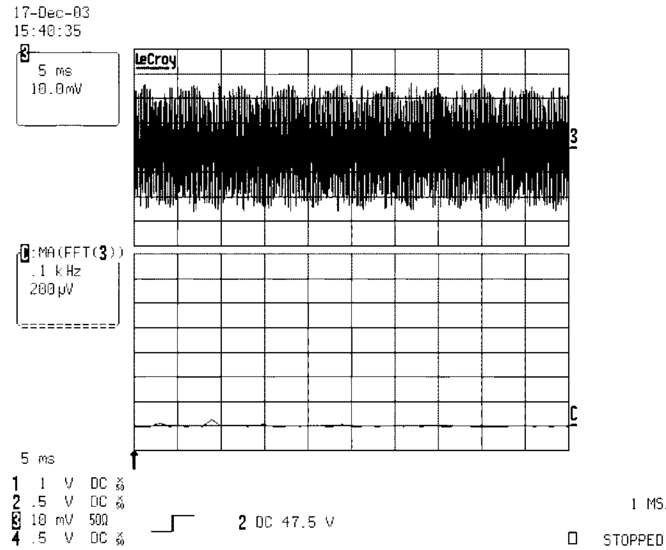

Fig. 19. Neutral-point current (2 A/div) and its spectrum (100 Hz/div) for RSS modulation.

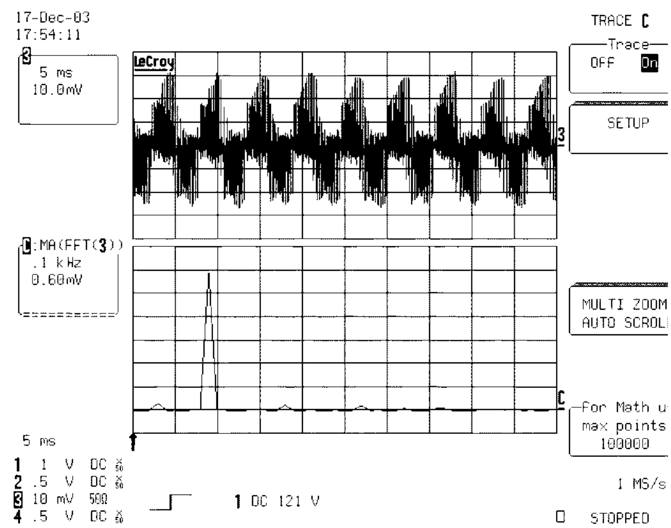

Fig. 20. Neutral-point current (2 A/div) and its spectrum (100 Hz/div) for ZCM modulation.

VIII. Conclusion

This paper has compared the performance of three space-vector modulation methods for three-level diode-clamped converters. The performance objectives of the three modulators are very different and this is clearly reflected in the results. The NTV modulator provides very low pole–pole voltage THD, the RSS modulator eliminates low-frequency neutral-point current while the ZCM modulator reduces the switching frequency harmonics of the common-mode voltage. Clearly, if any of these three goals is absolutely necessary for a given application, the choice of modulator is straightforward, and the loss of performance in other metrics can be tolerated. However, when a general solution that can be applied with acceptable performance across all metrics is desired the choice is more complicated.

The ZCM modulator has clear deficiencies as it rates poorly in all other metrics except the common-mode voltage. Furthermore, though the switching frequency content of the common-mode voltage is reduced, high dv/dt pulses are seen in the common-mode voltage due to the presence of deadtime. Deadtime compensation strategies can be useful for mitigation of low-frequency errors in the modulation process. However, the deadtime effects that lead to nonzero common-mode voltage with the ZCM modulator are a high-frequency phenomena and cannot be actively controlled using deadtime compensators. Thus, a common-mode filter will be required for converter systems with this modulator in place, if MIL-STD-461 needs to be met. The NTV modulator and the RSS modulator are very close in common-mode voltage (RSS is 30% worse), have identical bus utilization, and have very similar output voltage harmonics (RSS is slightly worse). However, there is a huge improvement in the neutral-point current harmonic content with the RSS modulator. This reduction can allow the use of film-type long-life capacitors, instead of electrolytic capacitors, prolonging the mean time between failures (MTBF), durability,

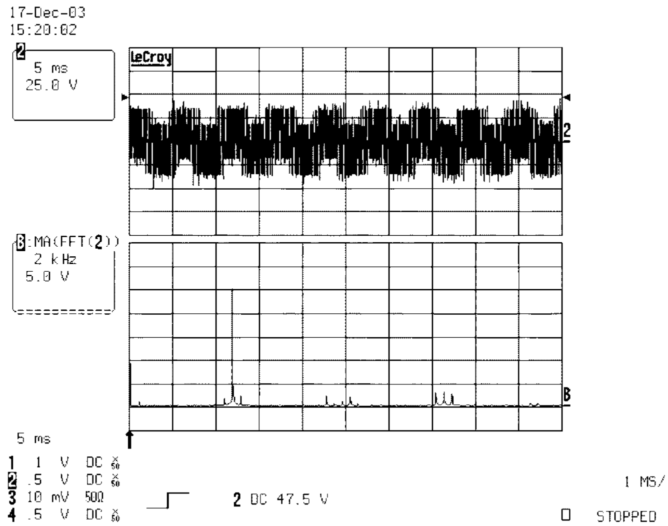

Fig. 21. Common-mode voltage (25 V/div) and its spectrum (2 kHz/div) for NTV modulation.

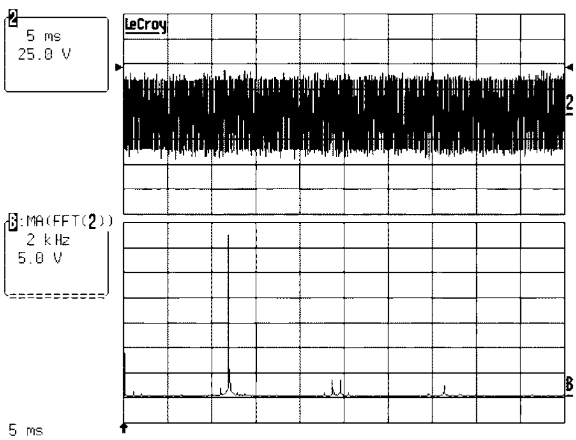

Fig. 22. Common-mode voltage (25 V/div) and its spectrum (2 kHz/div) for RSS modulation.

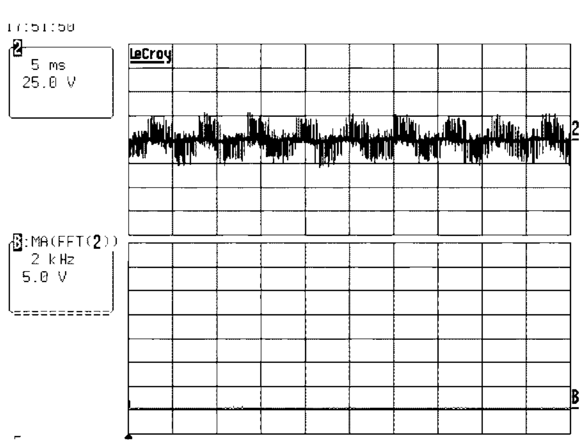

Fig. 23. Common-mode voltage (25 V/div) and its spectrum (2 kHz/div) for ZCM modulation.

and reliability, while reducing converter size. As a general-purpose modulator algorithm, RSS modulation appears to provide the best tradeoffs, as it satisfies its primary goal of neutral-point current harmonic elimination without severely compromising the other metrics.

TABLE IV
COMPARISON OF MODULATOR PERFORMANCE

	NTV	RSS	ZCM
Pole-Pole Voltage	Best	Moderate	Poor
Neutral point current	Moderate	Best	Poor
Common mode voltage	Moderate	Moderate	Best
Bus utilization	Full	Full	Moderate

REFERENCES

[1] B. P. Schmitt and R. Sommer, "Retrofit of fixed speed induction motors with medium voltage drive converters using NPC three-level inverter high-voltage IGBT based topology," in *Proc. IEEE Int. Symp. Industrial Electronics*, vol. 2, 2001, pp. 746–751.

[2] J. K. Steinke and P. K. Steimer, "Medium voltage drive converter for industrial applications in the power range from 0.5 MW to 5 MW based on a three-level converter equipped with IGCTs," in *Proc. IEE Seminar PWM Medium Voltage Drives*, 2000, pp. 6/1–6/4.

[3] G. Carrara, S. Gardella, M. Marchesoni, R. Salutari, and G. Sciutto, "A new multilevel PWM method: A theoretical analysis," *IEEE Trans. Power Electron.*, vol. 7, no. 3, pp. 497–505, Jul. 1992.

[4] N. Celanovic and D. Boroyevich, "A fast space-vector modulation algorithm for multilevel three-phase converters," *IEEE Trans. Ind. Appl.*, vol. 37, no. 2, pp. 637–641, Mar./Apr. 2001.

[5] Y.-H. Lee, R.-Y. Kim, and D.-S. Hyun, "A novel SVPWM strategy considering DC-link balancing for a multi-level voltage source inverter," in *Proc. 14th Annu. Applied Power Electronics Conf. Exposition*, vol. 1, 1999, pp. 509–514.

[6] G. Venkataramanan and A. Bendre, "Reciprocity-transposition-based sinusoidal pulsewidth modulation for diode-clamped multilevel converters," *IEEE Trans. Indu. Electron.*, vol. 49, no. 5, pp. 1035–1047, Oct. 2002.

[7] A. Bendre and G. Venkataramanan, " Modeling and design of a neutral point regulator for a three level diode clamped rectifier," in *Conf. Rec. IEEE-IAS Annu. Meeting*, vol. 3, 2003, pp. 1758–1765.

[8] ——, "Radial state space vector modulation—A new space vector technique for reducing dc link capacitor harmonic currents in three level converters," in *Conf. Rec. IEEE-IAS Annu. Meeting*, vol. 1, 2003, pp. 684–691.

[9] P. Loh, G. Holmes, Y. Fukuta, and T. Lipo, "Reduced common mode carrier-based modulation strategies for cascaded multilevel inverters," in *Conf. Rec. IEEE-IAS Annu. Meeting*, vol. 3, 2002, pp. 2002–2009.

[10] A. von Jouanne, S. Dai, and H. Zhang, "A multilevel inverter approach providing DC-link balancing, ride-through enhancement and common-mode voltage elimination," *IEEE Trans. Ind. Electron.*, vol. 49, no. 4, pp. 739–745, Aug. 2002.

[11] N. Celanovic, I. Celanovic, and D. Boroyevich, "The feedforward method of controlling three-level diode clamped converters with small DC-link capacitors," in *Proc. IEEE PESC'01*, vol. 3, 2001, pp. 1357–1362.

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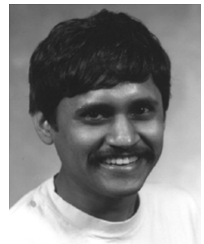

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