Comparative Evaluation of Multi-Loop Control Schemes for a High-Bandwidth AC Power Source with a Two-Stage *LC* Output Filter

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***Abstract*—This paper presents a comparative evaluation of four different multi-loop control schemes for a high-bandwidth AC power source. The power source considered in this work is based on a three-level T-type inverter with a two-stage *LC* output filter. The control schemes evaluated in this paper have an output voltage controller in the outer loop. For the inner control loop the following options are evaluated: capacitor current feedbacks, proportional-integral and proportional inverter output current control in combination with reference voltage and load current feedforward, and first *LC* stage capacitor voltage and inverter output current feedback.**

The reference tracking capabilities as well as the power source output impedance are evaluated. Analytical and simulation results are shown to be in very good agreement, and the frequency and step responses for the different control schemes are compared.

The results show that a cascaded structure consisting of a proportional-integral controller for the output voltage and a proportional controller for the inverter output current allows to achieve the best dynamic behavior in terms of output voltage control bandwidth and output impedance.

Keywords — AC source, high-bandwidth, two-stage LC filter, multi-loop control, capacitor current feedback.

I. Introduction

A high-bandwidth power source is the preferred option for testing new power electronic converters [1]–[3]. It allows to test different operating conditions like the presence of harmonics and step changes in the supply voltage. These kind of tests make possible to verify the compliance to specifications and standards, as described in [1]–[5].

A 10 kW three-phase power source is considered in this work. For a better handling of single-phase loads, each phase of the converter is controlled independently. Consequently, for the controller adjustment and the comparative results presented in this paper only one phase of the system is considered. The power source is composed of a three-level T-type converter and a two-stage LC filter with a passive damping circuit of the second stage, as shown in **Fig. 1**. The filter structure is briefly discussed in Section II.

Several control schemes have been proposed for power sources with a single-stage LC output filter. The use of a multi-loop structure is the most common choice for these kind of converters [6], [7]. However, there are many options in the selection of the feedback variables and in the type of the controller used in each loop. The use of more advanced control schemes like model predictive control has also been evaluated [8]. A dynamic control of the switching frequency has been proposed in [9] to improve the dynamic performance of the power converter.

As explained in [10], the addition of a second LC stage to the output filter affects the behavior of the output voltage control and the output impedance of the power source. A second filter stage is required in order to increase the attenuation of the switching high frequency harmonics without significantly reducing the filter dynamics. This imposes a higher complexity in the design of a high performance control scheme. Most of the published works deal with the control of converters with a single stage filter. Control schemes for converters with a two-stage filter have not been well analyzed in the literature.

Four different multi-loop control schemes for the AC power source are evaluated in this paper. The effect of the second filter stage on the output voltage dynamics and attenuation of high frequency harmonics is discussed in **Section II**. The control structures, their design and achieved performance are explained in **Section III**. Then, comparative simulation results are presented in **Section IV**, considering the frequency and step responses for the different control schemes. The control bandwidth of the output voltage and the output impedance of the system are the main performance indexes considered for comparison. Finally, the selection of the control scheme

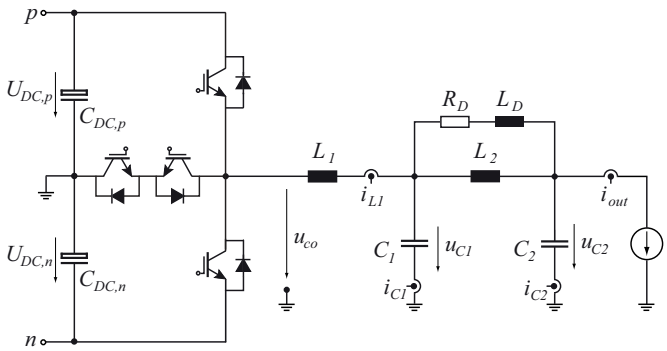


Fig. 1 Three-level T-type converter with a two-stage output LC filter.

that achieves the best performance indexes and future research topics are discussed in **Section V**.

II. Two-Stages LC Output Filter

The design of the output filter for a high-bandwidth AC power source has been studied in [11]. For a single-stage LC filter design there is a trade-off between the requirements in dynamics of the output voltage and the attenuation of high frequency harmonics in the output voltage. If the filter is designed for fast dynamics, as required for a high-bandwidth control of the output voltage, the required attenuation of high switching frequency harmonics might not be achieved. In this paper, the standard for conducted emission levels according to IEC/EN 55011 Class A is considered. The inclusion of a second LC stage allows to increase the attenuation of high frequency harmonics without reducing the filter dynamics significantly.

Usually a two-stage LC filter for switched mode AC power sources shows different inductance values for the two stages, thus L_1 is normally one order of magnitude higher in inductance value than L_2 (cf. **Fig. 1** and **Table I**). The reasons are: firstly, the inductance L_1 of the first filter stage is selected to be reasonably high in order to limit the inverter output peak-to-peak current ripple. Secondly, the inductance L_2 of the second filter stage is designed to achieve a reasonably low value as a compromise between an increased additional attenuation of high frequency harmonics and a reduced phase-shift between the first stage capacitor voltage u_{C1} and the second stage capacitor voltage u_{C2}. Furthermore, considering the output voltage dynamics and the output impedance of the converter with the two-stage LC filter, the first filter stage capacitor C_1 and second filter stage capacitance C_2 are in the same order of magnitude (cf. **Fig. 1**). Consequently, the characteristic impedance

$$Z_0 = \sqrt{\frac{L}{C}} \tag{1}$$

of the first filter stage L_1C_1 is higher than the one of the second filter stage L_2C_2.

It is remarked, that if a single LC filter stage is "distributed" to n LC filter stages of *equal* component ratings (L/n, C/n) [12], finally a lossless transmission line equivalent circuit model is obtained for $n \to \infty$. Such a circuitry would, however, no longer show a low-pass filter characteristic, which is required regarding conducted EMI noise suppression. Furthermore, the characteristic impedance of such a transmission line would be symmetrical which may be too low considering the inverter output peak-to-peak current ripple but too high regarding the filter output impedance seen by the load. As a consequence, multi-stage LC filters are usually dimensioned such that the characteristic impedances $Z_{0,i}$ of the individual stages i are lowered from the filter input side towards the output side.

In **Fig. 2** the transfer functions of the undamped and the damped two-stage LC filter considered in this paper (cf. **Fig. 1**) are plotted for the filter parameters given in **Table I**.

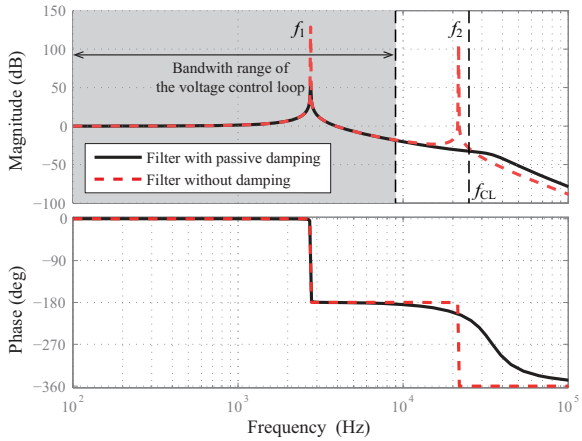


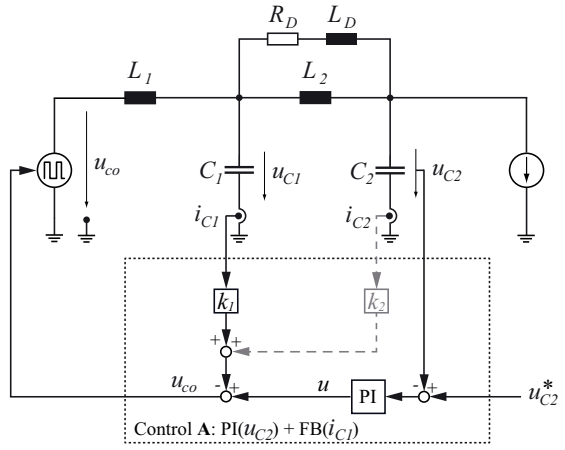
Fig. 2 Bode plot of the two-stages LC filter with and without the damping circuit shown in **Fig. 1** and filter parameters of **Table I**. The bandwidth of the current control loop is indicated with a dashed line at f_{CL}.

A straight forward approach to control a two-stage LC filter, derived from the classical control structure for a single-stage LC filter [6], is to employ a cascaded control structure with an inner inverter output current i_{L1} and an outer output voltage u_{C2} control loop (cf. **Section III.B** and **Section III.C**). In order to actively damp the resonance of the first filter stage at f_1, the inverter output current control loop bandwidth must be higher than f_1. Analogous, the resonance of the second filter stage at f_2 can only be actively damped if the output voltage control loop bandwidth is higher than f_2. The closed-loop bandwidth (-3dB) of the output voltage u_{C2} and the inverter output current i_{L1} control loops designed in this paper are indicated in **Fig. 2**. Concluding, as can be seen from **Fig. 2**, the first filter stage resonance can be damped by means of the current control loop. Furthermore, the output voltage control loop bandwidth is clearly not high enough to damp the resonance of the second filter stage, mainly because of the high Z_0 (inductor L_1) of the first filter stage. Thus, the second filter stage is passively damped by a parallel RL damping branch, which constitutes a low cost option to achieve the damping. As can be observed in **Fig. 2**, the resonance of the second stage is properly damped.

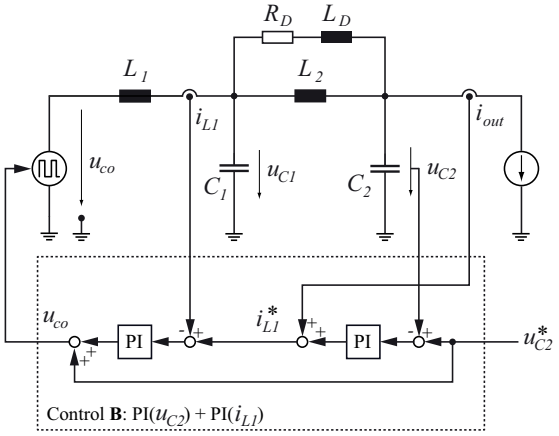
III. Multi-Loop Control schemes

The following control schemes with different numbers of control loops are evaluated and compared in this paper:

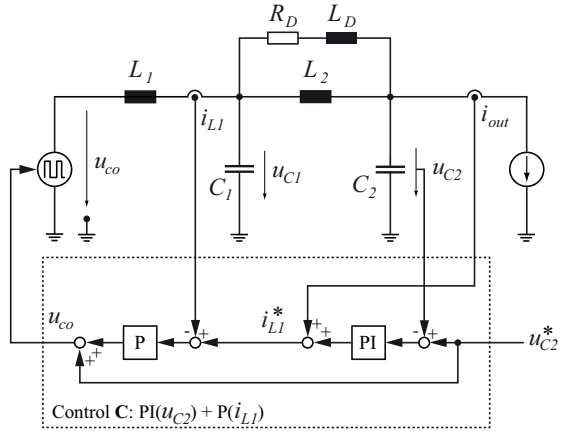
- **A. PI(u_{C2})+FB(i_{C1})**: proportional-integral (PI) controller for the outer voltage control loop and feedback (FB) of the capacitor current i_{C1} providing active damping of the filter resonance [cf. **Fig. 3(a)**]. The capacitor current feedback emulates the behavior of a damping resistor in the first stage of the filter.
- **B. PI(u_{C2})+PI(i_{L1})**: PI controller for the outer voltage control loop and PI controller for the inverter output current i_{L1} in the inner loop. Feedforward loops for the load



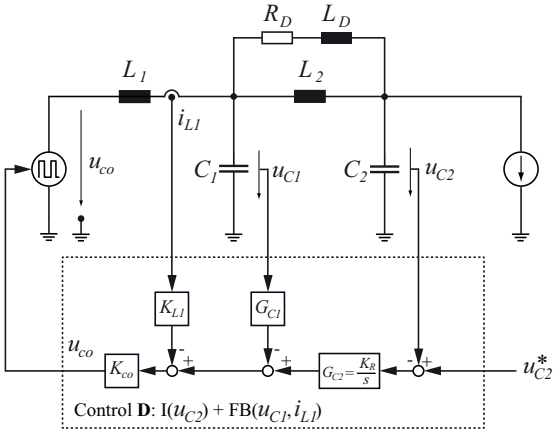
(a) Cascaded control scheme with one PI controller for the output voltage and feedback of first stage filter capacitor current, PI(u_{C2})+FB(i_{C1}).



(b) Cascaded control scheme with two PI controllers, one for the output voltage and one for the inverter output current, PI(u_{C2})+PI(i_{L1}).



(c) Cascaded control scheme with one PI voltage controller for the output voltage and one proportional inverter output current controller, PI(u_{C2})+P(i_{L1}).



(d) Three-loop control scheme: output voltage loop, first filter stage capacitor voltage loop and inverter output current loop, I(u_{C2})+FB(u_{C1},i_{L1}).

Fig. 3 Control schemes for the AC power source.

current i_{out} and the reference voltage u^*_{C2} are included [cf. **Fig. 3(b)**].

C. PI(u_{C2})+P(i_{L1}): PI controller for the outer voltage control loop and proportional (P) controller for the inverter output current in the inner loop. Feedforward loops for the output current and reference voltage are included [cf. **Fig. 3(c)**].

D. I(u_{C2})+FB(u_{C1}, i_{L1}): integral (I) controller for the outer voltage control loop and two inner feedback loops, one for the voltage across the capacitor C_1 of the first filter stage, u_{C1}, and one for the inverter output current i_{L1} [cf. **Fig. 3(d)**].

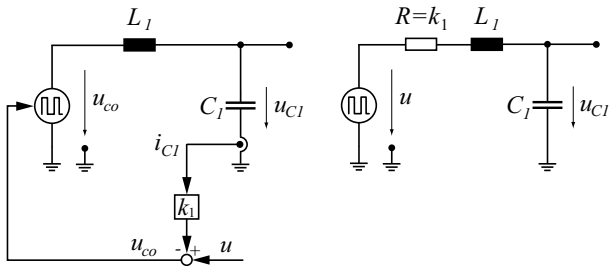
These control schemes can be classified into three groups according to the number of control loops. The PI(u_{C2})+FB(i_{C1}) scheme can be considered as single-loop control, with only one voltage controller for an actively damped filter. The PI(u_{C2})+PI(i_{L1}) and PI(u_{C2})+P(i_{L1}) schemes correspond to a two-loop structure, with one control loop for the output voltage and one control loop for the inverter output current. The I(u_{C2})+FB(u_{C1}, i_{L1}) scheme is a three-loop structure with an external output voltage control loop and two internal feedback loops.

In order to compare the different control schemes under similar conditions, the voltage controllers have been adjusted to obtain the fastest possible response with the limitation of a maximum overshoot of 10 % in the output voltage u_{C2} under different load conditions.

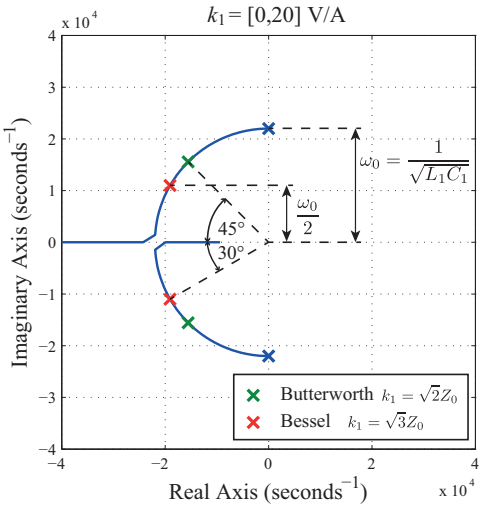
A. PI voltage control and capacitor current feedback [PI(u_{C2})+FB(i_{C1})]

The structure of this controller considers a single PI controller for the output voltage and an active damping of the first filter stage using the capacitor current i_{C1}. A block diagram of this scheme is shown in **Fig. 3(a)**.

A single voltage control loop achieves no damping of the first filter stage. The resonance must be damped by using passive elements in the circuit (as for the second filter stage) or actively, as shown in **Fig. 4(a)**.



(a) LC filter with current feedback. (b) Equivalent circuit.



(c) Filter poles.

Fig. 4 Poles of a single-stage LC filter for different values of the capacitor current feedback gain k_1.

The feedback gain k_1 can be adjusted to obtain the desired behavior of the filter. If only the first filter stage is considered, the effect of k_1 is identical to the effect of a resistance R in series with the inductor L_1 (cf. **Fig. 4(a)** and **Fig. 4(b)**). However, the use of a current feedback loop only emulates the resistive behavior but does not generate the power losses of an actual resistor added in series to the filter. By adjusting k_1 the filter can present a Butterworth or a Bessel response, as shown in **Fig. 4(c)**, or other type of filter response. For a Butterworth response, a feedback gain $k_1 = \sqrt{2}Z_0$ must be used, while for a Bessel response, a higher gain $k_1 = \sqrt{3}Z_0$ is required.

Furthermore, the transfer function of a single-stage filter with a capacitor current feedback gain k_1 can be compared to the response of a filter with two real poles:

$$G_f(s) = \frac{1}{1 + sk_1C_1 + s^2L_1C_1} \tag{2}$$

$$\triangleq \frac{1}{(1+sTn)(1+sT/n)} = \frac{1}{1+sT(n+1/n)+s^2T^2}, \tag{3}$$

where $T \triangleq \sqrt{L_1C_1}$ and n is a design parameter that represents the separation of the filter poles and defines the dynamics of the filter. Then, the filter gain can be expressed in terms of n

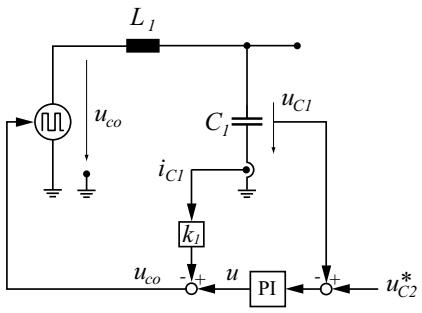


Fig. 5 Output voltage control with a single-stage filter.

and the filter parameters

$$k_1 = \sqrt{\frac{L_1}{C_1}}(n + 1/n). \tag{4}$$

Considering this filter design, a PI controller (cf. **Fig. 5**) can be designed for compensation of the slow pole of the filter,

$$G_{PI}(s) = \frac{1+sTn}{sTn}; \tag{5}$$

the resulting closed loop transfer function from the reference to the output voltage is then

$$G_o(s) = \frac{G_{PI}(s)G_f(s)}{1+G_{PI}(s)G_f(s)} = \frac{1}{1+sTn+s^2T^2}, \tag{6}$$

which corresponds to a second order filter with a damping factor n and a cut-off frequency $1/T$. In this way, n is adjusted to obtain the desired behavior.

As mentioned in the previous section, the overshoot in the output voltage is limited to a maximum value of 10 %. The design parameter n is adjusted accordingly and an optimal feedback gain k_1 is obtained. Considering that the addition of the second filter stage affects the position of the dynamically dominant poles of the first filter stage, as shown in **Fig. 6**, n and the PI controller gain must be slightly adjusted to fulfill the overshoot requirement. A feedback gain of $k_1 = 15$ V/A is obtained in the case at hand after this procedure.

The use of a feedback loop for the current of the second capacitor i_{C2} is also evaluated. Here, the converter voltage u_{co} is calculated from the output of the voltage controller u and the capacitor currents i_{C1} and i_{C2} as:

$$u_{co} = u - k_1 i_{C1} - k_2 i_{C2}, \tag{7}$$

where k_1 and k_2 are the feedback gains.

The feedback gains can be used to move the filter poles and to adjust the damping of the filter resonances. The effect of the feedback gains k_1 and k_2 on the placement of the filter poles is shown in **Fig. 7**. Only the inner loop is considered for these results (no voltage control loop). It can be observed in **Fig. 7(a)** that increasing k_1 moves the filter poles to the left side of the complex plane, providing damping of the resonances of both filter stages. By increasing the feedback gain k_2 the poles of the first stage of the filter move to the left while the poles of the second stage move to the right, as shown in **Fig. 7(b)**.

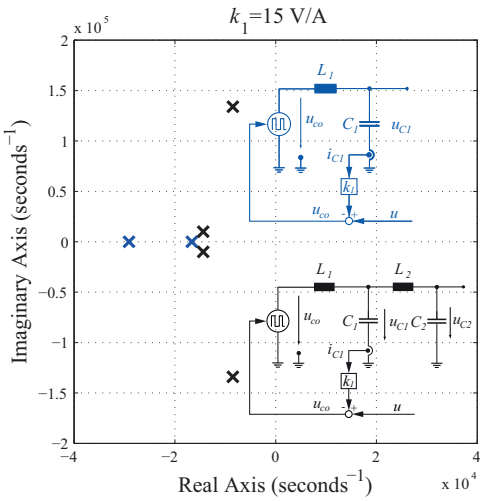
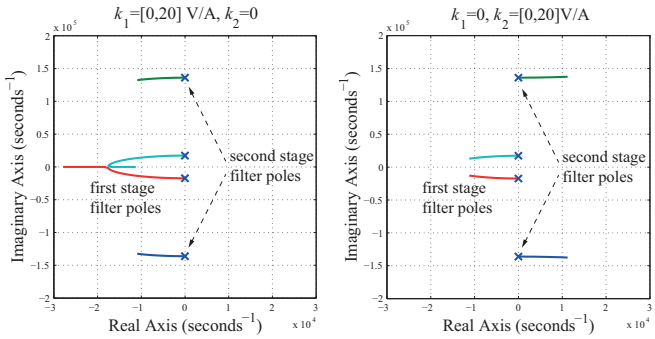


Fig. 6 Poles of the filter with feedback for a single-stage filter and a two-stage filter. Both systems using the capacitor current feedback with gain $k_1 = 15$ V/A and no load is connected at the output of the filter.



(a) Effect of k_1. (b) Effect of k_2.

Fig. 7 Effect of current feedback gains k_1 and k_2 on the poles of the system (the passive damping elements of the filter are not considered for these results). Output voltage is in open loop operation (no voltage controller). No load is connected to the filter.

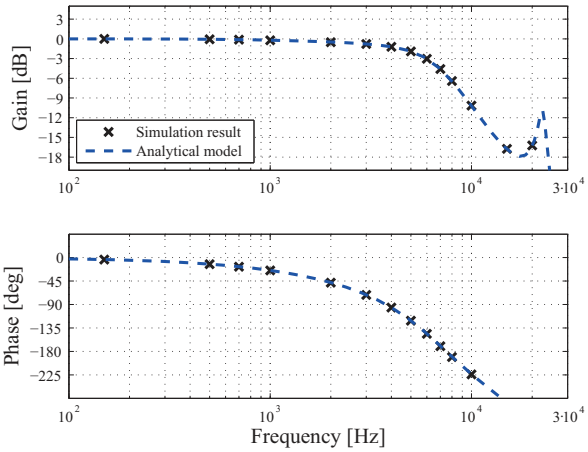


Fig. 8 Transfer functions from the reference to the output voltage for the PI(u_{C2})+FB(i_{C1}) scheme for a resistive load of 16 Ω (nominal load).

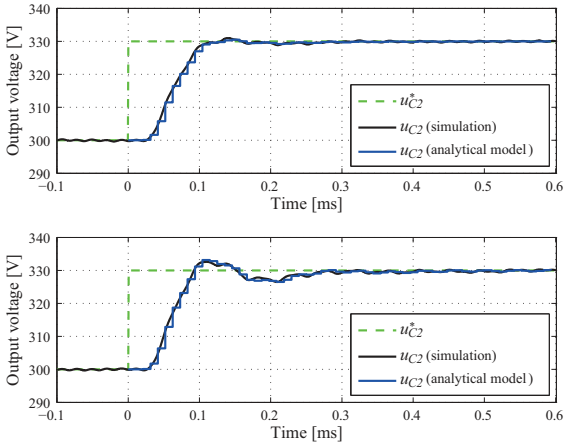


Fig. 9 Output voltage step responses for the PI(u_{C2})+FB(i_{C1}) scheme. Top: 16 Ω resistive load (nominal load), 1.7 % overshoot. Bottom: No load, 10.0 % overshoot.

Note that the poles of the second stage enter the right half plane, making the filter unstable. Considering these results, feedback of the capacitor current i_{C2} is not used in order to avoid instabilities.

The controller design is verified using a detailed analytical model of the AC source, considering the discrete-time implementation of the controller. A control bandwidth (-3 dB) for the output voltage of 5.9 kHz is achieved, as it can be observed from **Fig. 8**. This transfer function has been calculated analytically using Matlab and then verified with simulations of the controlled power source using GeckoCIRCUITS. The step responses with and without load are shown in **Fig. 9** for simulations and theoretical results from the analytical model. It can be observed that the highest overshoot is present during operation without load, for missing damping by a load resistance.

B. PI voltage control and PI current control [PI(u_{C2})+PI(i_{L1})]

A cascaded control scheme consisting of an inner current control loop and an outer voltage control loop is considered as the common structure for the control of high-bandwidth AC power sources [6], [7].

The use of the inner loop for controlling the inverter output current i_{L1} gives the opportunity of current limitation and therefore to protect the inverter against overcurrents. The dynamic response and compensation of load current harmonics can be improved by the inclusion of a feedforward of the reference voltage u^*_{C2} and of the load current i_{out}. The control scheme shown in **Fig. 3(b)** illustrates the implementation of these ideas. In this scheme a PI controller is used for the output voltage control loop and a second PI controller is used for the inner current control loop. The controllers can be designed

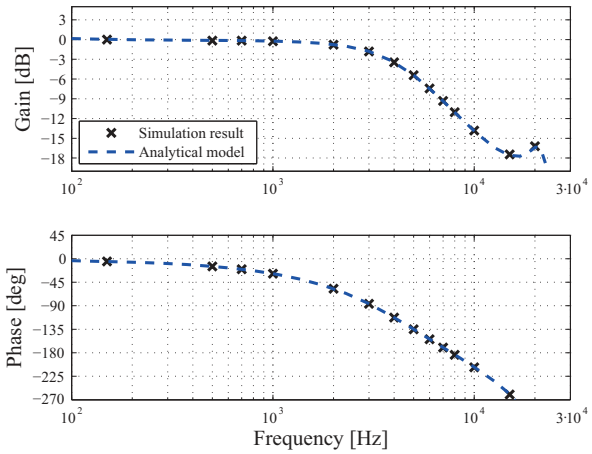


Fig. 10 Transfer functions from the reference to the output voltage for the PI(u_{C2})+PI(i_{L1}) scheme for a resistive load of 16 Ω (nominal load).

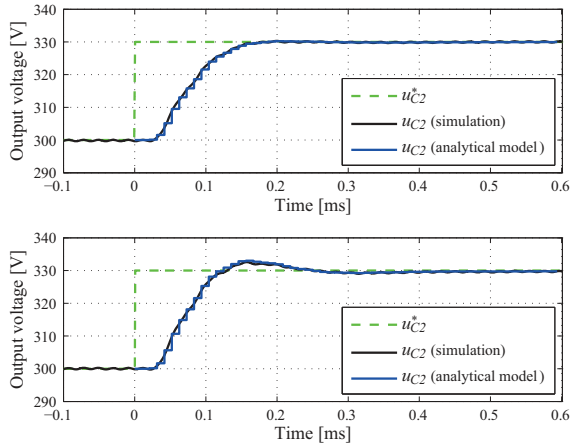


Fig. 11 Output voltage step responses for the PI(u_{C2})+PI(i_{L1}) scheme. Top: 16 Ω resistive load (nominal load), 0.8 % overshoot. Bottom: No load, 10 % overshoot.

independently if the inner control loop is much faster than the outer loop.

The inner control loop has been adjusted using a simple model of the inductor of the first stage of the filter as the controlled system. Then, a detailed model, including the inner loop and feedforward loops, is used for the adjustment of the voltage controller. The analytical and simulated results of the transfer function show that a small-signal control bandwidth (-3 dB) of 3.7 kHz is achieved (cf. **Fig. 10**). The step responses are shown in **Fig. 11**, where it can be observed that a very low overshoot occurs with nominal load, but a rather high overshoot appears when no load is connected to the output of the filter.

C. PI voltage control and P current control [PI(u_{C2})+P(i_{L1})]

In order to achieve the fastest possible response of the inner control loop, the previous control scheme can be slightly modified for using the deadbeat control concept for the inner loop. This concept has been proposed in [13] and [14] for uninterruptible power supplies with a single-stage LC filter, where deadbeat control is used of the inner and outer loops. In this paper, a PI controller is preferred for the outer loop in order to ensure a very low steady-state error for the output voltage (zero error for DC references).

Deadbeat control uses the system model to calculate the required converter voltage that makes the current error equal to zero in one single sampling interval. The equation that describes the dynamic behavior of the inverter output current i_{L1} is, based on the circuit diagram of **Fig. 1**:

$$L_1 \frac{di_{L1}}{dt} = u_{co} - u_{C1}. \tag{8}$$

By approximating the time derivative and assuming that the desired behavior of the system is to reach a current error of zero after one sampling interval, i.e. $i_{L1}(k+1) = i^*_{L1}(k)$, the required converter voltage for the deadbeat current controller is expressed as

$$u_{co}(k) = u_{C1}(k) + L_1 \frac{i^*_{L1}(k) - i_{L1}(k)}{T_s}. \tag{9}$$

Considering that the capacitor voltage u_{C1} is not measured, and that the dynamics of the outer control loop are much slower, it can be assumed that $u_{C1} \approx u^*_{C2}$ and the resulting current controller is equivalent to a proportional controller with voltage feedforward:

$$u_{co}(k) = u^*_{C2}(k) + L_1 \frac{i^*_{L1}(k) - i_{L1}(k)}{T_s}. \tag{10}$$

The block diagram for this control scheme is shown in **Fig. 3(c)**. By using a much faster inner control loop the outer control loop bandwidth can be increased, improving the overall performance of the power source.

The analytical and simulated results for the transfer function show that a rather high control bandwidth (-3 dB) of 9 kHz is achieved (cf. **Fig. 12**). However, it can be observed that a difference between the simulated and analytical results appears for frequencies higher than 10 kHz due to the voltage limitation of the inverter, which is not considered in the analytical model. The step responses are shown in **Fig. 13**, where it can be observed that a very fast response is achieved with this scheme. The highest overshoot is observed at no load operation.

D. Three-Loop Control [I(u_{C2})+FB(u_{C1}, i_{L1})]

A three-loop control scheme has been proposed in [15] to improve the dynamic performance of the output voltage u_{C2} of the power source, compared to a two-loop control (without feedforward loops), like the one presented in [7]. In addition to the bridge-leg current i_{L1} and output voltage feedback loops, a feedback loop for the capacitor voltage u_{C1} is included, as depicted in **Fig. 3(d)**.

According to the guidelines provided in [15], an integrator

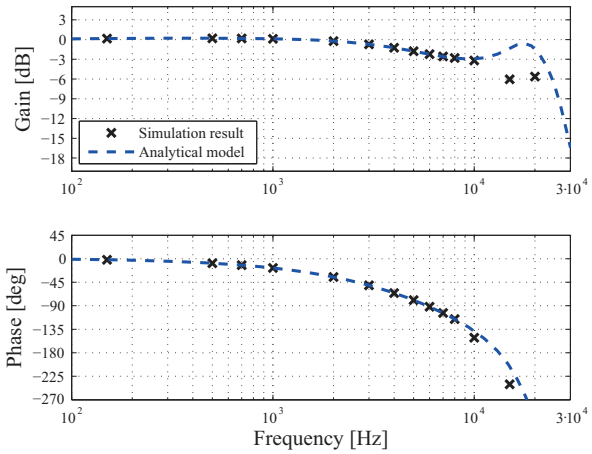


Fig. 12 Transfer functions from the reference to the output voltage for the PI(u_{C2})+P(i_{L1}) scheme (deadbeat control of i_{L1}) for a resistive load of 16 Ω (nominal load). Saturation of the controller for frequencies over 10 kHz is observed for the simulation results.

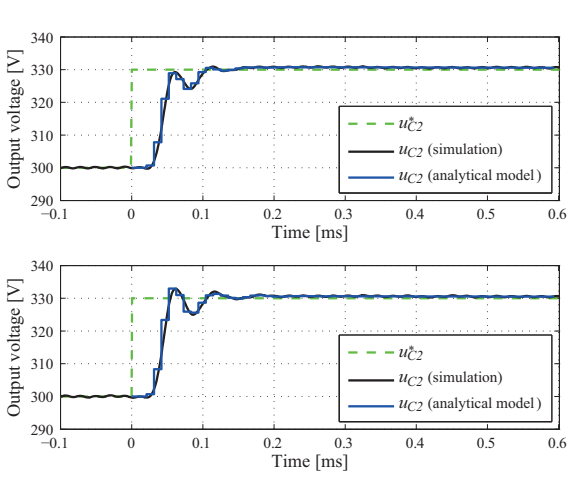


Fig. 13 Output voltage step responses for the PI(u_{C2})+P(i_{L1}) scheme (deadbeat control of i_{L1}). Top: 16 Ω resistive load (nominal load), 2 % overshoot. Bottom: No load, 10 % overshoot.

is used for the output voltage feedback loop:

$$G_{C2} = \frac{K_R}{s}, \tag{11}$$

where the integrator gain K_R determines the attenuation of the closed-loop transfer functions in the low-frequency range.

The capacitor voltage feedback loop considers a low-pass filter

$$G_{C1} = \frac{K_{C1}}{1 + sT_{C1}}, \tag{12}$$

where the filter pole is placed slightly beyond the resonance of L_2 and C_1, i.e. at $T_{C1} = \sqrt{L_2 C_1}/1.2$.

For the inductor current feedback, the gain K_L is set as high as possible without causing instability.

A control bandwidth (-3 dB) of 4.6 kHz is achieved with this control scheme, as observed from the transfer functions

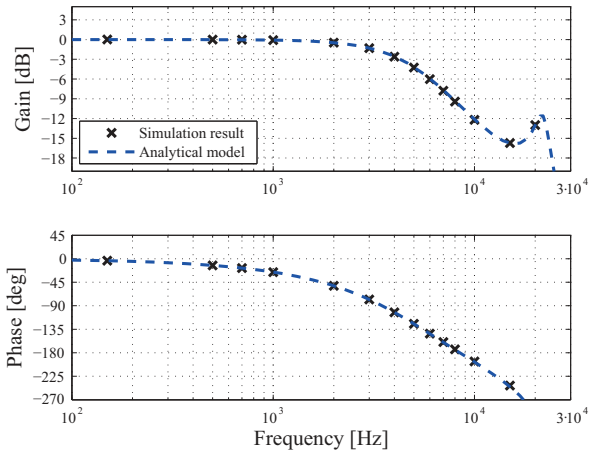


Fig. 14 Transfer functions from the reference to the output voltage for the I(u_{C2})+FB(u_{C1}, i_{L1}) scheme for a resistive load of 16 Ω (nominal load).

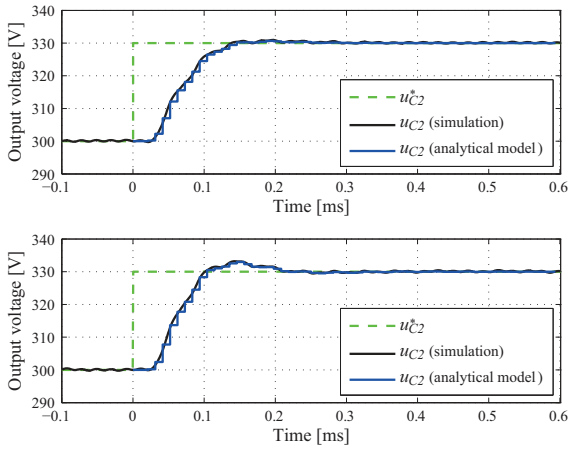


Fig. 15 Output voltage step responses for the I(u_{C2})+FB(u_{C1}, i_{L1}) scheme. Top: 16 Ω resistive load (nominal load), 2.1 % overshoot. Bottom: No load, 10 % overshoot.

of **Fig. 14**. The corresponding step responses are shown in **Fig. 15**. The highest overshoot appears when no load is connected to the output filter.

IV. Comparison of Results

Simulations of the power source circuit shown in **Fig. 1** are setup in GeckoCIRCUITS [16] where the different control schemes have been implemented digitally. One sampling time delay has been included in the control in order to emulate the delay introduced by the analog to digital conversion and calculation time of the control algorithms in the digital signal processor. As it is usual in a practical implementation, a delay compensation technique as the one presented in [17] and [18] is included in all the controllers.

The carrier frequency for the pulse-width modulation is 48 kHz and the sampling frequency for the control is 96 kHz

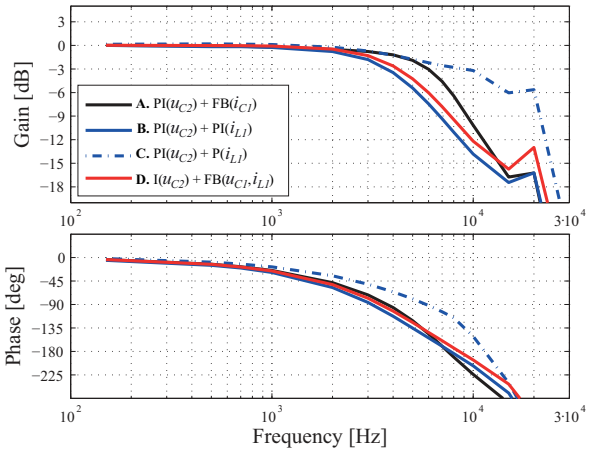


Fig. 16 Transfer functions from the reference to the output voltage obtained by simulation for a resistive load of 16 Ω (nominal load).

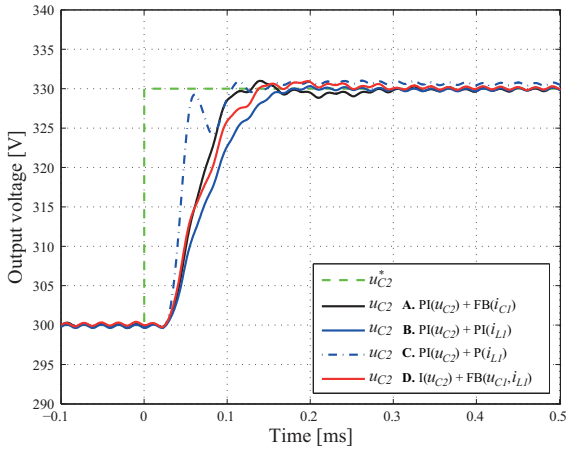


Fig. 17 Simulation results for a step change in the reference voltage for a resistive load of 16 Ω (nominal load).

(double-update mode). The filter parameters used in the simulations are listed in **Table I**.

The transfer function from the reference to the output voltage is calculated from simulation results by using a reference voltage composed of a DC value plus a 10 % AC component, i.e. $u^*_{C2} = U_0 + 0.1U_0 \sin(\omega t)$. Simulation results for the different control schemes are shown in **Fig. 16** for a DC voltage value $U_0 = 300$ V. It can be observed that the highest bandwidth is obtained with the PI(u_{C2})+P(i_{L1}) scheme, followed by the PI(u_{C2})+FB(i_{C1}) scheme. For frequencies higher than 10 kHz the voltage limitation of the inverter is observed. The step responses for a nominal resistive load of 16 Ω shown in **Fig. 17** illustrate the reference tracking capabilities of the different control schemes. It is observed that all control schemes present a low overshoot (below 2.1 %) for this loading. The fastest responses are achieved by the PI(u_{C2})+P(i_{L1}) and PI(u_{C2})+FB(i_{C1}) schemes, in concordance with the respective control bandwidths. The highest overshoot in the output voltage is observed under no load operation and has been fixed by design to 10 % for all control schemes. Simulation results for a step change in the reference voltage for no load operation are shown in **Fig. 18**.

In addition to the reference tracking, another important measure of the quality of a power source is the rejection of disturbances coming from the load current, which is equivalent

TABLE I Two-stage LC output filter values (cf. **Fig. 1**) used for the simulations.

Component	*Value*
L_1	328 µH
L_2	23 µH
C_1	6.3 µF
C_2	3.8 µF
L_D	11.5 µH
R_D	2.2 Ω

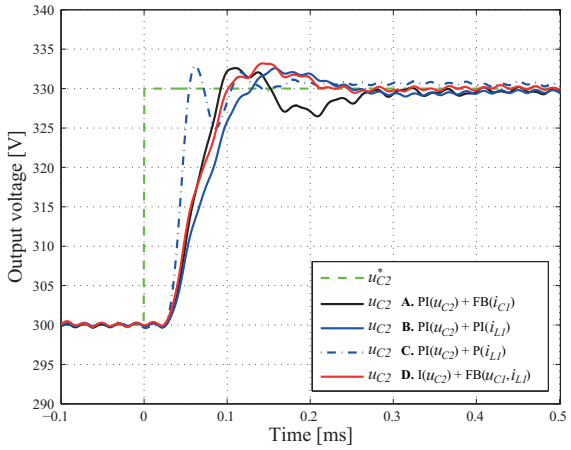


Fig. 18 Simulation results for a step change in the reference voltage under no load operation.

to a low output impedance. The output impedance of the power supply has been computed by simulations using a controlled current source as a load. For a constant voltage reference a load current composed of a DC component and an AC sinusoidal component $\tilde{i}_{f,i}$ of variable frequency f_i is injected. Then, the AC component in the output voltage $\tilde{u}_{f,i}$ is measured at the corresponding frequency and the output impedance is calculated as

$$|z_{out,i}| = \frac{|\tilde{u}_{f,i}|}{|\tilde{i}_{f,i}|}. \tag{13}$$

The results obtained in this way are shown in **Fig. 19**. The lowest output impedance is obtained with the PI(u_{C2})+P(i_{L1}) and the PI(u_{C2})+FB(i_{C1}) scheme, with an output impedance of 1.5 Ω and 3.7 Ω, respectively, measured at 3 kHz. The lowest peak value is obtained with the I(u_{C2})+FB(u_{C1}, i_{L1}) scheme, with 5 Ω at 5 kHz. For frequencies higher than 15 kHz the voltage limitation of the inverter is observed. The response to a step change in the load current from 13 A to 15 A

TABLE II Performance indexes for the different controller structures.

Performance index	PI(u_{C2})+FB(i_{C1})	PI(u_{C2})+PI(i_{L1})	PI(u_{C2})+P(i_{L1})	I(u_{C2})+FB(u_{C1}, i_{L1})
Control bandwidth (-3 dB)	5.9 kHz	3.7 kHz	9.0 kHz	4.6 kHz
Overshoot (16 Ω nominal load)	1.7 %	0.8 %	2.0 %	2.1 %
Overshoot (no load)	10.0 %	10.0 %	10.0 %	10.0 %
Output impedance at 3 kHz	3.7 Ω	4.9 Ω	1.5 Ω	3.9 Ω
Output impedance (max)	8.5 Ω	5.6 Ω	6.2 Ω	5.0 Ω

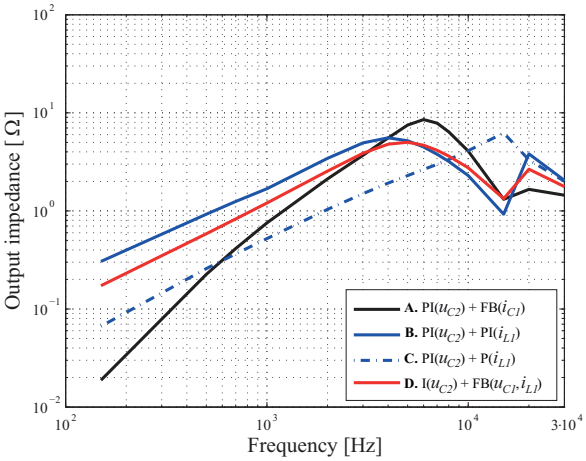


Fig. 19 Output impedances obtained from simulation results.

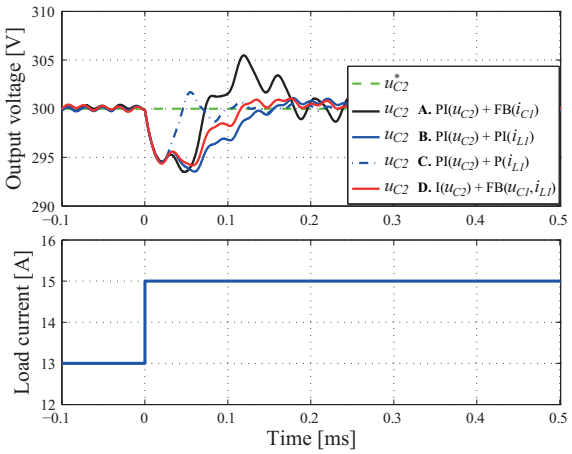


Fig. 20 Simulation results for a step change in the load current.

is shown in **Fig. 20**. A voltage drop of 5.5 V is observed for the PI(u_{C2})+P(i_{L1}) scheme. A similar voltage drop is observed for the I(u_{C2})+FB(u_{C1}, i_{L1}) scheme, but the disturbance is suppressed with slower dynamics, compared to the PI(u_{C2})+P(i_{L1}) scheme.

A summary of the comparative results is presented in **Table II**. From these results, it is clear that the highest bandwidth and lowest output impedance (at 3 kHz) is achieved by the PI(u_{C2})+P(i_{L1}) scheme. The second highest bandwidth is achieved by the PI(u_{C2})+FB(i_{C1}) scheme, which is also second in terms of output impedance. However, from the four control schemes, the PI(u_{C2})+FB(i_{C1}) presents the highest peak value of the output impedance. The I(u_{C2})+FB(u_{C1}, i_{L1}) scheme presents the lowest peak value of the output impedance and the third highest control bandwidth. The lowest bandwidth and the highest output impedance is achieved with the PI(u_{C2})+PI(i_{L1}) scheme. However, this scheme presents the lowest overshoot under nominal load.

V. Conclusions

Four multi-loop control schemes for a high-bandwidth power source with a two-stage LC output filter are evaluated in this paper. All these schemes have an output voltage controller in the outer loop, and for the inner control loop the following options are evaluated: capacitor current feedbacks, proportional-integral current control, proportional (deadbeat) current control, and capacitor voltage and inverter output current feedbacks. The comparative evaluation considers the small-signal control bandwidth, overshoot in the output voltage for step in the reference and load changes and output impedance as performance indexes.

According to the obtained results, the best dynamic performance, with respect to the defined indexes, is obtained using a cascaded structure with a PI controller for the voltage control and a proportional controller for the inner current control loop (PI(u_{C2})+P(i_{L1}) scheme). Another advantage of this scheme is the simplicity in the adjustment of the current controller, compared to the other three schemes. The sensitivity of this control scheme to errors in the applied voltage (e.g. caused by semiconductor on-state voltage drops or PWM errors) and filter parameters needs to be verified.

A different concept that also presents good performance indexes is the PI(u_{C2})+FB(i_{C1}) scheme. This scheme allows a more intuitive approach by using an active damping of the resonance of the first stage of the filter.

In the course of future research, the optimal selection of the feedback gains will be considered.

Furthermore, experimental verification of the theoretical results will be performed for a 10 kW laboratory prototype.

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