Comparative Evaluation of Voltage Source Converters with Silicon Carbide Semiconductor Devices for High-Voltage Direct Current Transmission

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***Abstract*—Recent advancements in silicon carbide (SiC) power semiconductor technology enable developments in the high-power sector, e.g., high-voltage direct current (HVdc) converters for transmission, where today silicon (Si) devices are state-of-the-art. New submodule (SM) topologies for modular multilevel converters (MMCs) offer benefits in combination with these new SiC semiconductors. This paper reviews developments in both fields, SiC power semiconductor devices and SM topologies, and evaluates their combined performance in relation to core requirements for HVdc converters: grid code compliance, reliability, and cost.**

A detailed comparison of SM topologies regarding their structural properties, design and control complexity, voltage capability, losses, and fault handling is given. Alternatives to state-of-the-art SMs with Si insulated-gate bipolar transistors (IGBTs) are proposed, and several promising design approaches are discussed. Most advantages can be gained from three technology features. Firstly, SM bipolar capability enables dc fault handling and reduced energy storage requirements. Secondly, SM topologies with parallel conduction paths in combination with SiC metal-oxide-semiconductor field effect transistors (MOSFETs) offer reduced losses. Thirdly, a higher SM voltage enabled by higher blocking voltage of SiC devices results in reduced converter complexity. For the latter, ultra-high-voltage (UHV) bipolar devices, such as SiC IGBTs and SiC gate turn-off thyristors (GTOs), are envisioned.

***Index Terms*—HVdc transmission, modular multilevel converter, power semiconductor devices, silicon carbide, submodules.**

I. Introduction

HVDC transmission technology requires integration into the existing alternating current (ac) grid. The conversion is performed via high-power converters. The modular multilevel converter (MMC) is a versatile and flexible topology with several options for optimization. MMCs have been intensively investigated since the early 2000's. It was identified, that modularity, scalability, built-in redundancy, and harmonic performance are advantageous for meeting widely varying requirements in grid applications. Compared to previous voltage source converters (VSC), the need for bulky harmonic filters is reduced or eliminated entirely. MMCs can be designed for low semiconductor losses around the 0.5 % mark, and active and reactive power can be adjusted independently during operation. With the named features the MMC is a promising option for high-voltage direct current (HVdc) transmission systems, flexible ac transmission systems (FACTS), and dc grids. The MMC consists of converter arms between ac and dc terminals. Each arms consist of a series connection of submodules (SMs) which operates as a variable voltage source, and an arm inductor. Other multilevel converter topologies [1], [2], and hybrid converter topologies, mixing VSC and current source converter (CSC), have also been proposed [3]–[5].

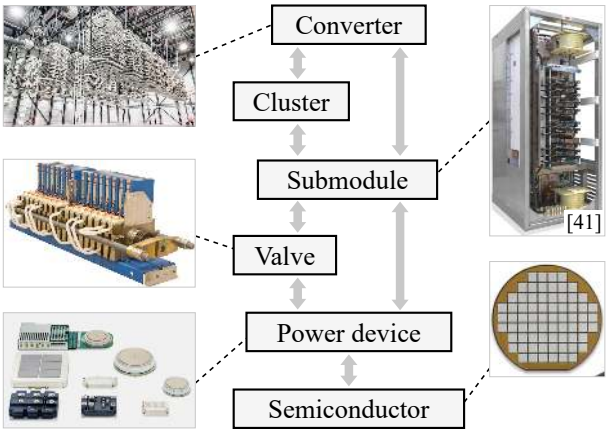

Fig. 1: Structural hierarchy of high-power electronic components in HVdc VSCs (photographs courtesy of Hitachi ABB Power Grids).

Several converter requirements for HVdc transmission systems are summarised and described in Table I. Grid code compliance, high reliability, and low cost are of paramount importance and, thus, considered as core requirements. Reliability of VSC systems has been analyzed in [6], and an example cost breakdown is given in [7]. Since the listed requirements ℛ1–10 are to some extent mutually dependent, it is necessary to find an optimum trade-off between them depending on the specific application, however, the core requirements should have the highest priority. Cost and performance of converters have to be judged from a system level [8].

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TABLE I: HVdc converter technical requirements $\mathcal{R}1$–10 addressing the core requirements (CRs): grid code compliance, high reliability, and low cost.

#	Requirement	CRs	Description
$\mathcal{R}1$	Sufficient harmonic performance		Harmonic distortion caused by the discrete arm voltage levels should not exceed limits defined by the grid operator (IEEE Std 519-1992 recommends THD $= 1.5 - 2\,\%$).
$\mathcal{R}2$	Dc-side fault handling		Faults occurring externally on the dc-side need to be handled in order to ensure the stability of the grid and avoid damage to the converter.
$\mathcal{R}3$	Robustness		Components need to survive events of stress beyond rated operation, such as surge currents during dc-faults or short-circuit.
$\mathcal{R}4$	Internal fault handling		In case of component failure in the SM, a reliable and uninterrupted operation of the converter has to be ensured.
$\mathcal{R}5$	Low complexity		Fewer points of failure are desirable to increase reliability, reduce cost, and offer simple maintenance.
$\mathcal{R}6$	High efficiency		Lower power losses decrease operational cost and might also relax requirements for the cooling system.
$\mathcal{R}7$	Maintainability		Spare parts need to be available, ideally from several sources. System complexity should be kept as low a possible to keep maintenance periods short.
$\mathcal{R}8$	Low semiconductor expenditure		Semiconductor expenditure directly translates to investment costs.
$\mathcal{R}9$	Low energy storage		SM capacitors are expensive and bulky. Thus, energy storage requirements have a direct impact on investment cost and converter weight.
$\mathcal{R}10$	Small footprint		Some applications, such as city center infeed and offshore platforms, require lightweight and compact converters.

The hierarchy of hardware in an MMC is illustrated in Fig. 1: Converter, converter arm, cluster, submodule, valve, power semiconductor device, semiconductor, where clusters and valves are optional. Technical requirements $\mathcal{R}1$–10 can or have to be addressed on different levels of the hardware hierarchy. This article focuses on benefits gained from recent developments in silicon carbide (SiC) semiconductor devices, power semiconductor device packaging, and SM topologies.

The article features the following original research contributions:

- New SM topologies with functionalities that have not been reviewed are included
- A power semiconductor device perspective with particular focus on new SiC devices is given
- A fair semiconductor loss and expenditure comparison is made by taking into account arm voltage modulation ratio, differing voltage capability of SM topologies, semiconductor count, and semiconductor type (unipolar or bipolar).
- Separate semiconductor loss evaluation for conduction losses, switching losses, and switch utilization
- Discussion of promising combinations of SM topology and semiconductor device technology

In Section II, recent advancements for high-power semiconductor devices are reviewed and evaluated. Section III compares a variety of SM topologies and their functionality. Promising combinations of SM topology and power semiconductor device technology are highlighted. The converter performance regarding power loss and semiconductor expenditure is presented in two studies in Section IV. Finally, in Section V, several promising design approaches for future HVdc converters are discussed.

II. High-Power Semiconductor Devices

The following section gives an overview of recent advancements in power devices relevant for HVdc converters. SiC semiconductors with high-power ratings have become available recently, but silicon (Si) devices are still the most viable option, due to their maturity and lower cost. A combination of Si and SiC devices in one SM has been proposed in [9], [10]. Relevant advancements in packaging are also highlighted, since it has a major impact on the power device performance and functionality.

A. High-Power Si Devices

1) IGBT: Today, a commonly used semiconductor technology for VSC HVdc applications is the IGBT. The anti-parallel diode can be integrated into the IGBT structure, known as bi-mode insulated gate transistors (BIGT) [11], [12].

The most common package for IGBT dies is the wire bonded module (WBM), with current ratings up to 3.6 kA or voltage ratings up to 6.5 kV. Since these devices are low-cost, mature, and widespread they satisfy $\mathcal{R}7$ and $\mathcal{R}8$. Due to degradation or over currents, the bond wires (or alternative die interconnect) can lift off or melt down. Parasitic- and circuit inductance maintain the current flow, resulting in arcing, evaporation of the insulating gel, and explosion of the power device. Such fault represents a high risk for neighboring equipment, and more robust solutions are preferable, e.g. press-packs (PPs).

Circular multi-chip press-packs (CMC-PP) for die sized semiconductors, exist since the 90's [13], [14] with products available up to 6.5 kV and approximately 2 kA [15]. These do not have the weakness of bond wires, contributing to $\mathcal{R}2$–4. Unequal distribution of thermo-mechanical stress remained an

issue until today [16]–[18]. A SM implementation with such devices has been presented in [19].

A similar type of package is the the modular press-pack (M-PP) [20], [21]. Semiconductor dies are arranged on a base-plate, and the drain or collector side is connected by an aluminum contact, pressured by a spring-washer pack. Several of these modules can be paralleled in one package. They feature double-sided cooling with low thermal junction-to-case resistance [22]. M-PP BIGTs have high-power density, reduced thermo-mechanical stress, and balanced power loss heat. Such devices offer the highest power rating for voltage controlled power semiconductor devices, and are available up to 5.2 kV and 3 kA [23].

Both, CMC-PP and M-PP, are suitable for series connection of several of these devices, forming a valve [24]. They feature short-circuit failure mode (SCFM) [25], [26], which makes them a viable option for cascaded two-level converters [27], and enables to implement redundancy into the valve. M-PP BIGTs have the properties to meet $\mathcal{R}2$–4 and $\mathcal{R}10$.

2) Integrated Gate-Commutated Thyristor: Early HVdc converters were CSCs using mercury arc valves and later thyristors [28], [29]. In VSCs, thyristors are still used in bypass equipment for SMs, meeting $\mathcal{R}4$, as shown in Fig. 5. There are SM implementations that propose thyristors as main power switches, because of their robustness, overcurrent capability and low conduction losses [30]. Also, it is possible to bypass groups of SMs with a stack of thyristors for reduced losses $\mathcal{R}6$ and increased dc fault tolerance $\mathcal{R}2$ [31], [32].

Another power device for SMs is the integrated gate-commutated thyristor (IGCT) [33], [34], a thyristor-based device with turn-off capability and superior conduction capability, resulting in low conduction losses $\mathcal{R}6$ [35]. The anti-parallel diode can be employed separately, on the same wafer [36], or integrated into the structure [37]. IGCTs are press-pack devices enclosed in a circular ceramic housing. The package features double-sided cooling and SCFM [38], which makes them suitable for series connection to form a valve [24]. Current filamentation within the wafer needs to be addressed by slowing down the turn-on process of the device. This is commonly done by limiting di/dt with an additional reactor $L_{\mathrm{di/dt}}$, as shown in Fig. 2(a). The reactor also limits current surges during SM internal faults $\mathcal{R}4$ [39], [40]. An RCD clamped snubber is necessary to avoid over-voltages during turn-off and to discharge the reactor, which adds to complexity and losses.

Robust SM implementations $\mathcal{R}3$ with IGCTs have been presented in [41], [42]. The auxiliary resonant commutated pole (ARCP) circuit can be used to soft-switch IGCT and reduce the need for $L_{\mathrm{di/dt}}$ [43], as shown in Fig. 2(b).

B. High-Power SiC Devices

With the recent success of the SiC MOSFET and advancements in bipolar SiC technology, new benefits for HVdc converters are within reach. Since available high-power Si devices are mature and cost-efficient, the change from Si to SiC technology needs to be motivated by significant improvements. In the following, recent progress for SiC device

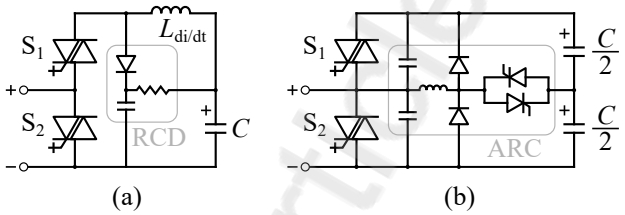


Fig. 2: (a) Half-bridge SM using IGCTs and auxiliary equipment, and (b) soft-switched ARCP version.

technology is reviewed and its potential impact on $\mathcal{R}1$–10 discussed. One difference between unipolar and bipolar SiC is their technology readiness level. Therefore, they are addressed separately in the following subsections.

1) Unipolar: SiC unipolar devices, such as the MOSFET, can provide high blocking voltage, low conduction loss, and superior switching speeds compared to same class Si IGBT modules [44]–[48]. The success of this type of semiconductor in the high-voltage segment in the last years requires a rethinking of converters and packaging to utilize their full potential. Challenges in packaging for SiC MOSFETs involve high-voltage insulation, high temperature operation, robustness, and low parasitics. WBM packaging for SiC MOSFETs has been reviewed in [49]–[52].

The resistive conduction characteristic of MOSFETs allows for significant reduction of on-state voltage by parallel connection, whereas a parallel connection of IGBTs is always limited to their built-in voltage. Apart from having a direct impact on efficiency $\mathcal{R}6$, this characteristic can also be used in order to obtain additional freedom for the cooling design. SiC can handle higher operation temperatures, which supports such a design approach and offers improvements regarding robustness $\mathcal{R}3$. However, available SiC power devices are WBMs and the power rating of most of them is not sufficient for HVdc transmission, as presented in Fig. 3. WBM layouts facilitating parallel connection on power device level are only available for Si IGBTs. The LinPak is reported as SiC ready [53], [54]. The PrimePack™ [55], [56] is currently only available with Si IGBTs. A packaging standard for high power SiC modules does not exist yet. The benefits of SiC MOSFETs regarding power losses in HVdc systems have already been demonstrated in [57], where 3.3 kV SiC MOSFETs achieved a loss reduction of 50 %.

Another interesting characteristic of SiC MOSFETs is the high blocking voltage enabling high SM voltage without series connection of devices, reducing converter complexity $\mathcal{R}5$ and size $\mathcal{R}10$. An implementation with 10 kV SiC MOSFETs and high switching frequency has been presented in [58]. A significant difference between Si IGBTs and SiC MOSFETs is the extremely fast switching speed. To support switching performance, reduced parasitic inductance in the range of 2 nH has been demonstrated with novel die interconnects and three-dimensional packaging concepts [59]–[65]. Note that although beneficial for switching losses, high-speed switching is not vital for MMCs.

External dc faults may result in surge currents which flow

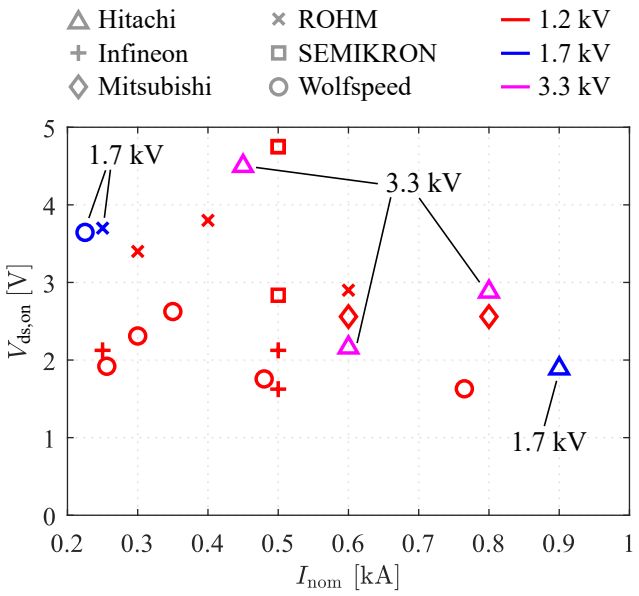


Fig. 3: Forward voltage drop of available SiC MOSFET modules of different current ratings ($T_j = 150\,°C$).

in reverse direction through the power semiconductor devices. For SiC MOSFETs the current would flow through the body diode. The surge current capability $\mathcal{R}2$ of SiC MOSFET modules and TO-247 at 10 times rated current has been tested in [66] and compared to Si PiN diodes in [67]. [68] has reported no degradation of on-state resistance for 1000 repetitive 10 µs surges at 10 times rated current for different manufacturers. Repetitive surges of 10 ms over a certain current level lead to degradation of the device in terms of threshold voltage, leakage current, and reverse voltage drop [69]. This shows that the SiC MOSFET is a promising candidate for fulfilling $\mathcal{R}2$ and $\mathcal{R}3$, however, further maturity of this technology is necessary.

SM-internal faults $\mathcal{R}4$ require power semiconductor devices to feature short-circuit capability. Current passes through the MOSFET channel and a hotspot is generated just a few µm below the gate oxide. A failure of the device is caused by either thermal runaway [70], or degradation (threshold voltage and leakage current) and damage to the gate oxide [70]–[74]. [75] has found the short-circuit capability of SiC MOSFETs to be much lower than for comparable Si IGBTs. While reported short circuit times range from 5 to 21 µs, the recommended value is in the range of a few micro-seconds for 1.2 kV devices [76]. Driver functionality for clearing short circuits has been presented for single-chip devices in [77] (within 420 ns), and for high-power modules in [78] (within 1.15 µs).

The mentioned currents above rating can also be damaging for the die interconnect of WBMs, hence, developments in packaging are needed to enable SiC MOSFETs for high-power applications, such as HVdc transmission. A novel PP concept with pressure applied in two directions, the power stage and the heatsink, is presented in [79], [80]. Recent investigations have shown that also SCFM can be achieved for PP SiC MOSFETs [81], [82]. SiC MOSFET PP devices have been presented in [82]–[84], enabling improvements regarding $\mathcal{R}2$–4.

It can be concluded that SiC MOSFET power devices can be suitable for MMCs. They are competitive with Si IGBTs in terms of conduction performance, and superior in terms of switching speed and blocking voltage. Basic surge and short-circuit capability has already been demonstrated, but robustness and reliability of SiC MOSFETs has yet to mature in order to achieve similar performance compared to Si IGBTs. This goes hand in hand with the development of highly reliable packaging solutions. Furthermore, developments in SiC MOSFET technology have been motivated by higher target operation frequencies required for passive component minimization. Conduction-optimized devices have been less of a focus, but are required for HVDC applications.

2) Bipolar: For bipolar charge carrier semiconductor devices (e.g. PiN diode, IGBT and GTO thyristor) the blocking voltage V_b can be designed significantly higher than for unipolar charge carrier devices (e.g. SBD and MOSFET). This is due to a low resistance of the relatively thick drift region, enabled by conductivity modulation. Unipolar devices with a drift layer thickness of 12–30 µm result in $V_b = 1.2{-}3.3$ kV, while for bipolar devices a drift layer thickness of 160–230 µm results in $V_b = 20{-}27$ kV [85]–[88]. The optimal transition point between unipolar and bipolar devices depends on the application, but is predicted at around 10 kV [89].

Simulation studies indicate that these UHV devices may offer a significant reduction of conduction losses $\mathcal{R}6$, system complexity $\mathcal{R}5$, control hardware, cables, and fibers (due to a lower amount of SMs per arm) [90]–[92], contributing to a smaller footprint $\mathcal{R}10$ and cost-reduction €. However, there are no bipolar SiC transistors on the commercial high-power market today and research is required in various fields, e.g., p-type substrate quality, epitaxial growth with low defect densities and high charge carrier lifetime, and low resistive contacts, to solve and/or circumvent known issues before high-voltage devices become available [93], [94].

State-of-the-art research level devices show promising results in terms of forward voltage drop which is less sensitive to temperature increase as compared to unipolar devices. The forward voltage characteristics of selected high-voltage devices [86]–[88], [95], [96] are shown in Fig. 4. As seen in the figure, the development of SiC IGBTs has evolved since 2014, indicated by improved conduction characteristic of the 26.8 kV SiC n-IGBT presented in [88], compared to the 27.5 kV SiC IGBT announced in [86]. Recent developments in increasing charge carrier lifetime have enabled a 15 kV SiC n-GTO which shows significantly better switching characteristics, i.e. 45 times shorter turn-off time, over a 15 kV SiC p-GTO [96]. High-voltage PiN diode structures demonstrate low conduction energy loss $\mathcal{R}6$, but may generate high reverse recovery currents [97]. Merged PiN-Schottky diodes show less reverse recovery, and may be a suitable alternative [98]. Short-circuit capability of 2 µs and clearing of the fault has been demonstrated for a 15 kV SiC IGBT module, however issues with gate-voltage overshoot remain [99].

In the future, it is predicted that devices up to 50 kV may be suitable in HVdc converter applications where a

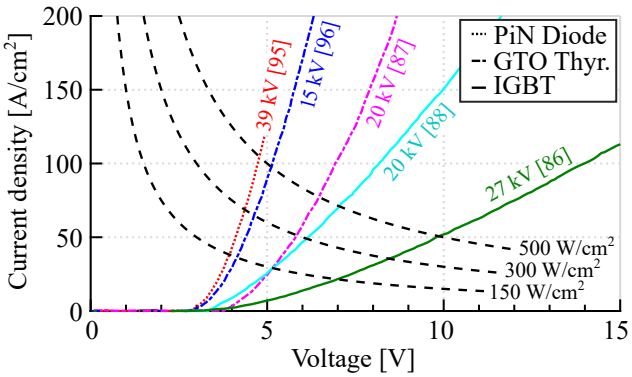


Fig. 4: Conduction characteristics of research level SiC bipolar devices ([86]–[88], [95], [96]).

low switching frequency is used [92], [93], [100]. Since the junction termination extension (JTE) determines the active area/chip area ratio, it is closely related to semiconductor chip cost and manufacturing yield. The state of art JTE designs range from 1.05-1.50 mm for 27 kV devices [86], [95], leading to an active area ratio of 35 % [86]. The majority of the high-voltage prototype devices is packaged in custom made high-voltage enclosures/modules [101]–[103] or immersed in dielectric fluid [96], [104]–[106]. Novel packaging solutions for high voltages and low thermal resistance have been demonstrated in [105], [106], where a stack of high-voltage diodes was immersed in dielectric fluid reaching breakdown voltages above 30 kV and with a large heat flux rate (i.e. 500 W/cm^2).

With the current state of development, it is difficult to evaluate robustness, reliability, and cost effectiveness of such bipolar SiC devices for HVdc application. Their conduction characteristic and high blocking voltage might offer significant benefits regarding complexity $\mathcal{R}5$ and efficiency $\mathcal{R}6$. However, further developments in die size, yield, and packaging are needed before high-power devices become available. Since MMCs can be scaled independently of power semiconductor device blocking voltage, it is questionable whether UHV bipolar SiC devices will be cost competitive $\mathcal{R}8$ with lower voltage SiC MOSFETs, whose commercial success is driven by a much larger market.

III. Submodules

SMs are the fundamental building block of MMCs. All SM topologies have in common that they consist of one or several capacitors, and several power semiconductor switches and diodes. The switches direct the orientation of the capacitor terminals, such that the SM contributes to the total arm voltage with its own. This section first discusses design choices regarding SM rating and how internal faults are handled. Subsequently, SM topologies and their functionality are reviewed and compared, as summarized in Table II.

A. Voltage and Current Rating

The modular structure of the MMC allows to choose the voltage class of the power device independently of the converter voltage rating. In practice, however, a design with a high amount of low-voltage SMs might have the disadvantage of increased complexity of the mechanical construction, and more components for control hardware, communication fibers, auxiliary equipment, cooling conducts, etc. which opposes $\mathcal{R}5$. On the other hand, a design with a small amount of high-voltage SMs may require costly specialized semiconductor power devices $\mathcal{R}10$, such as future UHV bipolar SiC semiconductors (Section II-B2), or series connection of devices with additional auxiliaries for voltage balancing [24], [25], [107]. MMC arms with fewer SMs may also have reduced harmonic performance and increased redundancy requirements, opposing $\mathcal{R}1$ and $\mathcal{R}4$. Furthermore, internal short circuits will become more difficult to handle, due to increased SM voltage and energy. Some implications of such SMs for the converter design and control have been discussed in [91], [108].

Another option for increasing converter power capability is parallel connection of SMs. The main problem is an uneven current sharing, caused by differences in the parasitic components, bus bars, capacitors, and the power semiconductor devices. Furthermore, capacitors may be charged to different voltages, in which case parallel connection results in high surge currents between them. Hence, in contrast to converter voltage rating, the converter current rating is more closely tied to the limits of available power devices. In practice, the current rating of components is often determined by expected overcurrent during fault cases, e.g., free-wheeling diodes must withstand surge currents $\mathcal{R}2$.

B. Internal Fault Handling

Internal faults $\mathcal{R}4$ are addressed with the SM design. During a short circuit, caused by semiconductor failure for example, the SM capacitance may discharge very rapidly. The resulting short-circuit current i_{sc} is a damped oscillation, limited by the SM parasitic components: busbar resistance R_{b} and inductance L_{b}, equivalent series resistance of capacitor $\mathrm{ESR}_{\mathrm{C}}$, switch resistance R_{sw} and built-in potential V_{bi}, as shown in Fig. 5. Such an event has the potential to thermally and/or mechanically destroy the SM and neighboring equipment. Hence, the fault should either be avoided or contained. One method is to enclose the SM with explosion-proof housing and bypassing it externally [109]. This requires fast bypass equipment, e.g., thyristor T and mechanical switch $\mathrm{S}_{\mathrm{mech}}$, to provide a path for the arm current i_{arm}. A measure on topology level would be to always have two turned-off power devices between the capacitor terminals. Another option is to use additional redundant switches with SCFM in a valve. In case of semiconductor device failure, the blocking voltage distributes over the remaining devices. Also, fuses in series to the SM capacitor are an option, so that the internal fault is cleared after half the oscillation period. Assuming a loss-less loop, one can estimate the maximum current during a short circuit to $I_{\mathrm{sc,max}} = V_{\mathrm{c,t=0}}\sqrt{C/L_{\mathrm{tot}}}$, where $V_{\mathrm{c,t=0}}$ is the voltage of the capacitor before the fault, C is the SM capacitance, and L_{tot} is the total inductance in the short-circuit loop. SMs with dedicated di/dt reactors, as shown in Fig. 2(a) have reduced peak currents and longer oscillation period.

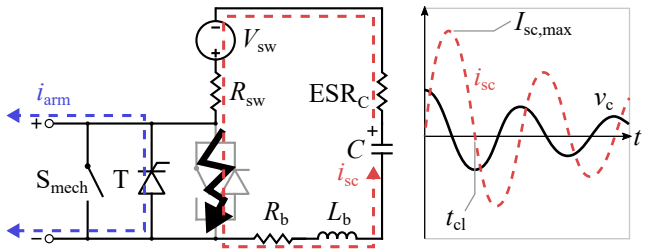


Fig. 5: Half-bridge SM during short circuit due to power semiconductor device failure.

C. Bipolar Capability

SMs with bipolar voltage capability enable negative arm voltage, which is relevant for dc-side fault handling $\mathcal{R}2$. During dc faults, the ability to support the ac grid (STATCOM operation), and dc current control are important. If a dc fault occurs, the voltage on the dc terminal drops. The missing voltage will then apply across the arm inductance of the converter, resulting in current surges. If a negative arm voltage can be inserted against the difference of alternating voltage and the dc terminal voltage, the voltage drop across the arm inductance can be controlled and surge currents can be reduced or prevented. SMs with fault controllability (bipolar four quadrant capable) can operate in STATCOM mode with full control over the direct current. Fault blocking SMs (bipolar three quadrant capable) may require additional dc-side switchgear, a circuit breaker or disconnector, to prevent the converter feeding the fault. For such converters, STATCOM capability may be interrupted temporarily [110]–[113]. Bipolar SMs also enable overmodulation capability, i.e. modulation index $M > 1$, leading to reduced rms arm current and lower power losses $\mathcal{R}6$. Additionally, energy storage requirements are reduced significantly $\mathcal{R}9$ [114]–[116], resulting in lower cost for SM capacitors and reduced converter weight.

In the following, the voltage modulation ratio, k, is introduced. It represents a design parameter defining the relation between the dc terminal voltage V_{dc} and the maximum ac terminal peak voltage $\hat{V}_{\mathrm{ac}}^{max}$ (1). M is an operation parameter defining the relation between V_{dc} and the actual ac terminal peak voltage $\hat{V}_{\mathrm{ac}}$ (2). The bipolar ratio r_{bip} defines how much negative voltage relative to the positive voltage can be provided in an arm, (3). For an arm consisting of only one SM topology, it equals to the amount of negative voltage levels $n_{\mathrm{Vc,neg}}$ in relation to the amount of positive voltage levels $n_{\mathrm{Vc,pos}}$.

$$\hat{V}_{\mathrm{ac}}^{max} = k\frac{V_{\mathrm{dc}}}{2}\begin{cases} k=1 & unipolar \\ k=\frac{1+r_{\mathrm{bip}}}{1-r_{\mathrm{bip}}} & bipolar \end{cases} \tag{1}$$

$$\hat{V}_{\mathrm{ac}} = M\frac{V_{\mathrm{dc}}}{2} \quad 0 \le M \le k \tag{2}$$

$$r_{\mathrm{bip}} = \frac{V_{\mathrm{arm,min}}}{V_{\mathrm{arm,max}}} = \frac{n_{\mathrm{Vc,neg}}}{n_{\mathrm{Vc,pos}}} \tag{3}$$

Bipolar capability comes at the cost of an increased semiconductor count, therefore opposes $\mathcal{R}8$. A way to reduce the semiconductor count is to either compose the arm of a mixture of SMs, known as hybrid MMC [117]–[121], or use asymmetrically bipolar SMs. The bipolar capability of the arm needs to satisfy requirements for dc-side fault handling $\mathcal{R}2$, and modulation index.

D. Topologies

Since the emergence of the MMC, a large variety of SM topologies have been proposed in order to improve the operation capabilities of the converter. Reviews have been provided in [2], [122]–[131]. A converter arm can consist of a single type of SM, or a mixture of several topologies, known as hybrid SM arm [117], [132]–[134]. This section offers additional contributions highlighting particularities and differences in the context of requirements for MMCs, and recent developments in SiC power semiconductor devices. The review is not exhaustive, but clearly highlights main benefits and mechanisms of each topology.

The reviewed SM topologies are depicted in Fig. 6 and Fig. 7. Higher voltage ratings are represented by a series connection of two devices. Evidently, also one device with twice the voltage rating can be used. The switching states presented for the different topologies do not represent all possible states, but the most common ones. All described states are valid for positive and negative arm current, i.e. unipolar topologies operate in two, and bipolar topologies in four quadrants.

1) Unipolar Voltage SMs: The well known half-bridge (HB) is the most basic SM topology. Multilevel topologies like the flying capacitor (FC), the neutral-point-clamped (NPC), and the T-connected neutral-point-clamped (TNPC), Fig. 6(a-c), have been proposed in the 90's [135]. Modulation and capacitor voltage balancing of the FC and the NPC topology as MMC SMs has been investigated in [136], and in more detail for the FC in [137], [138]. The NPC uses a switch arrangement, where the parallel connection of $[S_2 + S_5]$ and $[S_3 + S_6]$, may reduce conduction losses $\mathcal{R}6$ in one switching state. [139] proposes to rearrange the SM terminals, optimizing the NPC topologies in terms of semiconductor count and balancing. The parallel-connected-capacitor (PC) SM, Fig. 6(d), has been presented in [140]. The topology features parallel connection of switches and capacitors, reducing conduction losses $\mathcal{R}6$ and improving capacitor voltage balancing and harmonic performance $\mathcal{R}1$. In a similar way, the switched-capacitor (SC) SM presented in [141] and shown in Fig. 6(e), also features the parallel connection of capacitors and switches. The main benefit here is the reduced number of switches compared to PC, NPC and TNPC.

2) Symmetrically Bipolar Voltage SMs: The full-bridge (FB) SM, Fig. 6(f), features bipolar operation capability, at the cost of additional two switches, compared to the HB. There are two bypass states, giving the option of distributing power loss among the switches by alternating the switching states. The double-zero (DZ) SM, Fig. 6(h), has been proposed in [10], [142], [143]. Compared to the FB it employs an additional switch in series to the capacitor. For positive and negative SM

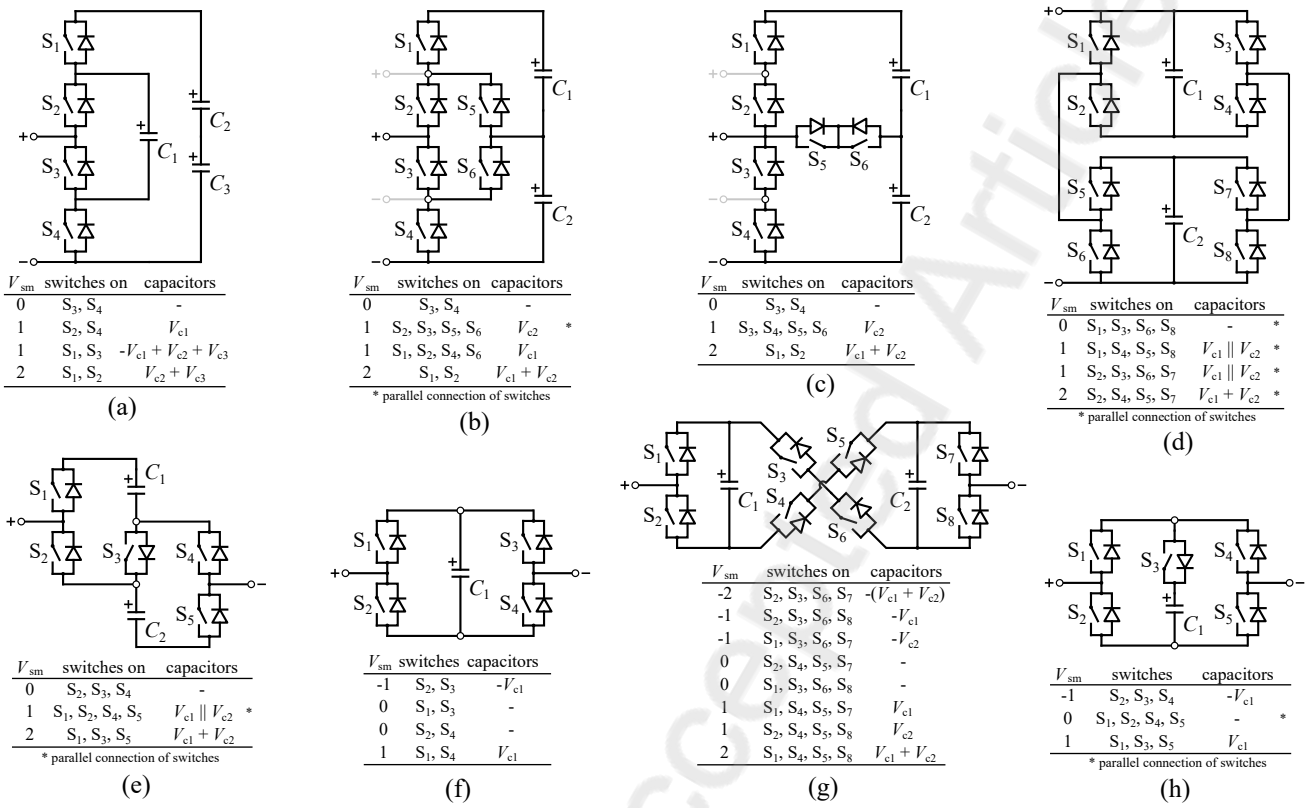
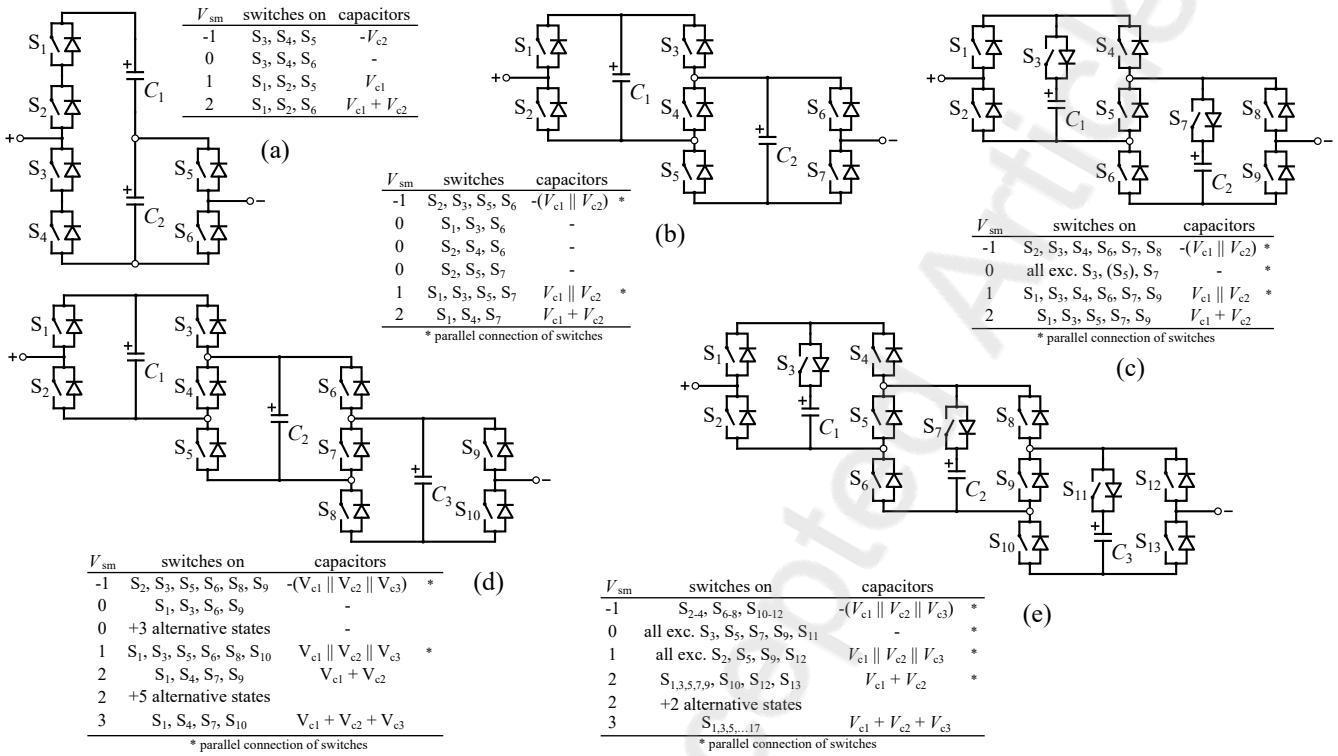


Fig. 6: SM topologies and their switching states, including SM voltage, V_{sm}, active switches, and active capacitors. Unipolar voltage topologies: (a) FC, (b) NPC, (c) TNPC, (d) PC, and (e) SC. Symmetrically bipolar voltage topologies: (f) FB, (g) CC5L, and (h) DZ.

voltage, this has the disadvantage of an additional switch in the path of the arm current. In bypass however, the current ideally splits equally, parallel connecting $[\mathrm{S}_1+\mathrm{S}_4]$ and $[\mathrm{S}_2+\mathrm{S}_5]$. This reduces conduction losses $\mathcal{R}6$ for two reasons: The arm current is highest when the arm voltage is low (i.e., most of the SMs are in bypass), and the parallel connection is a reduction of the semiconductor resistance by half. SiC MOSFETs are very suitable for such paralleling functionality due to their purely resistive characteristic. Furthermore, the extra switch between the capacitor terminals decreases the chance for internal short circuits $\mathcal{R}4$. The cross-connected 5-level (CC5L) SM [144], Fig. 6(g), can be derived from two cross connected FB and provides the same voltage capability as two series connected FB. The switch count is equal to two FB, with the difference of being able to replace $[\mathrm{S}_3+\mathrm{S}_6]$ and $[\mathrm{S}_4+\mathrm{S}_5]$ by single switches with twice the capacitor voltage rating, enabling a more compact structure $\mathcal{R}10$.

3) Asymmetrically Bipolar Voltage SMs: The required negative voltage capability of an MMC arm may just be a fraction of the positive arm voltage. Asymmetrically bipolar voltage topologies compromise on negative voltage capability for savings in semiconductor count $\mathcal{R}8$, or other benefits. The asymmetrical-commutation (AC) SM, Fig. 7(a), reduces switch count at the cost of one negative voltage level. Capacitor voltage balancing becomes more of an issue, because C_1 can only be inserted positively and therefore relies on negative arm current. The semi-full-bridge (SFB) SM, Fig. 7(b), is a topology with reduced semiconductor count, as S_4 is shared between the two double-connected FBs [145]. Internal current surges due to capacitor voltage imbalance have been investigated in [146], and have to be addressed similarly for all topologies featuring parallel connection of capacitors. The double connection of the DZ has been proposed in [10], [142] and yields the double-connected double-zero (DCDZ) SM, shown in Fig. 7(c). The DCDZ combines the advantages of the SFB and the DZ, such as low losses $\mathcal{R}6$, improved capacitor voltage balancing, and lower capacitor voltage ripple $\mathcal{R}9$ [143], [147]. The principle can be extended to more levels, for both the SFB and the DCDZ, resulting in the semi-full-bridge cluster (SFBC) and the cascaded double-zero cluster (CDZC), shown in Fig. 7(d-e). However, such a cascaded cluster will always be limited to $-1V_{\mathrm{c}}$. A HBFB hybrid arm can be tailored to achieve the same voltage functionality as these topologies by adjusting the proportion of HB and FB SMs, but capacitor voltage balancing is more complex and limited, since the HB requires negative arm current [142].

4) Fault Blocking Variants: For some topologies, switches can be replaced by diodes, reducing the switch count and associated auxiliaries $\mathcal{R}8$, but sacrificing the ability to operate in all four quadrants. These variants offer dc fault blocking capability $\mathcal{R}2$, meaning they provide negative SM voltage for negative SM current only. A short overview has been given in [129], [148]. The current path during fault blocking for the unipolar full-bridge (uFB) [149], [150], the clamped-double



V_{sm}	switches on	capacitors
-1	S_3, S_4, S_5	$-V_{c2}$
0	S_3, S_4, S_6	-
1	S_1, S_2, S_5	V_{c1}
2	S_1, S_2, S_6	$V_{c1} + V_{c2}$

V_{sm}	switches	capacitors	
-1	S_2, S_3, S_5, S_6	$-(V_{c1} \parallel V_{c2})$	*
0	S_1, S_3, S_6	-	
0	S_2, S_4, S_6	-	
0	S_2, S_5, S_7	-	
1	S_1, S_3, S_5, S_7	$V_{c1} \parallel V_{c2}$	*
2	S_1, S_4, S_7	$V_{c1} + V_{c2}$	

* parallel connection of switches

V_{sm}	switches on	capacitors	
-1	S_2, S_3, S_4, S_6, S_7, S_8	$-(V_{c1} \parallel V_{c2})$	*
0	all exc. S_3, (S_5), S_7	-	*
1	S_1, S_3, S_4, S_6, S_7, S_9	$V_{c1} \parallel V_{c2}$	*
2	S_1, S_3, S_5, S_7, S_9	$V_{c1} + V_{c2}$	

* parallel connection of switches

V_{sm}	switches on	capacitors	
-1	S_2, S_3, S_5, S_6, S_8, S_9	$-(V_{c1} \parallel V_{c2} \parallel V_{c3})$	*
0	S_1, S_3, S_6, S_9	-	
0	+3 alternative states	-	
1	S_1, S_3, S_5, S_6, S_8, S_{10}	$V_{c1} \parallel V_{c2} \parallel V_{c3}$	*
2	S_1, S_4, S_7, S_9	$V_{c1} + V_{c2}$	
2	+5 alternative states		
3	S_1, S_4, S_7, S_{10}	$V_{c1} + V_{c2} + V_{c3}$	

* parallel connection of switches

V_{sm}	switches on	capacitors	
-1	$S_{2\text{-}4}$, $S_{6\text{-}8}$, $S_{10\text{-}12}$	$-(V_{c1} \parallel V_{c2} \parallel V_{c3})$	*
0	all exc. S_3, S_5, S_7, S_9, S_{11}	-	*
1	all exc. S_2, S_5, S_9, S_{12}	$V_{c1} \parallel V_{c2} \parallel V_{c3}$	*
2	$S_{1,3,5,7,9}$, S_{10}, S_{12}, S_{13}	$V_{c1} + V_{c2}$	*
2	+2 alternative states		
3	$S_{1,3,5,\ldots17}$	$V_{c1} + V_{c2} + V_{c3}$	

* parallel connection of switches

Fig. 7: SM topologies and their switching states, including SM voltage, V_{sm}, active switches, and active capacitors. Asymmetrically bipolar voltage topologies: (a) AC, (b) SFB, (c) DCDZ, (d) SFBC3, and (e) CDZC3.

(CD) [151], [152], the half-voltage clamp (HVC) [153], [154], and the series-connected double (SCD) [155] SMs are shown in Fig. 8.

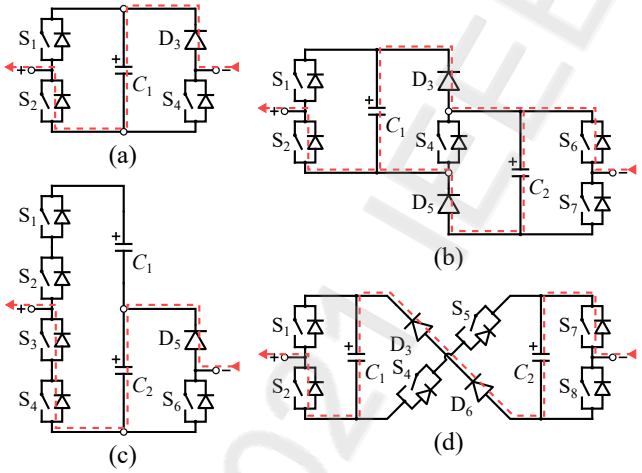


Fig. 8: SM variants featuring dc fault blocking capability instead of dc fault control capability: (a) uFB derived from FB by replacing S_3, (b) CD derived from SFB by replacing S_3 and S_5, (c) HVC derived from AC by replacing S_5, and (d) uCC derived from CC5L by replacing S_3 and S_6.

5) Comparison: A detailed comparison between the SM topologies is presented in Table II. The purpose of the table is to provide a summary of the attributes of the SM topologies mentioned in this paper. It allows to compare certain attributes directly, without analyzing the equivalent circuit diagrams, or consulting the given references. Furthermore, an evaluation of complexity and losses is given. The attributes of the topologies are grouped in four categories. ***"Structure"*** includes structural properties and the voltage ratings of switches and capacitors. It is also mentioned if the topology uses switches of different voltage rating, or double connection of SM segments. ***"Voltage"*** includes all properties related to voltage capability, and functions that benefit from it, such as the maximum k, and dc fault ride through $\mathcal{R}2$. Furthermore, it describes if there is a dc fault blocking version of the topology. In ***"Features"***, additional functionalities are listed. The amount of switches between the capacitor terminals indicates how robust the topology is against internal faults $\mathcal{R}4$. Switch parallel connection enables conduction loss reduction $\mathcal{R}4$. Capacitor parallel connection enables better capacitor voltage balancing $\mathcal{R}9$. Self-balancing is a feature, where the capacitors of an SM can be balanced easily for negative arm current. The switch that has to be turned OFF to activate self-balancing is indicated. ***"Evaluation"*** includes three attributes. Control complexity is an evaluation based on switch count, capacitor count, switch arrangement (simple HB pairs are easy to control), and modulation described in literature. Design complexity is an evaluation based on the structural properties, busbar connection points, nodes, and different switch- and capacitor ratings within the SM. Power loss is anticipating the results of the quantitative analysis provided in Section IV.

TABLE II: Comparison of SM topologies and their functionalities.
(Performance: – bad, ○ fair, + good, ++ very good)

		unipolar						symm. bipolar			asymm. bipolar				
	Topology	***HB***	***FC***	***NPC***	***TNPC***	***PC***	***SC***	***FB***	***CCSL***	***DZ***	***AC***	***SFB***	***DCDZ***	***SFBC3***	***CDZC3***
Structure	Basic building block					2FB			2FB		2HB	2FB	2DZ	3FB	3DZ
	# switches n_{sw} (normalized)	2	4	6	5	8	5	4	8	5	6	7	9	10	13
	# requ. switching signals	1	4	3-6	3	4	3	2	3	3	2	3	4-5	4	6-13
	Different switch voltage ratings				•				•		•				
	# capacitors n_{c} (normalized)	1	3	2	2	2	2	1	2	1	2	2	2	3	3
	Double connection					•	•		•			•	•	•	•
Voltage	# pos. voltage levels $n_{\mathrm{Vc,pos}}$	1	2	2	2	2	2	1	2	1	2	2	2	3	3
	# neg. voltage levels $n_{\mathrm{Vc,neg}}$							1	2	1	1	1	1	1	1
	Bipolar ratio r_{bip}							1	1	1	0.5	0.5	0.5	0.33	0.33
	Max. arm volt. modul. ratio k	1	1	1	1	1	1	∞	∞	∞	3	3	3	2	2
	dc fault-ride-through $\mathcal{R}2$							•	•	•	•	•	•		
	dc fault blocking version $\mathcal{R}2$							uFB	SCD	•[2]	uAC[1]	CD	•[2]		
Features	Add. switch at capacitor $\mathcal{R}4$						•			•			•		•
	Switch parallel connection $\mathcal{R}6$			•		•	•			•		•	•	•	•
	Cap. parallel connection $\mathcal{R}9$					•	•					•	•	•	•
	Self-balancing switch [146]					$S_{2,7}$	S_3					S_4	S_5	$S_{4,7}$	$S_{5,9}$
Eval.	Control complexity $\mathcal{R}5$	+	○	○	–	○	○	+	○	○	–	○	○	○	–
	Design complexity $\mathcal{R}5$	++	○	–	–	○	○	+	○	○	–	○	–	–	–
	Power loss $\mathcal{R}6$	++	++	+	+	++	+	–	–	–	○	○	○	+	+

[1] looses $-1V_{\mathrm{c}}$ state for positive arm current
[2] looses parallel path bypass capability

IV. Modular Multilevel Converter

This chapter combines the insights from the previous chapters and provides an evaluation with focus on the requirements $\mathcal{R}6$ and $\mathcal{R}8$. The converter- and arm design is based on the analytic approach described in the appendix.

A. Conduction Losses

Semiconductor conduction losses can be categorized as either resistive, caused by the resistivity of the semiconductor material (drift region, channel width, contact resistance of metal- semiconductor transition), or as constant, caused by the pn-junction within the device structure. The comparison of the two types of conduction losses is particularly interesting, since SiC MOSFETs are purely resistive, whereas future bipolar SiC devices possess a high built-in potential $v_{\mathrm{sw}} > 3\,\mathrm{V}$ and low resistance. Exemplarily comparing HB and FB, it is clear that the FB has always two switches conducting arm current, while the HB has only one. Hence, as a first approximation one could say that the FB has twice the conduction losses compared to the HB. However, comparing the topologies with equal semiconductor area, we achieve further conduction loss reduction in the HB due to an increased semiconductor rating. The difference between the two depends on the share of resistive and constant losses, determined by the power semiconductor device. A HB with purely resistive devices, e.g. SiC MOSFETs, has four times lower conduction losses as a FB. A HB using semiconductors with mostly constant losses, e.g. large area GTOs, would have a bit less than half the conduction losses of a FB. The ratio of built-in voltage drop V_{bi} to total voltage drop at nominal current $V_{\mathrm{tot,nom}}$ is defined as r_{v}, (4). As shown in Fig. 9, r_{v} has a typical value depending on the type of semiconductor. SiC MOSFETs have no built-in voltage, hence $r_{\mathrm{v}} = 0$. For commercially available Si IGBTs and the SiC IGBTs given in Fig. 4, r_{v} ranges from 0.4 to 0.6. Si GTOs and SiC GTOs reviewed in this paper have a value in the range of 0.6 and 0.8. The values $r_{\mathrm{v}} = \{0, 0.5, 0.8\}$ are chosen as test cases to reflect the variety of semiconductor types.

$$r_{\mathrm{v}} = \frac{V_{\mathrm{bi}}}{V_{\mathrm{tot,nom}}} \tag{4}$$

A simple way to compare the loss performance for the presented topologies, is via probability density functions, as done in [35]. The semiconductor characteristic in forward and reverse direction is assumed to be identical. Detailed loss calculations can be found in the Appendix. Two studies are conducted, covering two economic scenarios:

1) Semiconductor prices are high and it is to be determined which topology offers most benefits regarding power loss. The semiconductor expenditure per arm is kept constant among the cases and power loss $\mathcal{R}6$ is compared.
2) Electricity prices are high and the converter is designed with a target maximum loss in mind. The simulation is iterated until the target losses are obtained. The semiconductor expenditure $\mathcal{R}8$ and requirements regarding forward voltage drop are compared.

While switching losses can be reduced by improving modu-

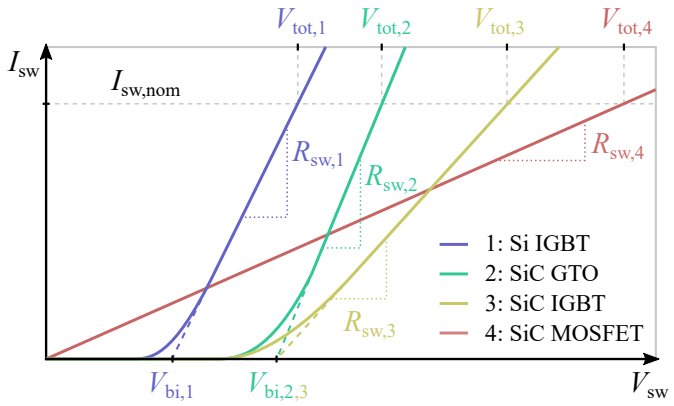


Fig. 9: Illustration of resistive voltage drop and built-in voltage for different semiconductor types: Si IGBT (typ. $r_{\text{v},1} = 0.5$), SiC GTO ($r_{\text{v},2} = 0.8$), SiC IGBT ($r_{\text{v},3} = 0.5$), SiC MOSFET ($r_{\text{v},4} = 0$).

TABLE III: Study cases for conduction losses, semiconductor expenditure, and target semiconductor forward voltage.

study	1)			2)		
r_{v}	0*	0.5†	0.8‡	0*	0.5†	0.8‡
$R_{\text{arm}} n_{\text{lvl}}$ [Ω]	0.23	0.12	0.05	— Fig. 12 —		
P_{cond}/S [%]	— Fig. 10, 11 —			0.5	0.5	0.5
V_{tot}				— Fig. 13 —		

* SiC MOSFET, † Si/SiC IGBT, ‡ SiC GTO

lation and capacitor voltage balancing techniques, conduction losses seem to be tied to the amount of semiconductors in a SM. A general consensus has been that increased SM functionality enabled by a higher semiconductor count leads to higher converter power loss. This is not true for some novel SM topologies, where parallel current paths are possible. The DZ and DCDZ feature a parallel connection of switches during bypass. For active power transfer, arm current is highest for low arm voltage (when most SMs are in bypass), hence, there are possible benefits regarding converter power losses ℛ6. Furthermore, redundant SMs in hot reserve (redundancy SMs which are active and can be used for additional capacitor voltage balancing capability) cause less losses, since they are mainly operated in bypass. The SFB and the DCDZ also parallel connect switches and capacitors in the switching states providing $+1V_{\text{c}}$ and $-1V_{\text{c}}$ reducing conduction losses for those states.

The converter conduction losses over k and over φ for the first study are shown in Fig. 10 and Fig. 11 respectively. The analysis is done for different r_{v}, in order to evaluate how the topologies perform with resistive semiconductors (e.g. SiC MOSFETs) and semiconductors with a certain content of built-in potential (e.g. IGBTs and GTOs). Looking at $r_{\text{v}} = 0$, SM topologies with parallel paths benefit, as seen clearly for the DCDZ and the CDZC3. The DCDZ provides similar functionality as a hybrid of 50 % HB and 50 % FB (HBFB), but features better capacitor voltage balancing and lower losses for $1 \leq k \leq 1.5$. The SFB, AC and HBFB show superior losses for reactive power at $\varphi = 90\,\text{deg}$. The DZ performs better than a FB for active power transfer, despite the extra switch. The clusters SFBC3 and CDZC3 have the lowest losses among all bipolar topologies.

For $r_{\text{v}} = 0.5$ and 0.8 the double-zero bypass of DZ, DCDZ, and CDZC3 can not unleash its full potential, due to the built-in potential of the semiconductor. Similarly, the losses for the PC are much higher than for $r_{\text{v}} = 0$. These topologies have increased losses for increased r_{v}. The SFB and the SFBC3 perform well regardless of the choice of semiconductor. The HB and the FC remain the loss benchmark, regardless of semiconductor type.

For the second study, the results can be found in Fig. 12 and Fig. 13. Fig. 12 shows the inverse of $R_{\text{arm}} n_{\text{lvl}}$, which can be seen as an indicator for the semiconductor expenditure, since it is proportional to the semiconductor area per converter arm. If a price for a certain resistance value is given for the different semiconductors, they can be directly compared. The characteristic corresponds to the one of the power losses in study 1). The scaling for semiconductor expenditure roughly corresponds to the inverse of r_{v} for most topologies, however topologies with parallel paths deviate from this rule.

In Fig. 13, the term $\{V_{\text{tot}} n_{\text{lvl}}\}$ is the required forward voltage drop, if the number of voltage levels per arm is given. For example, a HB MMC with $n_{\text{lvl}} = 400$, $k = 1$, and $r_{\text{v}} = 0.5$ (IGBT) may have a semiconductor with a maximum forward voltage drop $V_{\text{tot}} = 1\,\text{kV}/400 = 2.5\,\text{V}$. It can be seen that for $r_{\text{v}} = 0$ the permitted voltage drop is higher for topologies featuring parallel connection. For $r_{\text{v}} = 0.8$ the PC has the highest permitted V_{tot} among the unipolar SMs and the SFBC3 among the bipolar SMs. The DZ has a quite high normalized semiconductor count, therefore, as the benefit of paralleling is lost for high r_{v}, it becomes the most expensive solution requiring lowest V_{tot}.

B. Switching Losses

Switching losses occur when changing between SM switching states. This could either be due to the controller requesting a different arm voltage and the SM providing the voltage step, or due to capacitor voltage balancing. In the latter case, another SM must compensate for the change in arm voltage, causing additional switching losses. The capacitor voltage balancing, and modulation can be optimized for reducing switching losses [122], [156]–[163]. Furthermore, some SM topologies offer several states for a certain SM voltage. Different transitions between switching states may require a different amount of turn-on and turn-off processes, so that switching losses can be optimized choosing a suitable set of switching states. MMCs for grid applications employ a large amount of SMs, so that a good harmonic performance ℛ1 is possible without additional filters; even with low switching frequency. Nevertheless, switching losses can still account for a big part of the semiconductor losses ℛ6, depending on the optimization of the semiconductor devices. SiC MOSFETs offer fast switching transitions, so that the total power loss is expected to be governed mostly by conduction losses. The switching losses are shown in Fig. 14. The results are obtained via switching density functions similar to the procedure described for conduction losses. Only transitions between the SM

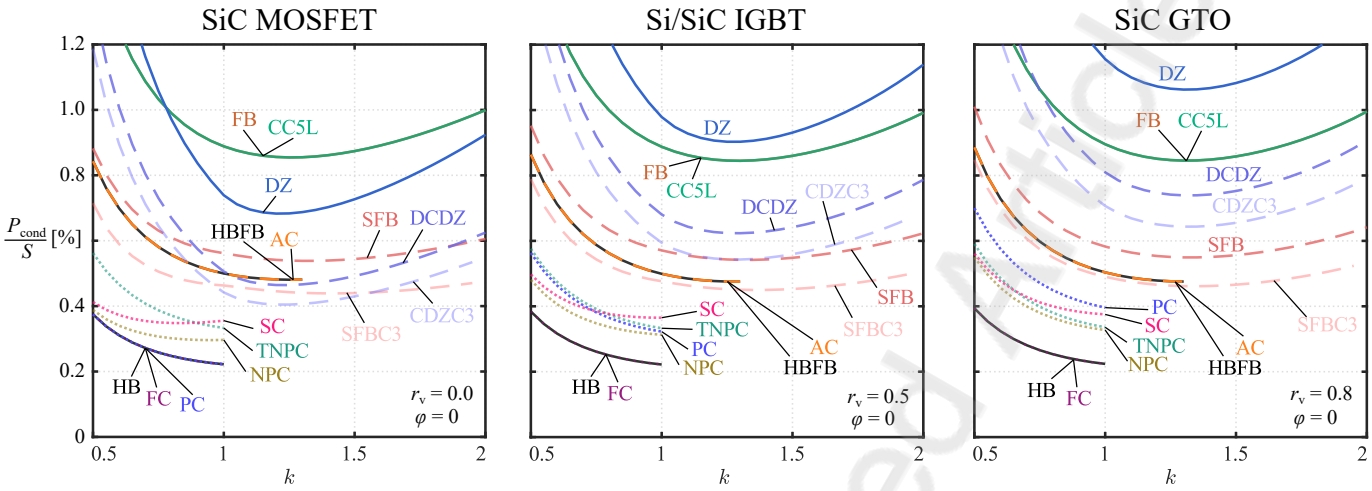


Fig. 10: Converter conduction losses over k. The semiconductor expenditure per arm is set constant.

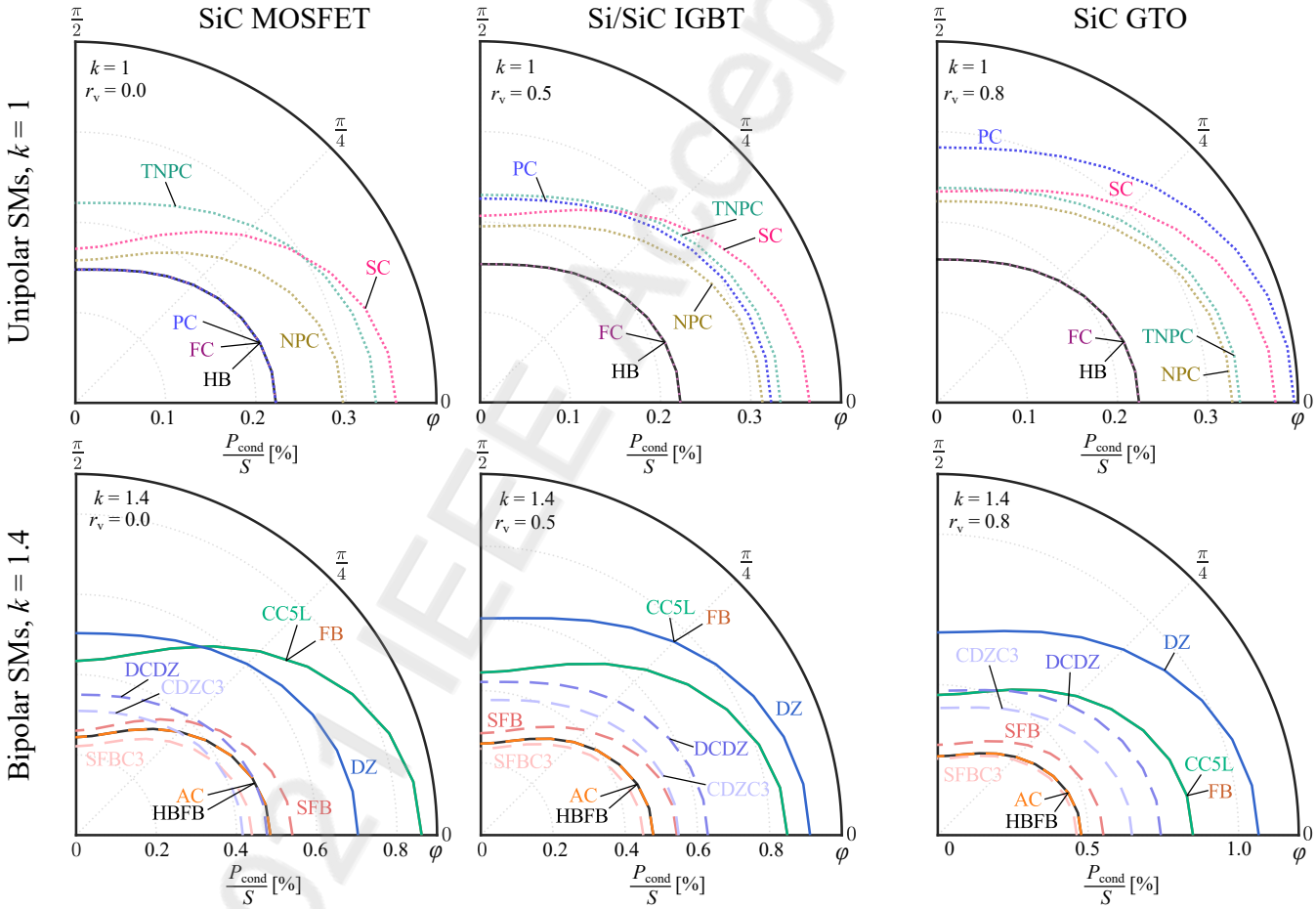


Fig. 11: Converter conduction losses over φ (with constant k). The semiconductor expenditure per arm is set constant.

states which are necessary to follow the reference arm voltage are considered. Additional balancing is not represented in this comparison, hence, the results should be taken as indication only. Switching losses of the semiconductors is assumed linear with current, so that parallel conduction paths result in reduced switching losses. Most of the topologies perform similarly well with their optimum being around $1 \leq k \leq 1.5$.

C. Switch Utilization

A good utilization of the power devices is desirable regarding cooling circuit design, and an even temperature distribution. It is possible to adjust the power device current rating for each switch, accounting for its utilization, but such designs become more complex, which not favorable. A measure for how well all SiC MOSFET switches are utilized

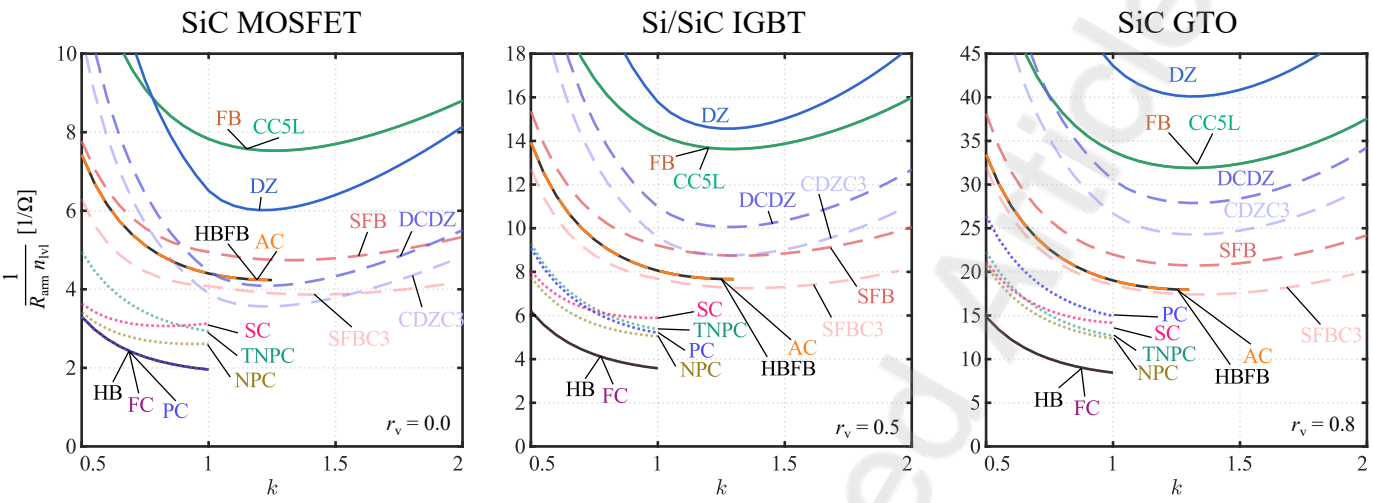


Fig. 12: Converter semiconductor expenditure $1/\{R_{\text{arm}} n_{\text{lvl}}\}$ for $r_{\text{v}} = \{0, 0.5, 0.8\}$ with conduction loss set to 0.5 % of S.

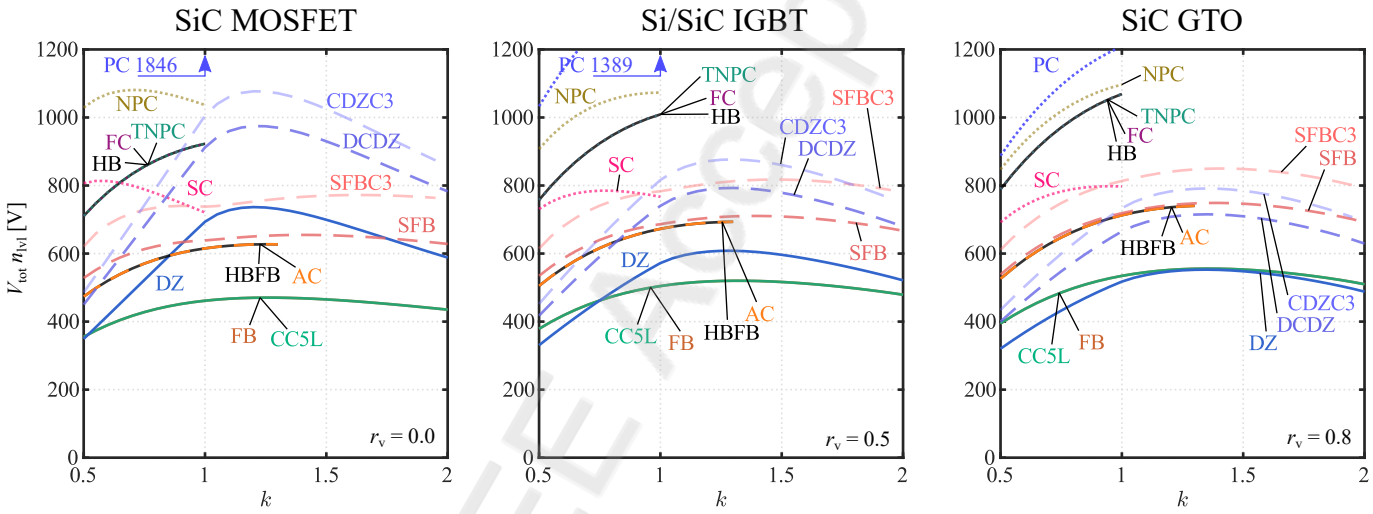


Fig. 13: Target total forward voltage drop $\{V_{\text{tot}} n_{\text{lvl}}\}$ for $r_{\text{v}} = \{0, 0.5, 0.8\}$, with conduction loss set to 0.5 % of S.

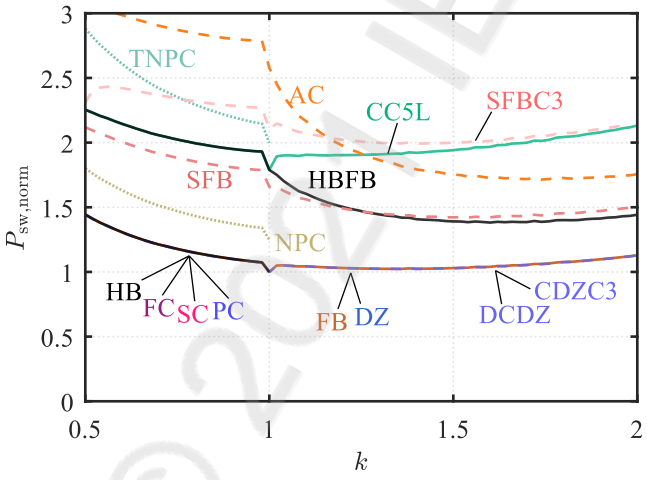


Fig. 14: Switching losses for different SMs, normalized to switching losses of HB at $k = 1$.

in a certain topology can be found by looking at the rms current distribution among the switches, expressed by η_{sm} in (5). Fig. 15 shows the result over k. Only the traditional topologies HB, FB, FC, and the PC are able to achieve a completely even distribution of the rms current among the switches. However, unipolar topologies peak far below $k = 1$, which is non-optimal in terms of losses R6 and energy storage requirements R9 [125]. Most of the bipolar topologies achieve their optimum current distribution around $k = 1.4$, with the exception of the SFB and the AC. The FB and the CC5L have a very even current distribution for that value.

$$\eta_{\text{sm}} = \frac{\sum_{x=1}^{n_{\text{sw}}} \frac{i_{\text{x,rms}}}{n_{\text{sw}}}}{max(i_{\text{x,rms}})} \tag{5}$$

V. Discussion

Based on the mentioned aspects of power semiconductor devices and SM topologies, the following discussion provides some proposals regarding the hardware design of the converter. Table IV summarizes the findings of this paper, showing which

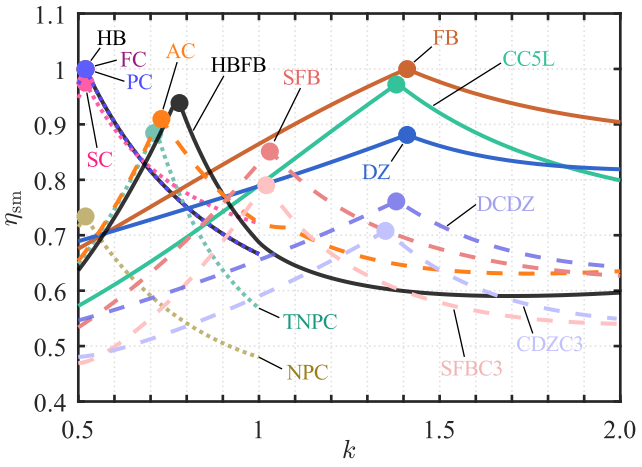


Fig. 15: Rms current distribution among all switches of a SM.

measures can be taken to address the technical requirements $\mathcal{R}1$–10. According to the evaluations and comparisons in this paper, the HB is still a very competitive option. However, HVdc transmission, especially with with overhead lines, and future HVdc grids may require bipolar capability of the SMs. The FB has high conduction losses and high switch count. Several alternatives to the FB with lower semiconductor expenditure, lower conduction losses, and additional features have already been presented. In the following, promising design approaches are discussed.

1) Reliable, Air-Cooled Converter (SiC MOSFET; HB): For certain applications, fast dc breakers and robust $\mathcal{R}3$ power devices might be sufficient for dc fault handling $\mathcal{R}2$ and resulting surge currents. In that case, the classical HB might still be the most viable option, due to its simplicity $\mathcal{R}5$ and low power loss $\mathcal{R}6$. Parallel connection of SiC MOSFETs allows to reduce conduction losses arbitrarily, which is not possible with Si IGBTs due to their built-in potential. Even if efficiency $\mathcal{R}6$ is not of major concern, power loss reduction may enable different cooling solutions. Eliminating the need for liquid cooling and replacing it with an air-cooled heatsink could be an interesting option. This requires overrating of power devices, and high temperature capability of semiconductors and packaging. Already today, SiC MOSFET modules can be operated at 175 °C and additional developments could push that limit even further. Furthermore, the overrated power device would not have issues handling dc fault surge currents. Due to economy of scale effects, a severe cost reduction for SiC MOSFET modules in the next years is possible. The increased semiconductor expenditure for such a design approach would have to be weighed against its benefits, i.e., cost reduction for cooling €, decreased complexity $\mathcal{R}5$, and increased reliability.

2) Low Complexity Converter with Large-Sized SMs (SiC bipolar; SFB or HBFB): UHV bipolar SiC devices enable high SM voltage, reducing the amount of required SMs per MMC arm. This is similar to the concept of cascaded 2-level converters [27], with the difference that switches can be realized with a single power device instead of a series connection. This would greatly reduce the amount of gate drivers, sensors, communication fibers, and structural components, with the possible benefit of reduced converter complexity $\mathcal{R}5$ and, therefore, increased reliability. Robustness and reliability of UHV SiC IGBTs and GTOs is to be investigated when they become available. Bipolar voltage capability of the SM topology would be advisable, to avoid excessive surge currents through the power devices. A good option would be the SFB. Major blockers for UHV bipolar devices could be the required high-power density packaging and the reduction of active area due to the required JTE. Since MMC voltage rating can be scaled independently from power device voltage, it remains to be seen if such UHV SMs are competitive with SMs of lower voltage.

3) Fault-Ride-Through MMC for HVDC Grids (SiC MOSFET; DZ, DCDZ or SFB): Reasons for choosing a bipolar topology could be the need for dc fault handling capability $\mathcal{R}2$ with quick recovery, as required for HVdc overhead lines and grids. Additionally, the converter can operate at $M = \sqrt{2}$, reducing energy storage requirements $\mathcal{R}9$. The state-of-the-art solution with FBs employing Si IGBTs can provide such a functionality. However, advanced SM topologies employing SiC MOSFETs offer a variety of advantages and improvements. The DZ, the SFB, and the DCDZ are promising alternatives to the FB, and unfold their full potential with SiC MOSFETs. They feature parallel conduction paths in certain switching states, resulting in significant conduction loss reduction $\mathcal{R}6$. The DZ should be chosen if full bipolar capability is required. The SFB and the DCDZ compromise on half of the negative voltage capability in favour of a reduced switch count $\mathcal{R}8$. Both feature internal capacitor voltage balancing, and enable reducing the capacitor size $\mathcal{R}9$. Another advantage of the DZ and the DCDZ is the increased robustness against SM-internal faults $\mathcal{R}4$. These advantages might compensate for the increased price of SiC MOSFETs, compared to Si IGBTs. Such designs can be realized with already available 1.2–3.3 kV SiC MOSFETs, if WBMs with higher current rating are developed.

4) MMC with 15 kV SiC SMs (SiC MOSFET; DZ, DCDZ or SFB): A combination of previously discussed advantages can be achieved with SiC MOSFETs with high blocking voltage. Predictions see the maximum feasible voltage of SiC MOSFETs at 10–15 kV. A prototype with reduced current capability, solving challenges regarding EMI and $\mathrm{d}v/\mathrm{d}t$ has already been demonstrated in [58]. A 15 kV SiC MOSFET would enable SM voltages of approximately 7.5 kV, reducing the amount of SMs per converter arm by a factor of 5, compared to state-of-the-art 1.5 kV SMs. In combination with the DZ, the DCDZ, or the SFB topology, such an SM design would feature a combination of the advantages described for the previous two approaches. This would address almost all of the requirements in Table I. Remaining blockers and challenges are the required current rating of such 15 kV SiC MOSFET WBMs, their robustness, cost, and availability.

5) Further Discussion: The SFBC3 and the CDZC3 are more complex topologies with reduced bipolar capability, i.e. $r_{\mathrm{bip}} = 1/3$, and are able to operate at $M \leq 2$. However, dc faults can only be handled if $M \leq 0.5$. As seen in Fig. 12,

TABLE IV: Summary of measures addressing HVdc converter technical requirements.

#	Requ.	Semiconductor	Power Device	Valve	Submodule
$\mathcal{R}1$	Sufficient harmonic performance	– Low switching-loss enabling higher f_{sw} for tracking of current waveform			– Sufficient voltage levels per arm
$\mathcal{R}2$	Dc-side fault handling	– Surge current capability of free-wheeling diode or MOSFET body diode	– Robust, bondwire-less packaging, for handling surge currents		– Bipolar SMs, counteracting loss of voltage on dc-terminal
$\mathcal{R}3$	Robust-ness	– Surge current capability – Short-circuit capability	– Surge current capability – Short-circuit capability		
$\mathcal{R}4$	Internal fault handling	– Technologies avoiding temperature sensitive gate oxide structure – SCFM avoiding device explosion	– Driver with short circuit protection – SCFM	– Redundancy via series connection (SCFM required)	– >1 off-state switch between capacitor terminals – Explosion-proof housing – Additional fuse
$\mathcal{R}5$	Low complexity	– UHV bipolar SiC devices, reducing the amount of SMs per arm		– Avoid series or parallel connection of power semi-conductor devices	– Large high-voltage SMs, reducing the amount of SMs per arm – SM topology (Table II)
$\mathcal{R}6$	High efficiency	– UHV bipolar SiC devices with low on-state voltage – SiC MOSFETs	– Parallel-connection of SiC MOSFETs (e.g. M-PP or parallel WBMs)		– Parallel current paths (Table II) – Unipolar SMs – $M > 1$ for bipolar SMs
$\mathcal{R}7$	Maintain-ability		– Multiple-sources for parts, e.g. widely available WBM		– Low complexity SM topology (Table II)
$\mathcal{R}8$	Low semi-conductor expenditure	– Low-cost Si IGBTs	– Low-cost WBM		– SM topology (Fig. 12)
$\mathcal{R}9$	Low energy storage				– SMs with parallel capacitors (Table II) – bipolar SMs at $M = \sqrt{2}$
$\mathcal{R}10$	Small footprint		– High current devices, trading voltage for current, reducing required clearances		– Lower energy storage requirements, reducing capacitor volume and weight

these SMs have the lowest semiconductor expenditure $\mathcal{R}8$ or losses $\mathcal{R}6$ among bipolar topologies. For converters with a target operation point at $1 < M \leq 2$ and dc breakers this might still be a viable option for point-to-point transmission. The SFB and the SFBC3 feature parallel conduction paths for $+1V_{\mathrm{c}}$ and $-1V_{\mathrm{c}}$, which leads to further reduced power loss $\mathcal{R}6$ for reactive power, as shown in Fig. 11. This could be very interesting for converters offering reactive power compensation for connected ac grids $\mathcal{R}1$. Additionally, the SFB can be controlled by three signals only (the SFBC3, by only four). Looking at a whole arm, this means that fewer switching signals are required as compared to a FB implementation. However, both topologies seem to have high switching losses.

VI. Conclusion

HVdc VSCs play an important role in applications like subsea interconnections, off-shore wind power integration, future HVdc grids, interconnections of asynchronous systems, and city center infeed. These systems are foreseen to become a vital part of our electricity grid, and potentially enable a worldwide interconnection, a global electricity grid. In these applications, grid code compliance, high reliability, and low cost are of vital importance. However, the relevance of the technical requirements $\mathcal{R}1$–10 might differ depending on the application. Developments in power semiconductor device technology and submodule topologies offer benefits for these requirements.

In order to unleash the full potential of SiC power semiconductor devices in HVdc transmission, SM topologies and design need to be revised. The comparisons and evaluations provided in this article do not represent an exhaustive study.

Rather, they contribute to identifying benefits, trade-offs, and synergies for various SM designs with different power semiconductor devices.

The main advantages of SiC MOSFETs and future UHV bipolar SiC devices are higher voltage capability, reduced conduction losses, and higher operation temperatures. This enables converters with reduced complexity $\mathcal{R}5$ and increased efficiency $\mathcal{R}6$. Remaining challenges for SiC MOSFETs are higher power density packaging solutions, reliability and robustness, availability, and cost reduction. Switched bipolar SiC devices are not yet commercially available. The initial challenges for the realization of future UHV SiC power semiconductor devices are insulation and cooling, and they require novel packaging solutions.

When it comes to simplicity $\mathcal{R}5$ and efficiency $\mathcal{R}6$, the HB is hard to beat. In these two aspects it outperforms any other SM topology, independent of the semiconductor type. However, two developments might justify the need for other SM topologies: future HVdc grids might require dc fault-ride-through capability $\mathcal{R}2$; and reduced energy storage $\mathcal{R}9$ might be a requirement, motivated by weight-, volume-, and cost constraints.

Several design approaches, representing viable alternatives to the classic FB or HB with Si IGBTs, have been proposed in the discussion. Great potential can be seen for bipolar SM topologies with parallel conduction paths, such as the DZ, the SFB, and the DCDZ. In combination with SiC MOSFETs, they offer a conduction loss reduction of 20 %, 28 %, and 44 % respectively, compared to the FB (assuming equal semiconductor area). For SiC bipolar devices, the SFB is the preferred option, with a loss reduction of approximately 35 %, compared to the FB. Furthermore, such advanced SM topologies offer additional features, e.g., tailored bipolar capability $\mathcal{R}2$, an additional switch in series to the capacitor $\mathcal{R}4$, reduced semiconductor count $\mathcal{R}8$, and internal capacitor voltage balancing.

Appendix
Converter Waveforms and Loss Calculations

The conduction losses in a semiconductor device are caused by resistive voltage drop (subscript r), and constant voltage drop (subscript v):

$$\begin{aligned} p_{\mathrm{cond,sw}} &= p_{\mathrm{cond,sw,v}} + p_{\mathrm{cond,sw,r}} \\ &= V_{\mathrm{bi}}|i_{\mathrm{sw}}| + R_{\mathrm{sw}} i_{\mathrm{sw}}^2 \end{aligned} \tag{6}$$

R_{sw} resistance of semiconductor switch
V_{bi} built-in potential of semiconductor switch
i_{sw} current through semiconductor switch

In the following the subscript *cond* is dropped for readability. The subscripts indicating arm values, SM values, and switch values are *arm*, *sm*, and *sw* respectively. For a comparison of converter designs it is sufficient to consider one arm only.

The converter arm losses p_{arm} are chosen as output variable. As input variable, a term reflecting the converter semiconductor expenditure is chosen, i.e. the semiconductor area per arm. For the simplicity of the nomenclature, we choose the combined resistance of the semiconductors in the converter arm, R_{arm}, which is inversely proportional to the semiconductor area per arm. Thus, the parallel connection of all semiconductors in one arm is expressed as R_{arm}. Furthermore, a parameter determining which type of semiconductor is used is added, i.e. r_{v} as defined in Fig. 9 and (4). Following (6) we pursue to find an expression for the arm losses:

$$p_{\mathrm{r,arm}} = f\left(R_{\mathrm{arm}}, i_{\mathrm{arm}}, \mathbb{P}\right) \tag{7}$$

$$p_{\mathrm{v,arm}} = f\left(R_{\mathrm{arm}}, r_{\mathrm{v}}, i_{\mathrm{arm}}, \mathbb{P}\right). \tag{8}$$

$\mathbb{P}$ probability function of switches conducting i_{arm}

The combined resistance of one SM, R_{sm}, and the resistance of one switch, R_{sw}, scale as

$$R_{\mathrm{arm}} = R_{\mathrm{sm}} \frac{n_{\mathrm{Vc,pos}}}{s_{\mathrm{arm}}\ n_{\mathrm{lvl}}} = R_{\mathrm{sw}} \frac{1}{n_{\mathrm{sw}}} \frac{n_{\mathrm{Vc,pos}}}{s_{\mathrm{arm}}\ n_{\mathrm{lvl}}} \tag{9}$$

with

$$s_{\mathrm{arm}} = \frac{V_{\mathrm{arm,max}}}{V_{\mathrm{dc}}} = \frac{1+k}{2}. \tag{10}$$

$n_{\mathrm{Vc,pos}}$ positive voltage levels of SM topology
n_{sw} switch count of SM topology
n_{lvl} arm voltage levels (excl. effect of k)
s_{arm} arm voltage scaling due to k

With (9) and a current reference point, e.g., nominal rms arm current, V_{bi} can be determined:

$$\begin{aligned} V_{\mathrm{bi}} &= \frac{r_{\mathrm{v}}}{1-r_{\mathrm{v}}} R_{\mathrm{sw}} I_{\mathrm{arm,rms,ref}} \\ &= \frac{r_{\mathrm{v}}}{1-r_{\mathrm{v}}} \frac{s_{\mathrm{arm}}}{n_{\mathrm{Vc,pos}}\ n_{\mathrm{sw}}} \{R_{\mathrm{arm}} n_{\mathrm{lvl}}\} I_{\mathrm{arm,rms,ref}} \end{aligned} \tag{11}$$

The arm losses can be calculated by (12)–(14), where $\mathbb{P}_{\mathrm{sw,x}}$ represents the probability to conduct i_{arm} for switch x.

$$\begin{aligned} p_{\mathrm{arm}} &= \frac{n_{\mathrm{lvl}}\ s_{\mathrm{arm}}}{n_{\mathrm{Vc,pos}}}\ p_{\mathrm{sm}} \\ &= \frac{n_{\mathrm{lvl}}\ s_{\mathrm{arm}}}{n_{\mathrm{Vc,pos}}} \sum_{x=1}^{n_{\mathrm{sw}}} p_{\mathrm{sw,x}} \end{aligned} \tag{12}$$

$$\begin{aligned} \left\{\frac{p_{\mathrm{r,arm}}}{n_{\mathrm{lvl}}}\right\} &= \frac{s_{\mathrm{arm}}}{n_{\mathrm{Vc,pos}}} \sum_{x=1}^{n_{\mathrm{sw}}} R_{\mathrm{sw}}\ i_{\mathrm{sw,x}}^2 \\ &= \frac{s_{\mathrm{arm}}^2}{n_{\mathrm{Vc,pos}}^2} \sum_{x=1}^{n_{\mathrm{sw}}} \{R_{\mathrm{arm}} n_{\mathrm{lvl}}\}\ i_{\mathrm{arm}}^2\ \mathbb{P}_{\mathrm{sw,x}} \end{aligned} \tag{13}$$

$$\begin{aligned}\left\{\frac{p_{\mathrm{v,arm}}}{n_{\mathrm{lvl}}}\right\} &= \frac{s_{\mathrm{arm}}}{n_{\mathrm{Vc,pos}}}\sum_{x=1}^{n_{\mathrm{sw}}} V_{\mathrm{bi}}\ |i_{\mathrm{sw,x}}| \\ &= \frac{s_{\mathrm{arm}}}{n_{\mathrm{Vc,pos}}}\sum_{x=1}^{n_{\mathrm{sw}}} V_{\mathrm{bi}}\ |i_{\mathrm{arm}}|\ \mathbb{P}_{\mathrm{sw,x}}\end{aligned} \tag{14}$$

It is desirable to make a comparison which is independent of the choice of n_{lvl} (i.e. the nominal voltage of the semiconductor device, valve, or SM). Therefore, (11), (13), and (14) are arranged so that $\{R_{\mathrm{arm}} n_{\mathrm{lvl}}\}$ is chosen as input variable, and $\{\frac{p_{\mathrm{r,arm}}}{n_{\mathrm{lvl}}}\}$ as output variable. Furthermore, note that in (13) the semiconductor parameter is the combined arm resistance R_{arm}, whereas in (14) it is the semiconductor built-in voltage V_{bi}.

The arm current is calculated analytically according to the equivalent circuit, shown in Fig. 16, and (15)–(16).

$$\hat{V}_{\mathrm{ac}} = M\tfrac{V_{\mathrm{dc}}}{2}, \quad 0 \le M \le k \tag{15}$$

$$\begin{aligned} i_{\mathrm{arm}} &= \frac{I_{\mathrm{dc}}}{3} + \frac{i_{\mathrm{ac}}}{2} \\ &= \frac{I_{\mathrm{dc}}}{3} + \frac{\hat{I}_{\mathrm{ac}}}{2}\cos(\omega t - \varphi) \\ &= \frac{S\cos(\varphi)}{3V_{\mathrm{dc}}} + \frac{S}{3\hat{V}_{\mathrm{ac}}}\cos(\omega t - \varphi) \end{aligned} \tag{16}$$

$\hat{V}_{\mathrm{ac}}$	peak ac voltage
M	modulation index
V_{dc}	dc voltage
I_{dc}	dc current
i_{ac}	ac current
$\hat{I}_{\mathrm{ac}}$	peak ac current
φ	power angle
S	converter power

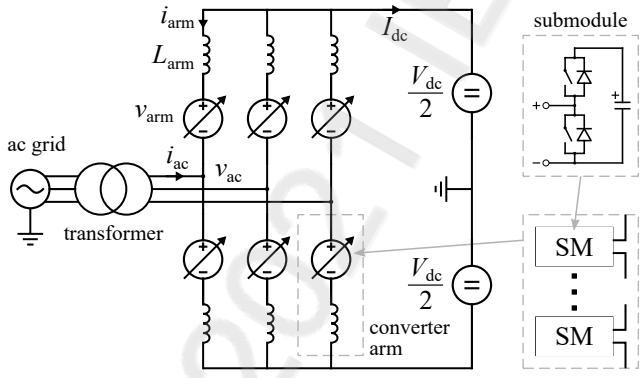


Fig. 16: Simplified equivalent circuit of MMC (symmetrical monopole) connected to ac-grid via transformer, and converter arms, consisting of SMs and arm inductor.

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