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Research Article

Comparative Simulation Analysis of Process Parameter Variations in 20 nm Triangular FinFET

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Technology scaling below 22 nm has brought several detrimental effects such as increased short channel effects (SCEs) and leakage currents. In deep submicron technology further scaling in gate length and oxide thickness can be achieved by changing the device structure of MOSFET. For 10–30 nm channel length multigate MOSFETs have been considered as most promising devices and FinFETs are the leading multigate MOSFET devices. Process parameters can be varied to obtain the desired performance of the FinFET device. In this paper, evaluation of on-off current ratio (I_{on}/I_{off}), subthreshold swing (SS) and Drain Induced Barrier Lowering (DIBL) for different process parameters, that is, doping concentration (10^{15}/cm^3 to 10^{18}/cm^3), oxide thickness (0.5 nm and 1 nm), and fin height (10 nm to 40 nm), has been presented for 20 nm triangular FinFET device. Density gradient model used in design simulation incorporates the considerable quantum effects and provides more practical environment for device simulation. Simulation result shows that fin shape has great impact on FinFET performance and triangular fin shape leads to reduction in leakage current and SCEs. Comparative analysis of simulation results has been investigated to observe the impact of process parameters on the performance of designed FinFET.

1. Introduction

To continue with the pace of Moore's law, reduction in transistor dimensions causes very significant short channel effects in device. Methods like (i) variable threshold CMOS, (ii) multithreshold CMOS, (iii) transistor stacking, and (iv) power gating are available to reduce the leakage current to some extent but are not suitable for technologies below 22 nm. FinFETs are considered as most promising device to reduce SCEs and leakage. FinFET is chosen to replace conventional planar CMOS devices below 22 nm [1, 2]. FinFET is a multigate transistor, in which gate is wrapped around the silicon fin channel. Better electrical control is provided by the wrap-around gate structure and thus leakage current and short channel effects are reduced.

FinFET has several advantages compared to planar devices such as well suppressed short channel effects, reduced subthreshold swing (~70 mV/dec), and small threshold voltage roll-off [3]. Rectangular cross section fins are commonly used for design and analysis of FinFET but they are rarely found in industry. In industries, cross section of FinFET is nonuniform and is similar to trapezoidal shape [4]. In a rectangular or trapezoidal FinFET top fin width can be decreased up to minimum possible value to get triangular FinFET keeping all other parameters the same as those of rectangular or trapezoidal FinFET. Hence, shape of fin is approximately triangle in triangular FinFET.

Triangular fin cross section and 3D schematic representation of triangular FinFET are shown in Figure 1. In this paper, evaluation of on-off current ratio (I_{on}/I_{off}), subthreshold swing (SS), and Drain Induced Barrier Lowering (DIBL) for various process parameters, that is, doping concentration (N_{ch}), oxide thickness (T_{ox}), and fin height (H_{fin}), has been presented for 20 nm triangular FinFET device.

In deep submicron technology, quantum effects become significant. Hence, density gradient model is used in design simulation which incorporates the considerable quantum

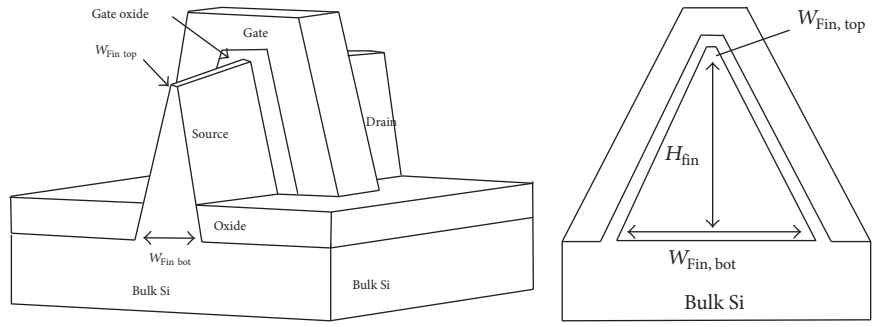


Figure 1: Triangular FinFET. (a) 3D schematic representation. (b) Triangular fin cross section of FinFET.

effects. By considering the quantum effects, more practical environment is provided for device simulation.

This paper has been formulated as follows. Section 2 presents the earlier work on FinFETs. Subsequent section explains the device design and simulation setup. Results have been discussed in Section 4. Conclusion of the work has been presented in Section 5.

Table 1: Geometry of designed FinFET.

SN	FinFET parameters	Value
(1)	Top fin width (nm)	1
(2)	Bottom fin width (nm)	15
(3)	Oxide thickness (nm)	1
(4)	Fin height (nm)	10 to 40
(5)	Doping concentration (/cm^3)	10^{15} to 10^{18}

2. Literature Review

In deep submicron technology further downscaling in gate length and oxide thickness can be achieved by varying the device structure of MOSFET. For 10–30 nm channel length double-gate MOSFET (DG-MOSFET) has been considered as most promising device. FinFET process parameters such as T_{ox}, H_{fin}, N_{ch}, fin width (W_{fin}), and gate length (L_{gate}) highly affect the performance of the device. These process parameters can be varied to achieve the desired performance of the FinFET device such as high on-off current ratio, low DIBL, and low SS. The fin thickness should be kept less than 1/3 of channel length to reduce SCEs [5]. Due to reduction in SCEs and leakage performance is improved in bulk FinFETs compared to planar CMOS. Reduction in fin width leads to decrement in leakage due to SCEs. By optimizing input process parameters for a 22 nm triangular FinFET leakage current can be reduced up to 70% as compared to rectangular fin shape with same base fin width [6]. To overcome the gate oxide leakage current in CMOS devices high-k gate stack is used. With high-k gate stack, gate-to channel capacitive coupling can also be improved without any reduction in the gate oxide layer. Variation in work function leads to variation in threshold voltage and it is identified as the main hurdle in scaling of CMOS technology. Below 22 nm technology, due to nonrectangular fin shape, for quantitative estimation of the work-function variation, the work-function values of metallic gate are randomized. Dependence of threshold voltage (V_{th}) on work function can be reduced by 30% for FinFET devices [7]. To characterize Trigate FinFET devices, no complete analytical model is published; in most of the literature, experimental or simulation results are presented. Developing compact model for FinFETs is a very challenging task due to 3D structure and ultrasmall dimensions [3].

Due to presence of the wrapped gate over three sides of semiconductor channel in FinFET devices, the electrostatic control of the gate is improved and several problems of planar transistors are solved. Compact models are one of the important components in circuit simulators which establish a link between the device technology and circuit designers. For different doping concentrations rectangular FinFETs can be accurately modelled [4]. Compared to rectangular fin shape triangular fin cross section reduces the SCEs to a greater extent [2]. The body of bulk FinFET should be lightly doped or undoped, to achieve similar on-state performance in Silicon on Insulator (SOI) and bulk FinFET [8]. In FinFETs, immunity to SCE decreases with increase in H_{fin}. It leads to good subthreshold slope and more significant DIBL. Sidewall angle which can be achieved from a particular process limits the fin height [9].

3. Device Design and Simulation Setup

3.1. Device Design Parameters and Material Composition. FinFET of triangular fin shape with 20 nm channel length is designed on Cogenda's GDS2Mesh 3D construction Technology Computer Aided Design (TCAD) tool [10]. The geometrical dimensions used in design are listed in Table 1. Si is used for substrate and fin, and high-k dielectric Hafnium Oxide is used as gate oxide. Device design is shown in Figure 2.

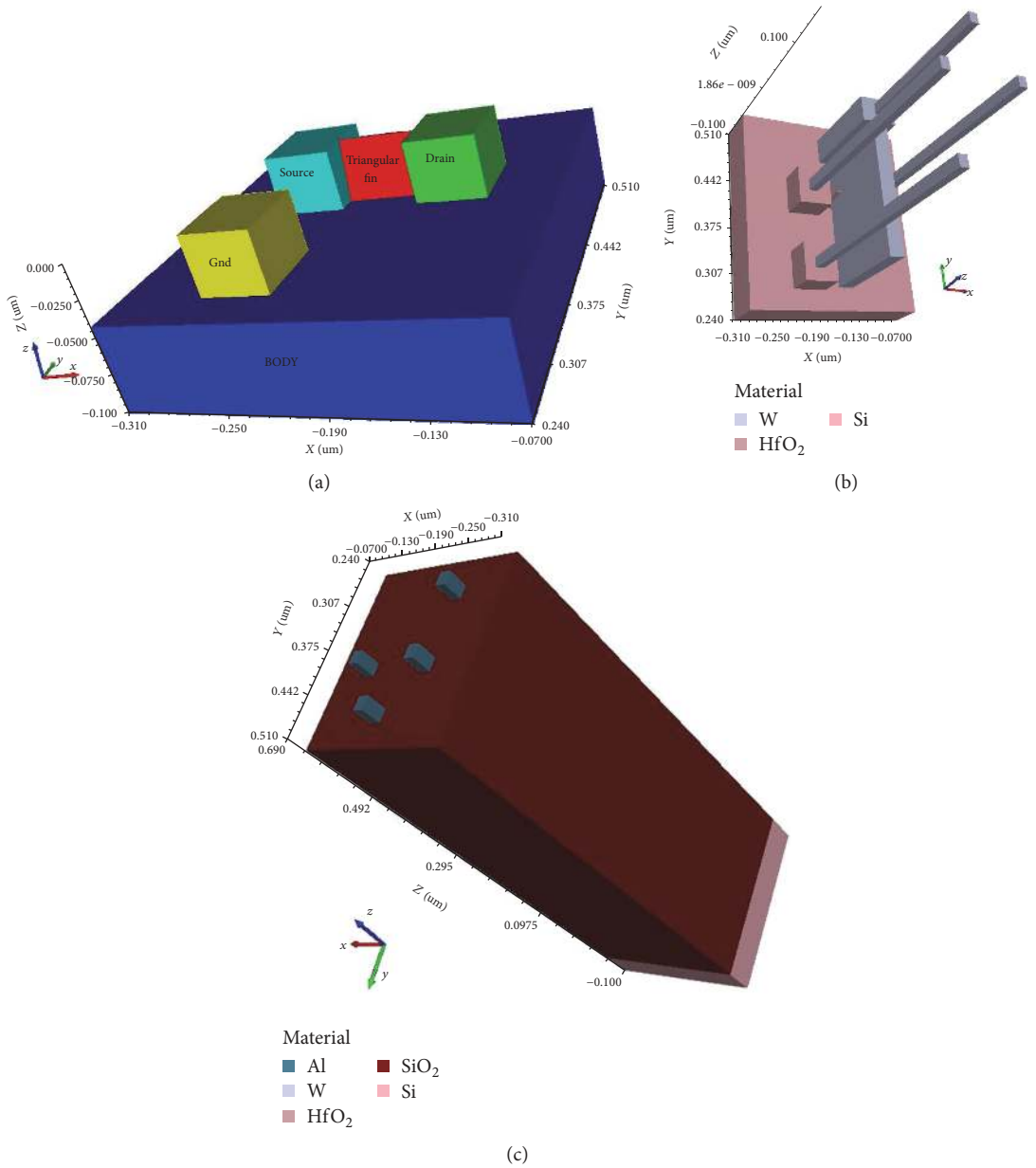


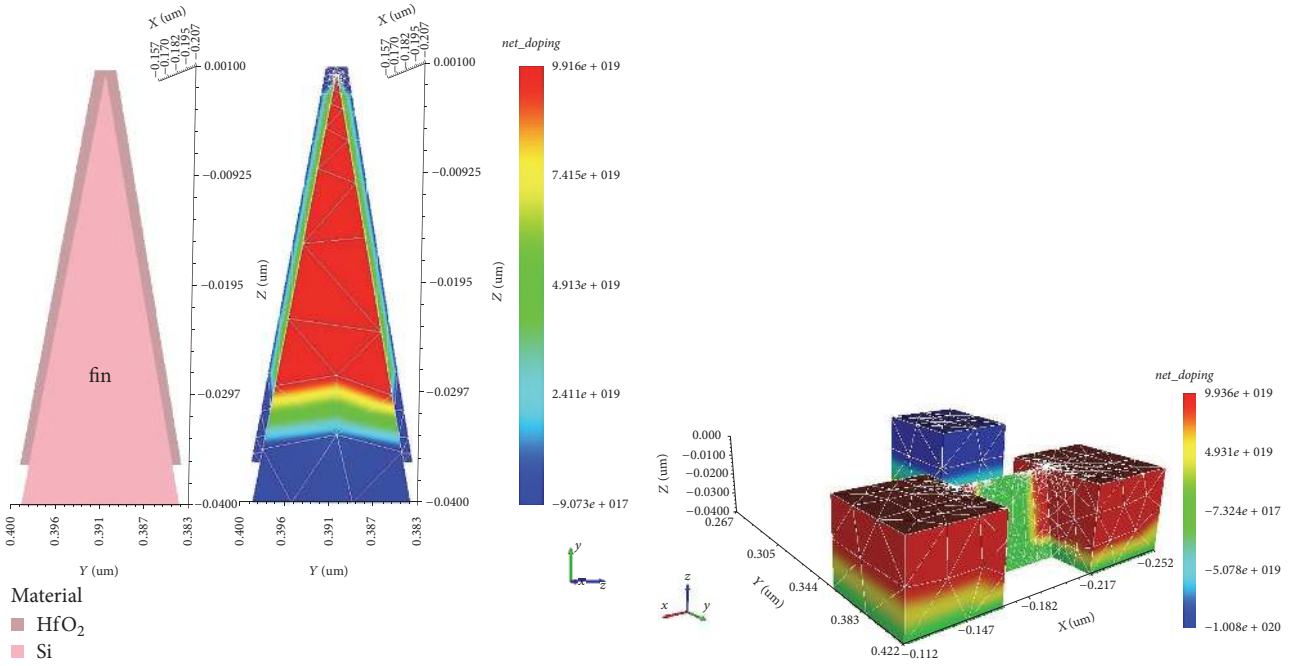
FIGURE 2: Bird's eye view of 3D triangular FinFET device. (a) Active region with triangular fin. (b) Internal view with active region material. (c) Complete device 3D structure.

3.2. Simulation Setup. In this work, triangular FinFET has been simulated at 20 nm gate length for varying H_{fin} and doping using Cogenda's Visual TCAD [11]. In nanoscale devices, quantum effect becomes significant due to very small device size. For such kind of device classical physics model is not suitable for analysis. Hence, quantum physics model is used while simulating the device. The TCAD simulations include density gradient quantum correction model for quantum effects consideration.

An additional quantum potential is included in density gradient (DG) model for calculating the driving force of electrons and holes [10, 11]. The electron and hole quantum correction equation included in simulation is shown as follows [12]:

$$\Lambda_n = -\frac{\hbar^2 \gamma n}{6qm_n^*} \frac{\nabla^2 \sqrt{n}}{\sqrt{n}}$$
$$\Lambda_p = \frac{\hbar^2 \gamma p}{6qm_p^*} \frac{\nabla^2 \sqrt{p}}{\sqrt{p}}, \quad (1)$$

where $\hbar$ is reduced Planck's constant (i.e., $h/2\pi$), m_n^* and m_p^* are the electron effective mass and hole effective mass, respectively, n and p are the electron concentration in



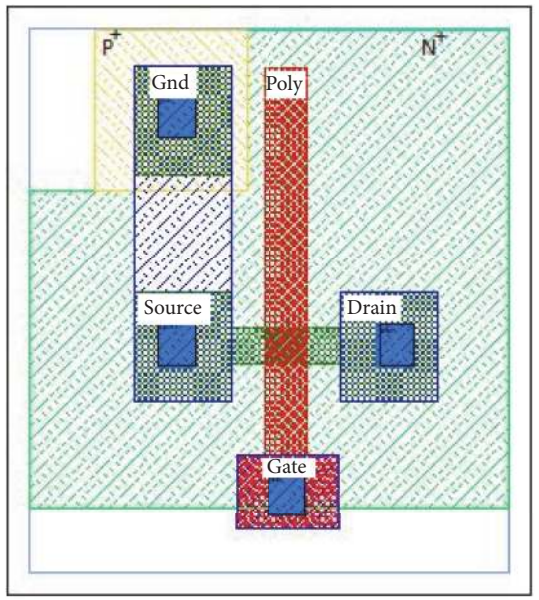


FIGURE 3: Triangular FinFET. (a) Triangular fin material and net doping in triangular fin. (b) Net doping in active region. (c) Mask of designed FinFET.

conduction band and hole concentration in valence band, respectively, and q is electron charge.

For Fermi-Dirac statistics, the electron and hole concentration at Ohmic boundaries must be adjusted as per [12]

$$n = N_c F_{1/2}\left(\frac{E_F - E_{c,\text{eff}} - \Lambda_n}{K_b T}\right)$$
$$p = N_v F_{1/2}\left(\frac{E_{v,\text{eff}} - \Lambda_p - E_F}{K_b T}\right), \quad (2)$$

where K_b is Boltzmann's constant, T is temperature, N_c is effective density of states (DOS) for electrons in conduction band, N_v is effective density of states (DOS) for holes in valence band, and E_F, $E_{c,\text{eff}}$, and $E_{v,\text{eff}}$ represent fermi level, conduction band edge, and valence band edge, respectively.

Consideration of quantum effects provides more practical environment to design simulation. Net doping profile for fin and active region is shown in Figure 3. Fin height is varied from 10 nm to 40 nm and doping is varied from $10^{15}/\text{cm}^3$ to

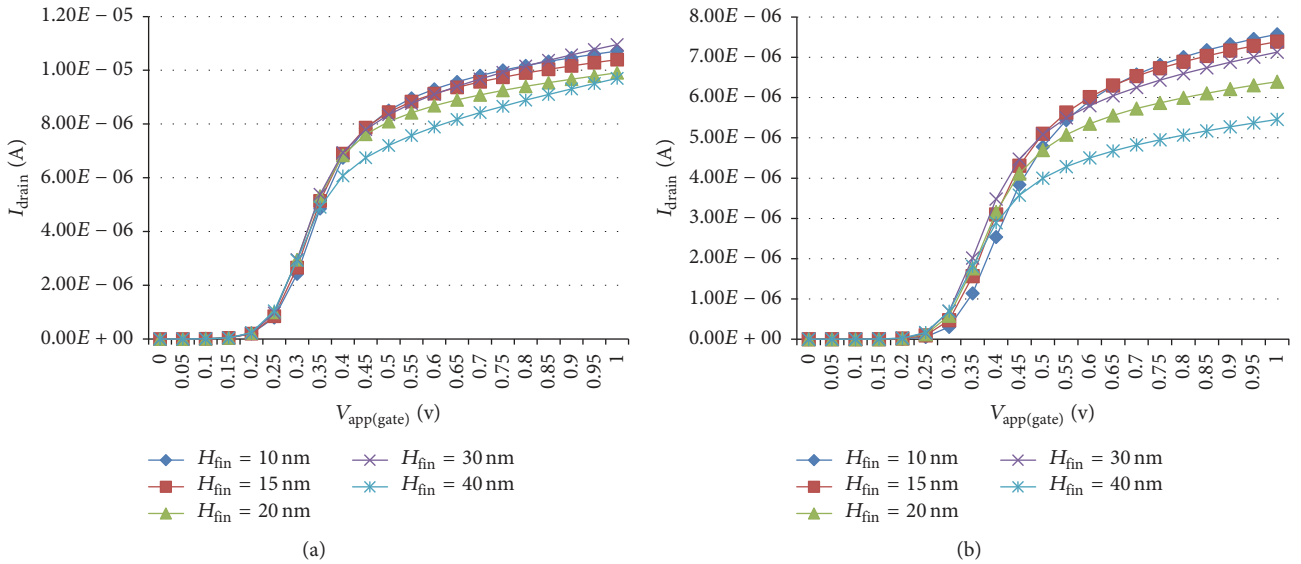


Figure 4: Transfer characteristics of triangular FinFET. (a) For low doping level (10^{15}/cm^3). (b) For high doping level (10^{18}/cm^3).

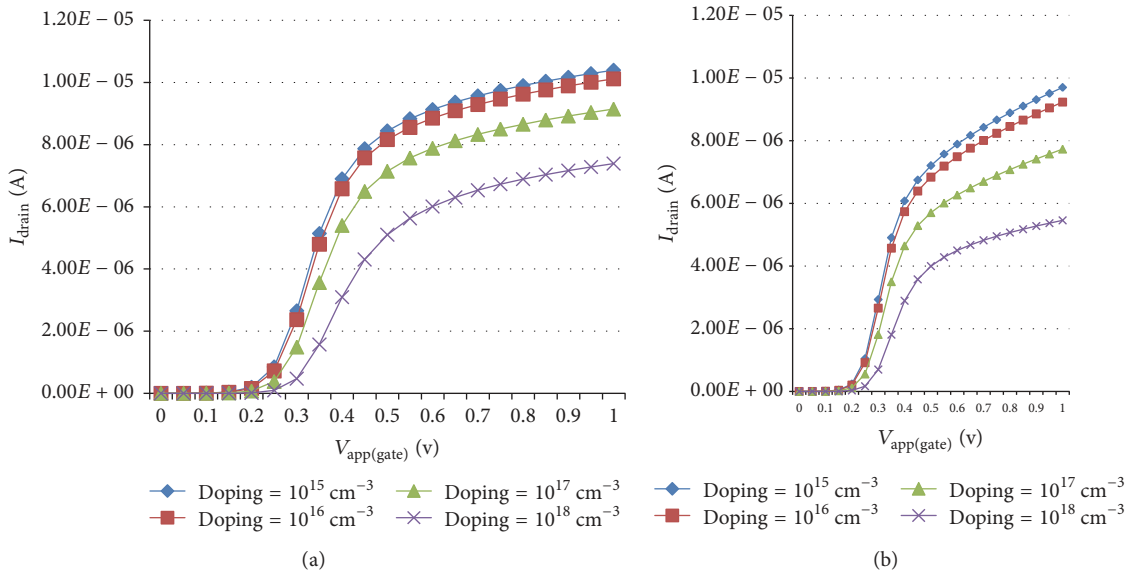


Figure 5: Transfer characteristics of triangular FinFET. (a) For 15 nm fin height. (b) For 40 nm fin height.

10^{18}/cm^3 for oxide thickness of 1 nm. The impact of doping and fin dimensions like fin height (H_{fin}) on output parameters of FinFET is investigated using TCAD tool. Evaluation of fin height and fin doping concentration corresponding to better device performance is presented.

4. Results and Discussion

Simulation results show that drain current of the triangular FinFET at drain voltage 50 mV decreases with H_{fin} at constant doping concentration of 10^{15}/cm^3 and 10^{18}/cm^3 as shown in Figure 4. Variation of drain current with doping is evaluated for different values of fin height. Drain current decreases with increase in doping level for constant H_{fin} of 15 nm and 40 nm as shown in Figure 5. High channel doping causes more impurity scattering in the crystal and the consequence is that carrier mobility gets reduced, thus resulting in low drain current whereas, in case of low doping concentration, on current is more due to lesser impurity scattering as shown in Figure 5. Drain voltage was kept at 50 mV for measurement of on-off current ratio. On current was studied at gate voltage (V_g) = 1 V and off current was measured at V_g = 0 V.

The variation of on-off current ratio with varying H_{fin} for different doping levels is shown in Figure 6. To maximize this ratio, the doping level should be high (i.e., 10^{18}/cm^3) because off current is also less in case of high channel doping similar to on current and leads to better on/off current ratio.

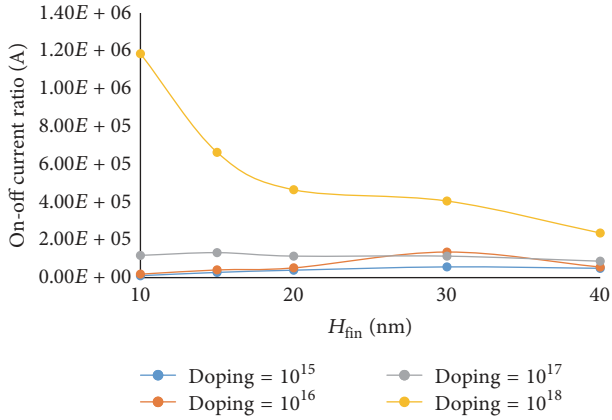


Figure 6: Variation of on-off current ratio with fin height for different doping concentration at 1 nm oxide thickness.

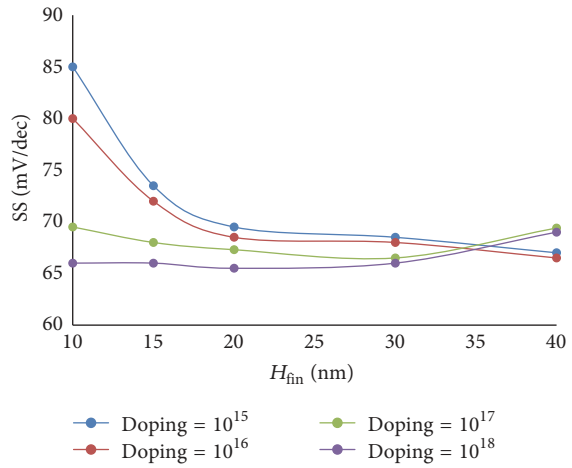


Figure 7: Variation of SS with fin height for different doping concentration at 1 nm oxide thickness.

Change in gate voltage for a decade change in drain current is known as subthreshold swing (SS). It is calculated using (3) keeping drain voltage at 50 mV.

$$\mathrm{SS} = \frac{dV_g}{d\log(I_d)}. \tag{3}$$

For low doping level, SS reduces with H_{fin}. For high doping levels (10^{17}/cm^3 and 10^{18}/cm^3) SS decreases for H_{fin} range of 10 nm to 30 nm and it increases with H_{fin} after 30 nm. Comparison of SS for all the doping levels shows that high doping results in decreased SS as shown in Figure 7.

For DIBL calculations, simulations (at drain voltage 20 mV and 1 V) are performed for each combination of input process parameters. The horizontal displacement of the experimental transfer characteristics for V_d = 20 mV and 1 V at constant drain current is defined as DIBL [13].

Table 2: Variation of W_{eff} and I_{DIBL} with H_{fin}.

SN	H_{fin} (nm)	W_{eff} (nm)	I_{DIBL} (μA)
(1)	10	30.042	0.1502083
(2)	15	40.042	0.2002083
(3)	20	50.042	0.2502083
(4)	30	70.042	0.3502083
(5)	40	90.042	0.4502083

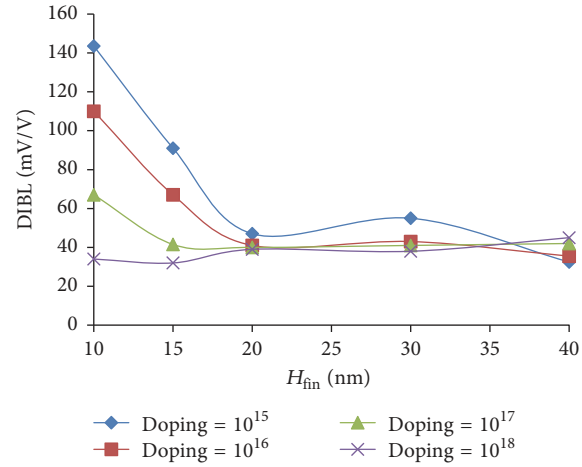


Figure 8: Variation of DIBL with fin height for different doping concentration at 1 nm oxide thickness.

The constant drain current at which the horizontal displacement of transfer characteristics is observed for the calculation of DIBL is given as [13]

$$I_{DIBL} = 10^{-7} \times \left(\frac{W_{eff}}{L}\right) A. \tag{4}$$

W_{eff} is effective channel width and for rectangular FinFET it is defined as

$$W_{eff} = 2H_{fin} + W_{fin}. \tag{5}$$

W_{fin} for rectangular FinFET is constant throughout the fin but for triangular FinFET it varies from $W_{fin.bot}$ to $W_{fin.top}$. In [14], the equivalent fin width for trapezoidal FinFET with $W_{fin,top}$ = 5 nm and $W_{fin,bot}$ = 15 nm is given at its orthocenter. The same idea can be extended to find the equivalent fin width for the triangular FinFET at its orthocenter and can be given as

$$W_{fin} = W_{fin,top} + \frac{\alpha}{1+\alpha}\left(W_{fin,bot} - W_{fin,top}\right), \tag{6}$$

where

$$\alpha = \frac{2W_{fin,bot} + W_{fin,top}}{2W_{fin,top} + W_{fin,bot}}. \tag{7}$$

For the designed triangular device $W_{fin,top}$ = 1 nm, $W_{fin,bot}$ = 15 nm and hence from (7), α = 1.82353. Since H_{fin} is varied from 10 nm to 40 nm, the value of W_{eff} and I_{DIBL} is listed in Table 2.

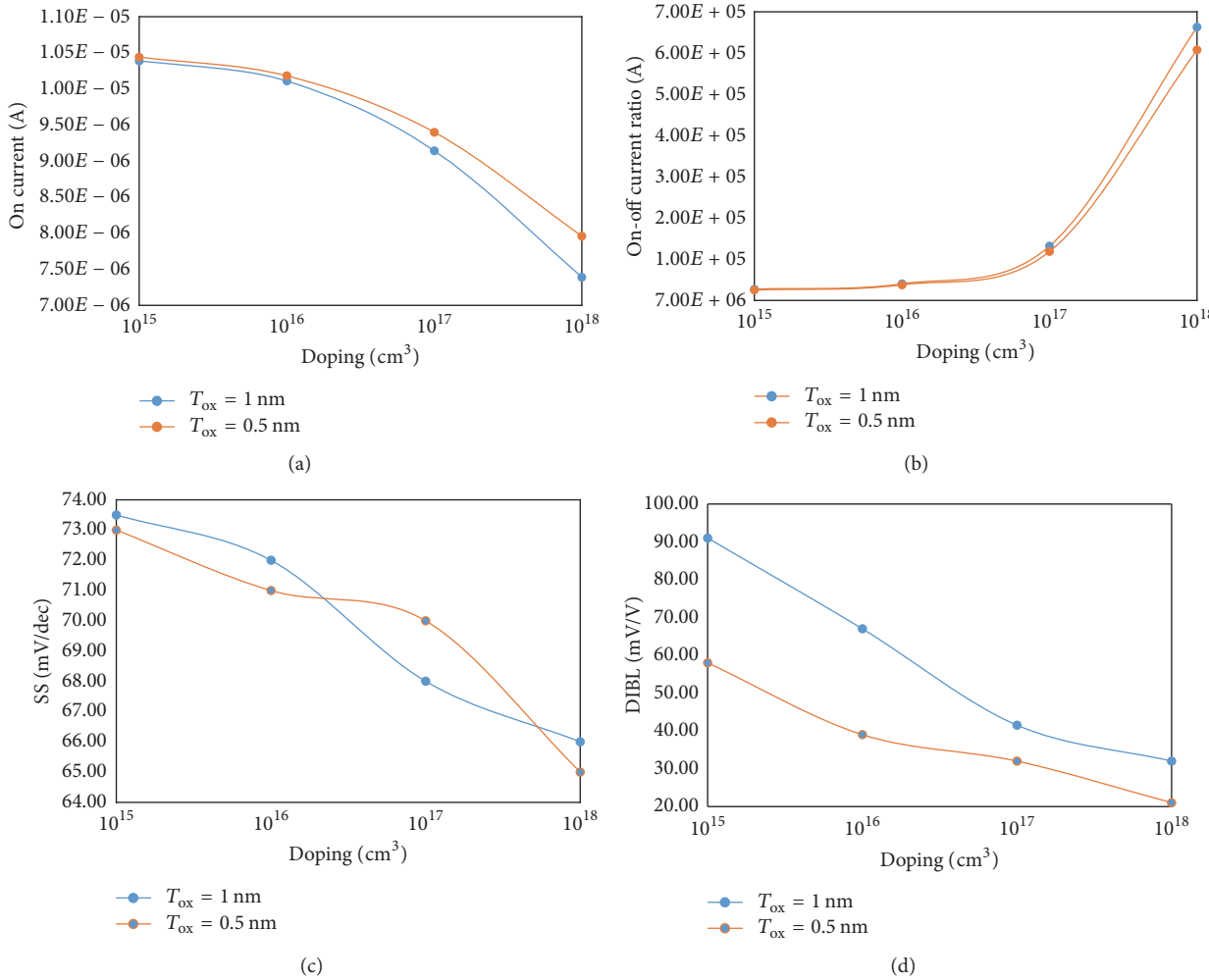


FIGURE 9: Variation of output parameters of FinFET with respect to different doping concentration for T_{ox} = 0.5 nm and 1 nm and H_{fin} = 15 nm. (a) On current. (b) On-off current ratio. (c) SS. (d) DIBL.

DIBL value is improved for high channel doping; this is due to the reason that high doping in the channel lessens the impact of drain potential onto it which further shields channel from drain terminal. In [13], for 25 nm gate length device it is shown that for nonrectangular FinFET device if $W_{fin,top}/W_{fin,bot}$ is less than 0.2 then the range of SS is 74 mV/dec to 76 mV/dec and DIBL is 80 mV/V to 90 mV/V. In this work, simulation results show that, with the gate length reduced to 20 nm, $W_{fin,top}$ = 1 nm, and $W_{fin,bot}$ =15 nm (i.e., $W_{fin,top}/W_{fin,bot}$ = 0.0667), SS can be achieved as low as 65.5 mV/dec and DIBL can be minimized to 32 mV/V as shown in Figures 7 and 8.

On current of device is decreasing with increase in doping concentration; however increasing doping concentration leads to increment in on-off current ratio. SS and DIBL decrease with high doping concentration for 15 nm fin height. Dependence of on current, on-off current ratio, SS, and DIBL on doping concentration for different gate oxide thickness is shown in Figure 9. It is noticed that mobility gets decreased for high doping and thus results in lesser on current and also, leakage current is decreased thus leading to improved on-off current ratio. Better values of SS and DIBL are obtained with doping of $10^{18}/cm^3$ as compared to $10^{15}/cm^3$. Oxide thickness of 0.5 nm shows better result for DIBL. This is because of the fact that gate has strong control over three sides of channel for T_{ox} = 0.5 nm compared to that for T_{ox} = 1 nm which reduces the influence of drain over channel. Thus, threshold voltage is less affected by variations in applied drain voltage and results in lower DIBL. Also, the use of HfO_2 as gate dielectric can scale the oxide thickness down simultaneously without increasing gate tunneling current.

5. Conclusion

Simulation results show that the variation of process parameters of FinFET has considerable impact on performance parameters of the FinFET. Due to reduced top fin width, gate control over channel is improved and it leads to better performance. On-off current ratio sharply decreases with decrease in doping concentration and increase in fin height. On-off current ratio is improved for high doping ($10^{18}/cm^3$) and minimum fin height (10 nm). SS is better for maximum

doping concentration with 20 nm fin height. DIBL is best for maximum doping concentration with 15 nm fin height. For 1 nm gate oxide, DIBL reduces with doping. For 0.5 nm gate oxide the results are better than that of 1 nm gate oxide provided that fin height is less than 15 nm. For fin height more than 15 nm, performance at 1 nm oxide thickness is better.

Conflicts of Interest

The authors declare that there are no conflicts of interest regarding the publication of this paper.

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