Journal of The Electrochemical Society, **154** (5) H374-H379 (2007)
0013-4651/2007/154(5)/H374/6/$20.00 © The Electrochemical Society

Comparative Studies on Double δ-Doped $Al_{0.3}Ga_{0.7}As/In_xGa_{1-x}As/GaAs$ Symmetrically Graded Doped-Channel Field-Effect Transistors

Ching-Sung Lee,[a,z] Chien-Hung Chen,[a] Jun-Chin Huang,[b] and Ke-Hua Su[b]

[a]*Department of Electronic Engineering, Feng Chia University, Taichung, Taiwan 40724*
[b]*Institute of Microelectronics, Department of Electrical Engineering, National Cheng Kung University, Tainan, Taiwan*

This work provides comparative studies of a double δ-doped $Al_{0.3}Ga_{0.7}As/In_xGa_{1-x}As/GaAs$ symmetrically graded ($x = 0.15 \rightarrow 0.2 \rightarrow 0.15$) doped-channel field-effect transistor (DD-DCFET) with respect to a conventional double δ-doped pseudomorphic high electron mobility transistor (pHEMT) and a conventional DCFET structure. All threes samples, grown by the low-pressure metallorganic chemical vapor deposition (LP-MOCVD) system, have identical layer structures except for their different doping schemes. Comprehensive investigations on the static, microwave, and temperature-dependent characteristics have been made. Possessing the advantages of DCFETs and pHEMTs, the proposed DD-DCFET has demonstrated comprehensively superior linearity, current drive, voltage gain, high-frequency characteristics, and thermal stability characteristics. It is promisingly suitable for millimeter-wave integrated circuit applications.
© 2007 The Electrochemical Society. [DOI: 10.1149/1.2711079] All rights reserved.

Manuscript submitted September 7, 2006; revised manuscript received December 29, 2006.
Available electronically March 16, 2007.

Over the past years, various compound semiconductor high-speed devices have been devised to meet the growing demands of millimeter-wave integrated circuit (MMIC) applications.[1,2] The advanced development in the epitaxial systems,[3,4] such as the metallorganic chemical vapor deposition (MOCVD) and the molecular-beam epitaxy (MBE) technologies with precise control of growth specifications, has stimulated prosperous investigations in the high-speed heterostructure field-effect transistor (HFET) designs.[5-8] The doped-channel field-effect transistors (DCFETs), due to their distinguished doped-channel structure design, have demonstrated distinguished linearity characteristics, because electrons in the channel being attracted to their ionized donors are difficult to be depleted by the decreased gate biases. However, the intrinsic ionized impurity scattering[9] in DCFETs degrade the carrier transport properties. The pseudomorphic high electron mobility transistors (pHEMTs) preventing the ionized impurity scattering have demonstrated superior high-gain performances. The double δ-doping techniques have also been employed to enhance the two-dimensional electron gas (2DEG) concentration and current-drive capability. Nevertheless, the linearity issue may need to be improved as compared to the performance of DCFET structures.

By inheriting the distinguished performance from DCFET and pHEMT structures, respectively, this work proposes a double δ-doped $Al_{0.3}Ga_{0.7}As/In_xGa_{1-x}As/GaAs$ symmetrically graded ($x = 0.15 \rightarrow 0.20 \rightarrow 0.15$) DCFET to provide comprehensively superior high-gain, high-power, and high-linearity performances. Devising a symmetrically graded InGaAs channel can effectively increase the discontinuity barrier height within the channel/buffer heterostructure to further improve its channel confinement capability. Comparative studies of various device characteristics have been made with respect to a δ-doped pHEMT and a DCFET, correspondingly, in the present work.

Material Growth and Device Fabrication

The studied structures were grown by the LP-MOCVD deposition system on the semi-insulating (SI) GaAs substrates. Table I lists the compared DCFET (sample A), δ-doped pHEMT (sample B), and the proposed DD-DCFET (sample C) structures, respectively. Upon the SI GaAs substrate, the proposed sample C structure consists of, sequentially, a 1000 Å thick GaAs buffer, a 1500 Å thick $Al_{0.3}Ga_{0.7}As$ buffer, an inverted δ-doping layer ($n^+ = 5 \times 10^{11}$ cm^{-2}), a 50 Å thick $Al_{0.3}Ga_{0.7}As$ inverted spacer, a 150 Å thick n^+-$In_xGa_{1-x}As$ symmetrically graded ($x = 0.15 \rightarrow 0.20 \rightarrow 0.15$) doped-channel layer ($n^+ = 1 \times 10^{18}$ cm^{-3}), a 50 Å thick $Al_{0.3}Ga_{0.7}As$ upper spacer, an upper δ-doping layer ($n^+ = 2.5 \times 10^{12}$ cm^{-2}), a 400 Å thick $Al_{0.3}Ga_{0.7}As$ Schottky layer, and finally a 600 Å thick n^+-GaAs cap layer ($n^+ = 1 \times 10^{19}$ cm^{-3}), respectively. In comparison, sample A has a doped channel ($n^+ = 4 \times 10^{18}$ cm^{-3}), yet without the δ-doping and spacer layers, whereas sample B has a undoped channel with both upper and inverted δ-doping concentrations of 3 and 1×10^{12} cm^{-2}, respectively. Except for the above different doping schemes, all the studied devices have identical layer structures. The Al compositions of the AlGaAs compounds of the present devices were set to be 0.3 to effectively increase their conduction-band discontinuities without suffering the deep level (DX) centers effects.[10,11] Standard photolithography, lift-off, and rapid thermal annealing (RTA) techniques were employed for the device fabrication. AuGeNi alloy was deposited as the source/drain ohmic contacts, onto which Au was evaporated to reduce the contact resistance. Pt/Au were deposited on the undoped AlGaAs Schottky layer as the gate electrode. The gate dimensions were 1.2×100 μm^2 for all devices. Mesa etching was performed down to the buffer layer to reduce the substrate leakages. Chemical solutions of $H_3PO_4/H_2O_2/H_2O$ were used to wet-etch the GaAs capper.

Results and Discussion

Hall measurements have been conducted to characterize the studied devices at 300 and 77 K under a magnetic field of 5000 G, after removing the cap layers. The corresponding measured 2DEG concentrations, mobility, and mobility-concentration products for samples A, B, and C have been listed in Table II. Unlike the doped-channel structures of samples A and C, sample B has an undoped psudomorphic channel. Therefore, the 2DEG in sample B can significantly prevent the ionized scattering effects to demonstrate the highest transport mobility of 4675 (21757) cm^2 V s at 300 (77) K. The proposed DD-DCFET, sample C, having a slightly lower doped channel than sample A, also shows a higher mobility of 3850 (18000) cm^2/V s than 2804 (14380) cm^2/V s of sample A at 300 (77) K, respectively. In order to provide a fair comparison, the doping schemes for all three devices have been devised to provide a similar 2DEG concentration, as shown in Table II. Sample C has employed the dual δ-doping layers to compensate for the 2DEG concentration loss, decreasing its channel doping more than sample A. Besides, all three samples have the same symmetrically graded InGaAs channel design. Thus, most of the 2DEG population can be

[z] E-mail: cslee@fcu.edu.tw

Downloaded 22 Sep 2009 to 140.116.208.56. Redistribution subject to ECS license or copyright; see http://www.ecsdl.org/terms_use.jsp

Table I. Layer structures of the studied devices denoted by samples A, B, and C, respectively.

Layer structures	Sample A DCFET	Sample B pHEMT	Sample C DD-DCFET
Drain/source contact layer		n^+-GaAs 600 Å ($n^+ = 1 \times 10^{19}$ cm^{-3})	
Schottky contact layer		i-$Al_{0.3}Ga_{0.7}As$ 400 Å	
Upper δ-doping	nil	$n^+ = 3 \times 10^{12}$ cm^{-2}	$n^+ = 2.5 \times 10^{12}$ cm^{-2}
Upper spacer	nil	i-$Al_{0.3}Ga_{0.7}As$ 50 Å	
Symmetrically graded		i-$In_xGa_{1-x}As$ 150 Å ($x = 0.15 \rightarrow 0.20 \rightarrow 0.15$)	
V-shaped channel	$n^+ = 4 \times 10^{18}$ cm^{-3}	undoped	$n^+ = 1 \times 10^{18}$ cm^{-3}
Inverted spacer	nil	i-$Al_{0.3}Ga_{0.7}As$ 50 Å	
Inverted δ-doping	nil	$n^+ = 1 \times 10^{12}$ cm^{-2}	$n^+ = 5 \times 10^{11}$ cm^{-2}
Buffer		i-$Al_{0.3}Ga_{0.7}As$ 1500 Å	
Buffer		i-GaAs 1000 Å	
Substrate		SI GaAs	

confined in the central part of the V-shaped channel with the lowest In composition to further improve its transport velocity. Consequently, samples B and C have exhibited similar mobility-concentration products of 1.44 and 1.31×10^{16} V^{-1} s^{-1}, respectively, at 300 K, and both are higher than 1.1×10^{16} V^{-1} s^{-1} of sample A. The above comparisons indicate that samples B and C demonstrate more improved current drive capability than sample A.

The device dc current-voltage characteristics were characterized using a Keithley 4200 analyzer. The common-source current-voltage characteristics for samples A, B, and C at 300 K are shown in Fig. 1a-c, respectively. Figure 2 shows the extrinsic transconductance (g_m) and the saturation drain current density (I_{DS}) as a function of the gate-to-source voltage for samples A, B, and C at 300 K with $V_{DS} = 3$ V, respectively. Both samples B and C have shown higher drain-source saturation current densities (I_{DSS}), defined at $V_{GS} = 0$ V, of 193.6 and 167.9 mA/mm and maximum saturation drain current densities ($I_{DS,max}$) of 363 and 360 mA/mm than those of sample A ($I_{DSS}/I_{DS,max}$ = 99.9/342 mA/mm). These verify the comparisons in 2DEG concentration-mobility products characterized by the Hall measurement. Similarly, samples B and C have shown higher maximum extrinsic transconductance ($g_{m,max}$) of 182 and 164 mS/mm than 140 mS/mm of sample A. This is mainly due to the reduced impurity scattering phenomena by the undoped channel of sample B and the decreased channel doping in sample C, as compared to the heavily-doped channel structure of sample A. Nevertheless, we define the gate-voltage swing (GVS) as the available gate bias range where the transconductance plateau is no less than 90% of the $g_{m,max}$ value. Samples A and C have shown improved GVS linearity of 1.25 and 1.07 V than 0.75 V of sample B. The corresponding available I_{DS} ranges for samples A, B, and C were determined to be 175, 152, and 170 mA/mm, respectively, as shown in Fig. 3. The improved GVS linearity property of samples A and C is attributed to their doped-channel structures. Alhough the attractive forces between the channel impurities and the 2DEG would degrade the electron-transport property, they could retard the 2DEG depletion by the decreased gate bias, thus leading to the improved GVS linearity. Consequently, in contrast to only partially good device characteristics of samples A and B, respectively, the compromised design by employing the decreased channel doping and the double δ-doped structure in sample C has demonstrated comprehensively superior performances with regard to the device gain, current drive, and GVS linearity at the same time.

Table II. Corresponding 2DEG carrier concentrations and mobility of samples A, B, and C at 300 (77) K, respectively.

Hall characteristics	Sample A	Sample B	Sample C
Electron mobility (cm^2/V s) at 300 (77) K	2804 (14380)	4675 (21757)	3850 (18000)
2DEG concentrations ($\times 10^{12}$ cm^{-2}) at 300 (77) K	3.91 (3.67)	3.1 (2.55)	3.41 (3.01)
Mobility-concentration product ($\times 10^{16}$ 1/V s) at 300 (77) K	1.10 (5.27)	1.44 (5.55)	1.31 (5.42)

Figure 4 and its inset show the two-terminal gate-drain breakdown and forward turn-on characteristics at 300 K for samples A, B, and C, respectively. Higher turn-on voltage, being able to allow a larger induced current in the channel, together with lower breakdown voltage can provide a broader bias regime, thus advantageous to the output power performance. The two-terminal gate-drain breakdown voltage (BV_{GD}) and forward turn-on voltage (V_{on}) are defined to be the gate-drain voltages at which the magnitudes of gate current densities are 1 mA/mm. The BV_{GD} (V_{on}) values for samples A, B, and C are −27.9 (1.2), −22 (0.95), and −24.3 (1.0) V, respectively. Though samples A and C show similar reverse breakdown curves in the small voltage regime, they significantly deviate close to the defined $I_G = 1$ mA/mm level. This is attributed to the fact that the δ-doped quantum wells (QWs) in the Schottky contact layer enhance the tunneling mechanism, because the gate-leakage currents mainly consist of two major contributions: (*i*) the electron injection through thermionic-field emission over the Schottky gate barrier and (*ii*) the tunneling current through the Schottky gate barrier at high electric field. Therefore, sample A without the upper δ-doping structure can greatly prevent the tunneling leakages through the Schottky gate barrier at high electric field and has resultantly shown more improved BV_{GD} (V_{on}) characteristics than samples B and C.

The characteristics of extrinsic transconductance, output conductance, and voltage gain at 300 K with respect to the drain-source voltage for samples A, B, and C have been shown in Fig. 5, respectively. Because lower In composition of the $In_xGa_{1-x}As$ compound can suffer less from the high-field kink effects, the In compositions of the symmetrically graded ($x = 0.15 \rightarrow 0.2 \rightarrow 0.15$) $In_xGa_{1-x}As$ channel of the studied devices were designed to linearly decrease from the central part of the InGaAs channel towards the buffer side. The kink effects, the substrate leakage current, and the output conductance can then be effectively reduced. Consequently, samples A, B, and C have all demonstrated low output conductance (g_d) values of 0.76, 1.12, and 0.9 mS/mm at $V_{DS} = 4$ V, respectively. Lower g_d values of samples A and C than sample B are possibly attributed to the impurity scattering effects in the doped channel. Similar to the discussions on the transport property in the previous section, the attractive forces resulted from the channel impurities would slow down the 2DEG transport. Thus, electrons in the doped channel are more difficult to initiate the effective impact ionizations. The kink-effects phenomena in samples A and C are more alleviated than in sample B. Moreover, higher channel doping in sample A has resulted in a lower g_d value than that of sample C. Consequently, with the voltage gain defined to be g_m/g_d, both samples A and C have shown higher device gains of 181 and 176 than 159 of sample B at $V_{DS} = 4$ V. In comparison to the dc characteristics, the present

Downloaded 22 Sep 2009 to 140.116.208.56. Redistribution subject to ECS license or copyright; see http://www.ecsdl.org/terms_use.jsp

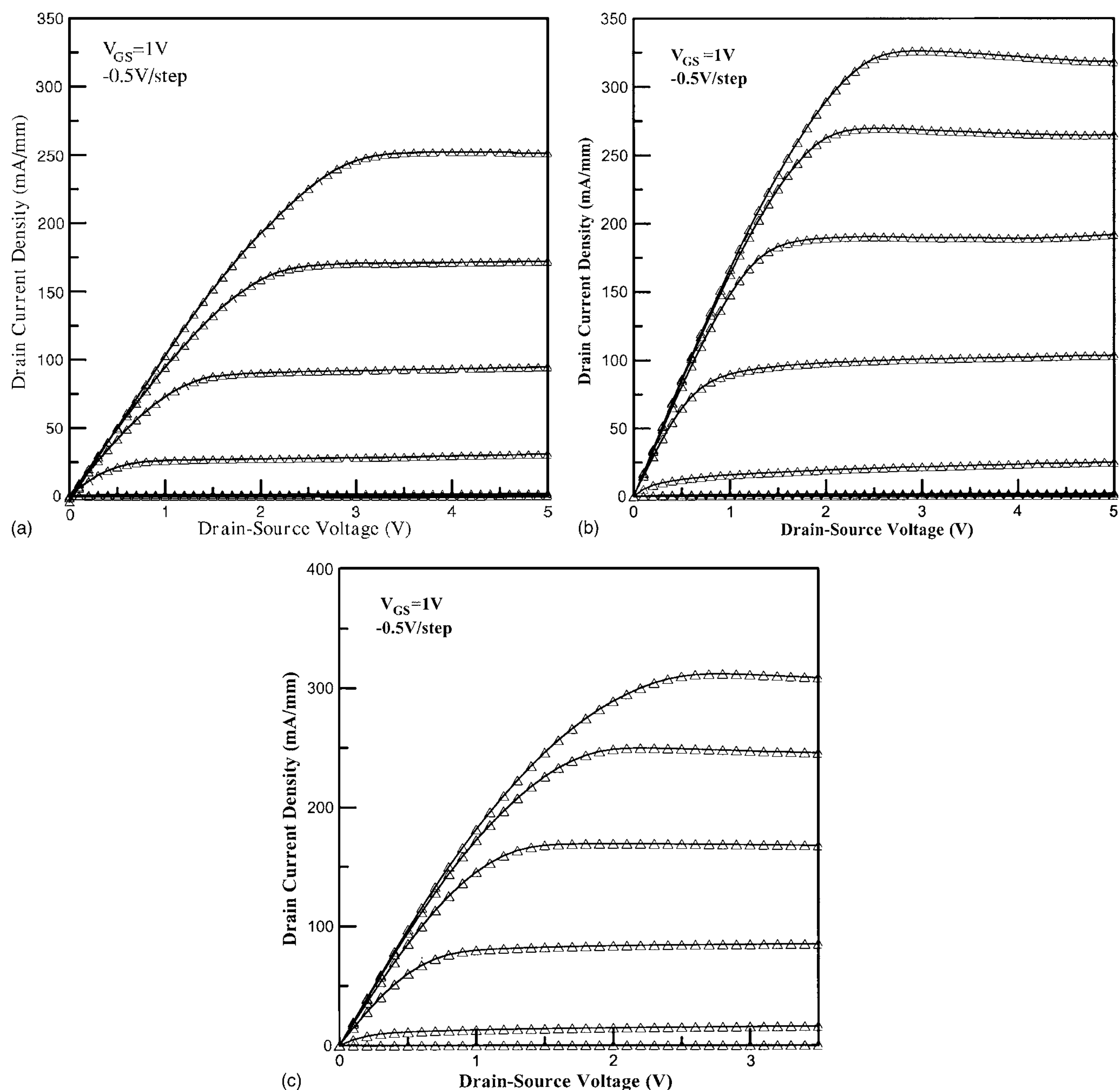

Figure 1. Common-source current-voltage characteristics for (a) sample A, (b) sample B, and (c) sample C, respectively, at 300 K.

sample C of DD-DCFET is comprehensively superior to one of our previous works[12] with $A_v = 132$, $g_d = 2.24$ mS/mm, $BV_{GD} = -15.9$ V, and GVS = 0.8 V at 300 K.

Figure 6 shows the output power (P_{out}), power gain (G_s), and the power-added efficiency (PAE) characteristics at 300 K, measured at 2.4 GHz using an on-wafer load-pull system. The devices are operated at class-AB condition and compromised by the power-added efficiency and the output power. The characterized power performances with their respective gate-bias conditions for all three samples are listed in Table III. The product of high device gain and enhanced current drive capability directly result in the improved power performance, and the extended bias range formed by BV_{GD} and V_{on} is further beneficial to the power applications, as discussed before. Though sample B has the highest $g_{m,max}$ value as compared to samples A and C, its limited linearity and breakdown properties degrade the power characteristics.[7] Consequently, samples A and C have shown comparably superior power characteristics, including P_{out} of 13.29 (213.3)/12.75 (188.4) dBm (mW/mm), G_s of 17.11/17.05 dB, and PAE of 49.03/48.84%, as compared to those of sample B and the insulated-gate FET.[13] The noise characteristics with their respective gate-bias conditions for samples A, B, and C are also listed in Table III, respectively. It was characterized over a frequency range of 1.2 to 7.2 GHz at 300 K using an HP8970B noise figure meter. Although higher drain current leads to more noisy characteristics, decreasing the current from its $g_{m,max}$ peak degrades the device gain, as shown in Fig. 2, and exaggerates the noise figures by the following equation[14]

$$NF_{min} \approx 1 + \omega \frac{C_{gs}}{g_m} \sqrt{\frac{R_s + R_g}{R_i}} \qquad [1]$$

where NF_{min} denotes the minimum noise figure, ω is the operation frequency, C_{gs} is the gate-to-source capacitance, R_s/R_g are the parasitic source/gate resistance, and R_i is the equivalent input resistance,

Downloaded 22 Sep 2009 to 140.116.208.56. Redistribution subject to ECS license or copyright; see http://www.ecsdl.org/terms_use.jsp

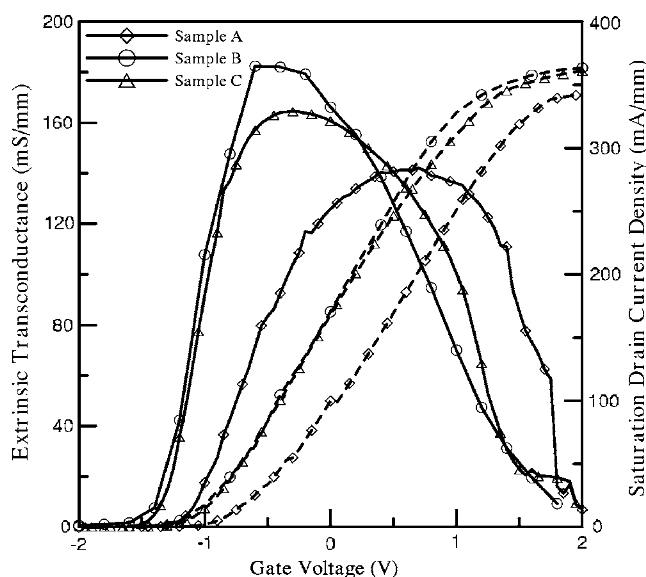

Figure 2. Extrinsic transconductance and saturation drain current density characteristics vs gate voltage at 300 K for samples A, B, and C, respectively.

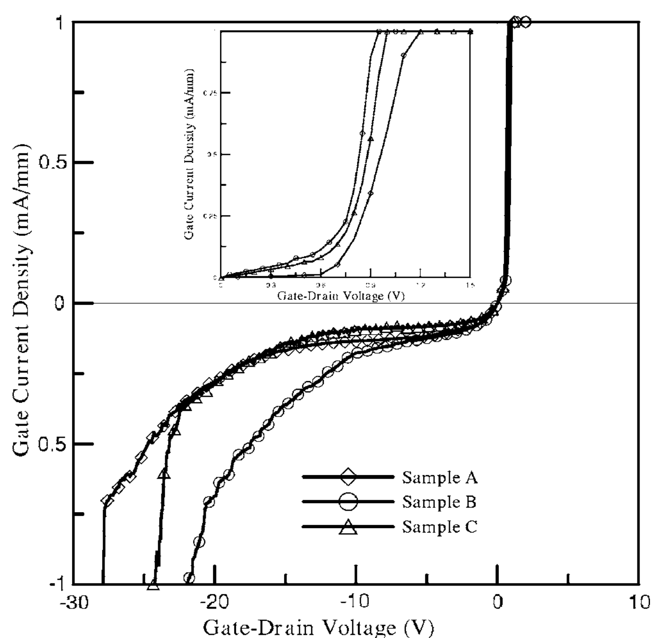

Figure 4. Two-terminal gate-drain breakdown characteristics at 300 K for samples A, B, and C, respectively. (Inset) Zoomed-in forward characteristics.

respectively. Therefore, optimum bias conditions were obtained in Table III to achieve the minimum noise figure performance with a similar current level for the studied devices, as can be found in Fig. 2. Consequently, sample B has demonstrated the lowest minimum noise figure of 1.2 dB and highest associated gain of 18.74 dB as compared to samples A and C, respectively, at the same I_{DS} level. Sample B is more suitable for low-noise circuit applications, whereas sample A is suitable for high-power implementations. Besides, sample C, possessing the compromised design between the DCFET (sample A) and the pHEMT (sample B) structures, can be promisingly applied to high voltage-gain, high power, and high linearity MMIC technologies.

The temperature-dependent g_m and I_{DSS} characteristics, from 300 to 450 K, vs the gate voltage for sample C have further been indicated in Fig. 7 to investigate its thermal stability. Both g_m and I_{DSS} were observed to decrease with temperature. The decrease of I_{DSS} was due to the enhanced carrier-carrier scattering effects at high temperatures, because the increased thermal energies of carriers enhance the carrier-carrier collisions and degrade the transport property. The decrease of g_m was due to the decreased current densities and the degraded substrate/gate leakages at high temperatures. As discussed before, samples B and C have shown comparably higher $g_{m,\max}$ and $I_{DS,\max}$ values than sample A at room temperature, due to their improved transport properties. As shown in Fig. 8, sample C (A) has shown more stable variations of 25.6 (22)/31.4 (23)% in $g_{m,\max}/I_{DS,\max}$, respectively, as the ambient temperature is increased from 300 to 450 K, which are superior to the 31.6/34% in $g_{m,\max}/I_{DS,\max}$ of sample B. The following are possible reasons to

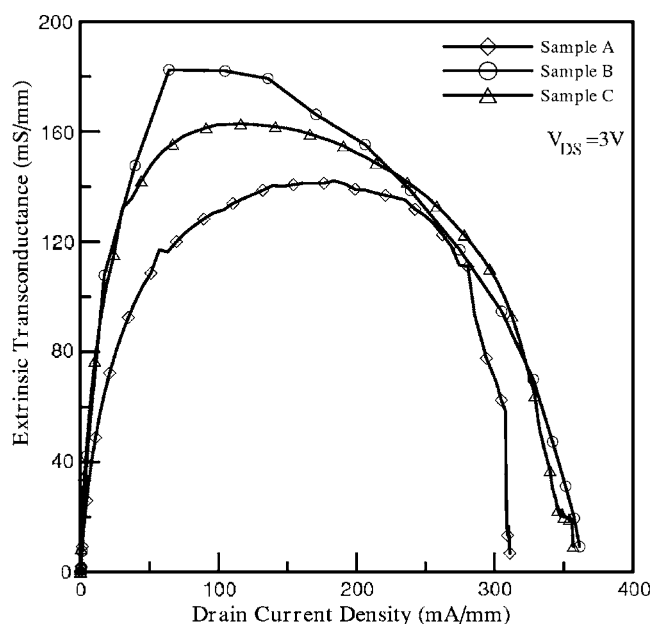

Figure 3. Extrinsic transconductance as a function of the drain current density at 300 K for samples A, B, and C, respectively.

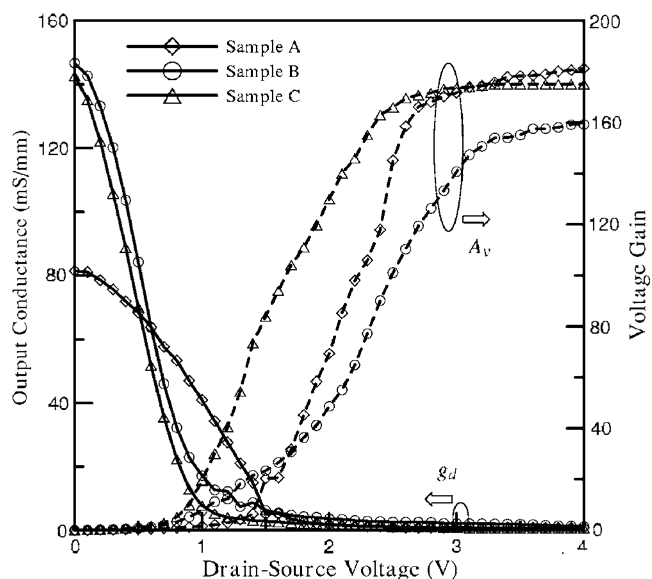

Figure 5. Output conductance and voltage characteristics vs drain-source voltage at 300 K for samples A, B, and C, respectively.

Downloaded 22 Sep 2009 to 140.116.208.56. Redistribution subject to ECS license or copyright; see http://www.ecsdl.org/terms_use.jsp

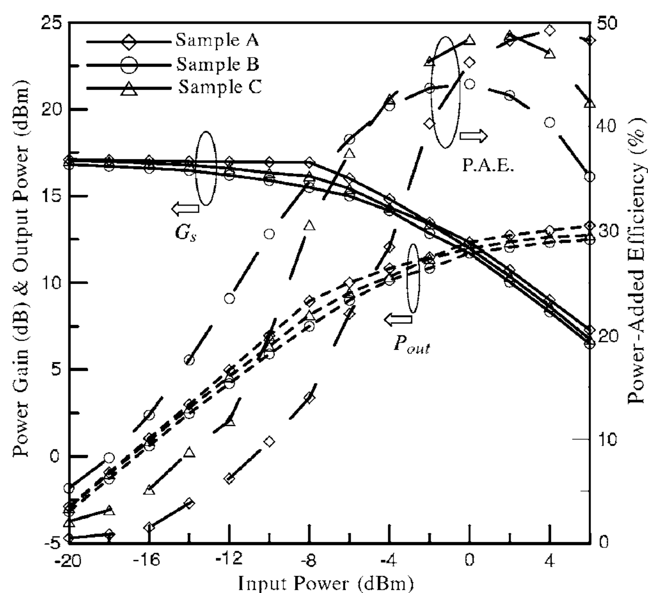

Figure 6. Output power, power gain, and power-added efficiency characteristics vs input power for samples A, B, and C, respectively.

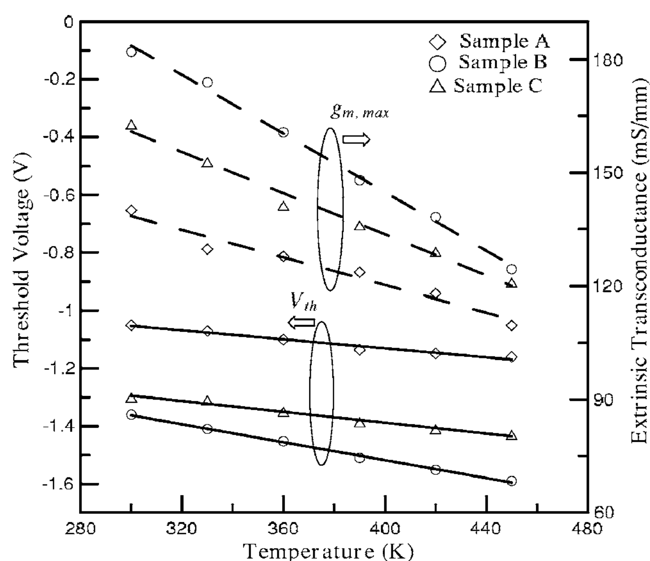

Figure 8. Temperature-dependent V_{th} and $g_{m,max}$ characteristics for samples A, B, and C, respectively.

account for this observation. Because sample B with an undoped InGaAs channel is much more dominated by the lattice scattering at high temperatures than the doped-channel structure of sample C, its carrier transport property is more likely degraded by the increased thermal vibrations of lattice atoms, as compared to that in sample C. The thermally generated carriers enhance the screening effects to reduce the impurity scattering mechanism in the doped-channel devices. Therefore, the doped-channel structure can suffer less than the thermal variations as observed in samples A and C, respectively. The threshold voltage (V_{th}) was determined from the intercept of the gate-voltage axis of the extrapolated line of the I_{DSS} slope in Fig. 7. The temperature dependences of V_{th} for samples A–C have also been shown in Fig. 8. The threshold voltage shifts (ΔV_{th}) from 300 to 450 K were determined to be −0.11, −0.23, and −0.13 V, and the thermal threshold coefficients ($\partial V_{th}/\partial T$) were −0.73, −1.53, and −0.86 mV/K for samples A, B, and C, respectively. Similar to the observed g_m characteristics, sample C has demonstrated comparably good thermal threshold characteristics as sample A, yet has shown lower threshold magnitude and much improved thermal threshold stability than sample B. In addition, samples A and C have shown superior thermal threshold stability as compared to other reports.[15,16]

The microwave characteristics of the studied devices were characterized using a HP 8510B vector network analyzer in conjunction with the cascaded probes over the frequency range of 0.2–20 GHz. The gate dimensions are $1.2 \times 200\ \mu m^2$ with the drain-to-source spacing of 7 μm for all three devices. Due to the distinguished g_m performances, both samples B and C have shown a higher cutoff frequency (f_T) of 20.5 and 18.1 GHz and the maximum oscillation frequency (f_{max}) of 43 and 34.5 GHz than those of sample A (f_T/f_{max} = 13.3/30 GHz) at 300 K. The high-frequency characteristics of sample C at 300, 360, and 420 K have also been shown in Fig. 9, respectively. Figure 10 draws the extracted temperature dependences of f_T and f_{max} for samples A, B, and C, respectively. Both f_T and f_{max} decrease monotonously with temperature, which are similar to the decreased g_m characteristics. The thermal coefficients for $f_T(f_{max})$, defined as $\partial f_T/\partial T$ ($\partial f_{max}/\partial T$), were calculated to be −4.17 (−22.5), −18.4 (−75), and −8.33 (−37.5) Hz/K for samples A, B, and C, respectively. Consequently, sample C has shown comparably good high-frequency performance with much improved thermal stability as compared to sample B.

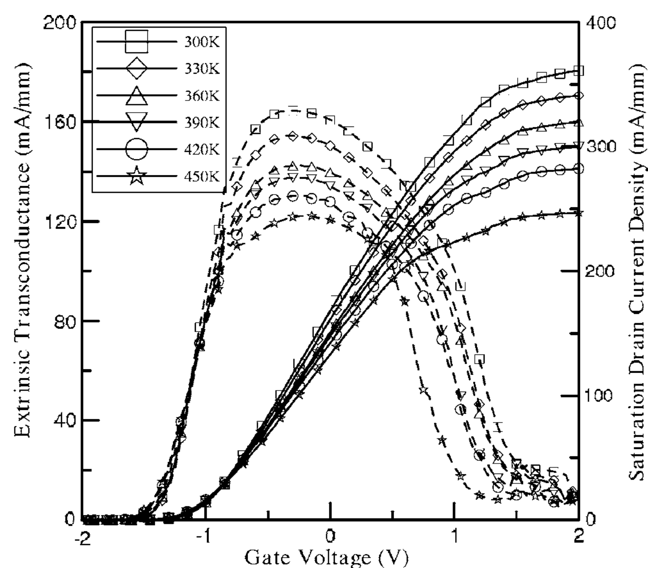

Figure 7. Temperature-dependent g_m and I_{DSS} characteristics vs V_{GS} for sample C from 300 to 450 K, respectively.

Table III. Power and noise characteristics for samples A, B, and C, respectively.

Power and noise characteristics	Sample A	Sample B	Sample C
Gate bias (V)	−0.2	−0.5	−0.4
Output power (dBm, mW/mm)	13.29, 213.3	12.49, 177.4	12.75, 188.4
Power gain (dB)	17.11	16.82	17.05
PAE (%)	49.03	44.1	48.84
Gate bias (V)	−0.2	−0.5	−0.45
NF_{min} (dB)	1.35	1.2	1.24
Associated gain (dB)	13.75	18.74	15.62

Downloaded 22 Sep 2009 to 140.116.208.56. Redistribution subject to ECS license or copyright; see http://www.ecsdl.org/terms_use.jsp

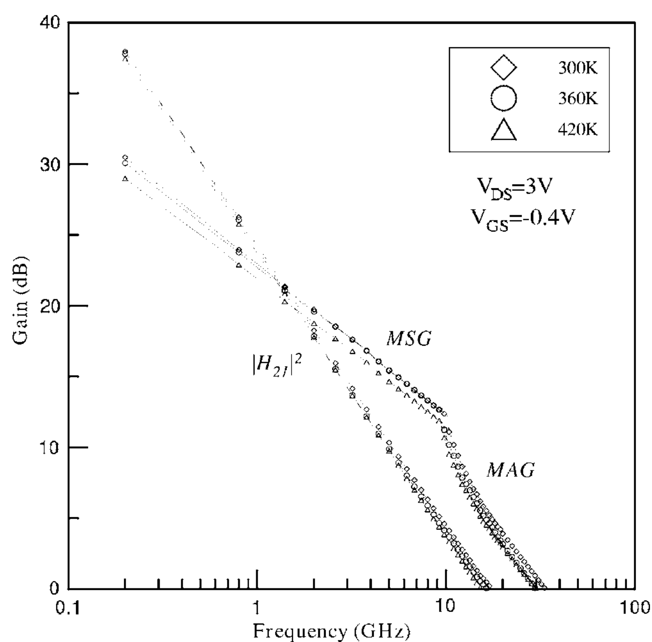

Figure 9. Temperature-dependent high-frequency characteristics for sample C from 300 to 420 K, respectively.

Conclusion

In summary, comprehensive device characterizations of the present double δ-doped $Al_{0.3}Ga_{0.7}As/In_xGa_{1-x}As/GaAs$ symmetrically-graded $(x = 0.15 \rightarrow 0.2 \rightarrow 0.15)$ DD-DCFET (sample C) have been investigated and compared with those of the symmetrically graded DCFET (sample A) and pHEMT (sample B). The respective influences of the device design on the various device characteristics have been physically discussed. In contrast to only partial good device characteristics of samples A and B, respectively, the present DD-DCFET of sample C has demonstrated superiorly high $g_{m,\max}$ of 164 mS/mm, high $I_{D,\max}$ of 360 mS/mm, wide GVS linearity of 1.07 V, improved BV_{GD} (V_{on}) of −24.3 (1.0) V, low g_d of 0.9 mS/mm, high A_v of 176, high f_T ($f_{\max}$) of 18.1 (34.5) GHz, high P_{out} (G_s) of 12.75 dBm (17.0.5 dB) with PAE of 48.84%, and low $NF_{\min}$ of 1.24 dB. Possessing the advantages of DCFETs and pHEMTs, the proposed DD-DCFET has also exhibited improved thermal stability, indicating its promising applications in MMIC technologies.

Acknowledgments

The authors thank Professor Wei-Chou Hsu for his helpful discussions. This work was also supported by the National Science

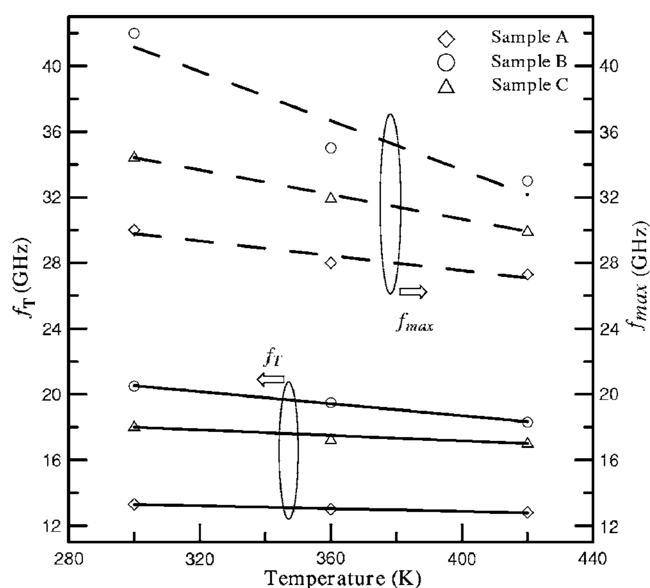

Figure 10. Temperature-dependent f_T and $f_{\max}$ characteristics for samples A, B, and C, respectively.

Council of the Republic of China under contract no. NSC 94-2215-E-035-012.

Feng-Chia University assisted in meeting the publication costs of this article.

References

1. T. Saito, N. Hidaka, and K. Ono, *IEEE GaAs IC Symposium*, Vol. 95, p. 222 (1995).
2. C. K. Chu, H. K. Huang, H. Z. Liu, R. J. Chiu, C. H. Lin, and C. C. Wang, *IEEE Microw. Wirel. Compon. Lett.*, **15**, 667 (2005).
3. S. C. Warnick and M. A. Dahleh, *IEEE Trans. Control Syst. Technol.*, **6**, 62 (1998).
4. J. L. Gentner, P. Jarry, and L. Goldstein, *IEEE J. Sel. Top. Quantum Electron.*, **3**, 845 (1997).
5. C. S. Lee, Y. J. Chen, W. C. Hsu, K. H. Su, J. C. Huang, D. H. Huang, and C. L. Wu, *Appl. Phys. Lett.*, **88**, 223506 (2006).
6. J. C. Huang, W. C. Hsu, C. S. Lee, Y. J. Chen, and D. H. Huang, *Semicond. Sci. Technol.*, **21**, 619 (2006).
7. W. C. Hsu, Y. J. Chen, C. S. Lee, T. B. Wang, J. C. Huang, D. H. Huang, K. H. Su, Y. S. Lin, and C. L. Wu, *IEEE Trans. Electron Devices*, **52**, 1079 (2005).
8. C. S. Lee and W. C. Hsu, *Appl. Phys. Lett.*, **84**, 3618 (2004).
9. Y. Betser and D. Ritter, *IEEE Trans. Electron Devices*, **43**, 1187 (1996).
10. J. V. Thordson, J. J. Harris, and M. R. Fahy, *Solid-State Electron.*, **43**, 141 (1999).
11. K. W. Kim, H. Tian, and M. A. Littlejohn, *IEEE Trans. Electron Devices*, **38**, 1737 (1991).
12. D. H. Huang, W. C. Hsu, Y. S. Lin, J. C. Huang, and C. L. Wu, *J. Electrochem. Soc.*, **153**, G826 (2006).
13. S. S. Lu, Y. W. Hsu, C. C. Meng, and L. P. Chen, *IEEE Electron Device Lett.*, **20**, 21 (1999).
14. P. H. Ladbrooke, *MMIC Design GaAs FETs and HEMTs*, p. 160, Artech House, Boston (1991).
15. S. J. Yu, W. C. Hsu, Y. J. Li, and Y. J. Chen, *Jpn. J. Appl. Phys., Part 1*, **43**, 5942 (2004).
16. Y. J. Li, W. C. Hsu, and S. Y. Wang, *J. Vac. Sci. Technol. B*, **21**, 760 (2003).

Downloaded 22 Sep 2009 to 140.116.208.56. Redistribution subject to ECS license or copyright; see http://www.ecsdl.org/terms_use.jsp