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Comparative Study of a Three Phase Cascaded H-Bridge Multilevel Inverter for Harmonic Reduction

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Abstract

The aim of this research project is to analyze and design of energy storages in electrical distribution system. In this paper presents a comparative study between sinusoidal pulse width modulation (SPWM) and space vector pulse width modulation (SVPWM) technique, based on generate signal five level of cascaded H-bridge for reduction harmonics in the multilevel inverter output. A multilevel inverter is a preferred choice for most medium-voltage and high-power applications, as well as cascaded H-bridge (CHB) five-level inverters due to its advantages such as low cost, light weight and compact size. It is suitable particularly for use in a cascaded H-bridge multilevel inverter due to reduced total harmonic distortion (THD). Harmonic content in three phase multilevel inverter can be investigated by generating (SPWM) and (SVPWM) algorithm signal based on a five-level (CHB). The proposed system is designed using MATLAB/SIMULINK consists of cascaded H-bridge (CHB) multilevel inverter.

Keywords: *Cascaded H-bridge (CHB), SVPWM, SPWM, total harmonic distortion (THD).*

1. Introduction

The development of power electronics and increased powers involved and the flexibility of the use of semiconductors has electricians encouraged to undertake significant associations of static converters power to electric machines A multilevel inverter is a preferred choice for most medium-voltage and high-power applications, as well as cascaded H-bridge (CHB) two-level inverters due to its advantages such as lower common-mode voltage, lower dv/dt, reduced total harmonic distortion (THD) in output voltage current and reduced voltage on power switching for a general circuit of 5-level cascaded H-bridge inverter [1]. Converting a static structure that comprises mainly applications of power electronic is becoming increasingly important for power of the topology. It has to adapt to the growth of the power to convert a multilevel inverter, for example three topology cascaded H-bridge (CHB), diode clamped (NPC) and flying Capacitor (FC) [2] Cells with separated DC sources shown in Figure1.

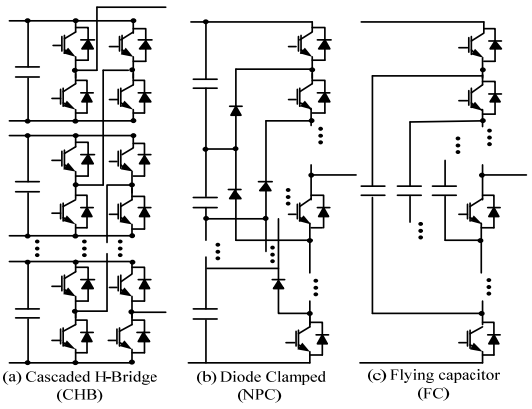

Figure 1. Topologies of Multilevel Inverter, (a) Cascaded H-Bridge (CHB), (b) Diode Clamped (NPC), (c) Flying Capacitor (FC)

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Our job is to the Implementation of technical SPWM which is to minimize the rate harmonics (THD) of the output wave [3]. The performance of the inverter, for any what control strategy related to content harmonics of its output voltage. A lot of techniques have been studied to reduce harmonics. Pulse width modulation (PWM) technique gives the effect on the switching losses inverter, harmonic contents in the output waveform, and overall performance of the inverter [4, 5]. Sinusoidal PWM (SPWM) is an effective method to reduce lower order harmonics while varying the output voltage In contrast, Phase Disposition (PD) modulation of a CHB is harmonically high quality due to direct harmonic energy altogether with carrier harmonic. In case of the three-phase inverter, the ratio of the fundamental component of the utmost line-to-line voltage to the direct supply voltage is 86.6% [6]. Space vector pulse width modulation algorithm (SVPWM) is a more attractive candidate and its advantage is the six sector voltage $(V_1 - V_6)$ that operates starting from each switching vector as a point in complex (α, β) space and consists of six sectors, with each having an angle of 60 degree as shown in Figure 2 [7, 8].

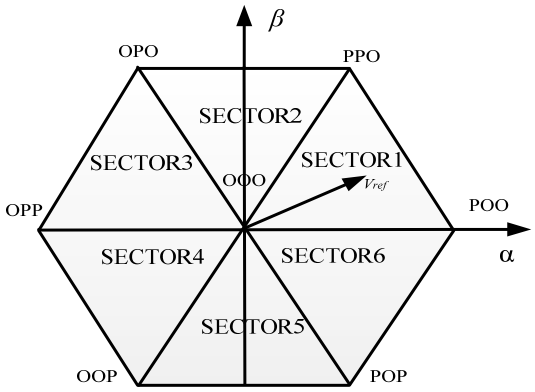

Figure 2. Space vector diagram for a two-level inverter

Each sector consists of $(n-1)^2$ triangle. SVPWM diagram of an n-level inverter consists of 125 five-level, [9]. In this paper presents a comparative study between sinusoidal pulse width modulation (SPWM) and space vector pulse width modulation (SVPWM) technique, based on generate signal five level of cascaded H-bridge for reduction harmonics in the multilevel inverter output. The aim of this study is to implement the carrier frequency parameter with modulation index for achieving the low harmonic distortion. Harmonic content in three phase multilevel inverter can be investigated by generating (SPWM) and (SVPWM) algorithm signal based on a five-level (CHB). The proposed system is designed using MATLAB/SIMULINK consists of cascaded H-bridge (CHB) multilevel inverter.

2. Multilevel Inverter

The Concepts of multilevel inverters (MLI) depends not only on two voltage levels to create the AC signal. Instead, it is added to most levels of voltage to the other to create a form of reinforced smooth wave, with a low dv/dt and less harmonic distortion [10]. With more in the inverter voltage levels it creates a smoother waveform becomes, but with many levels of design becomes more complex, with more components and must be more complex controller for inverter [11]. The multilevel inverters diagrams Figure 3. Illustrates of the inverters have been 2-level inverter, 3-level inverter, and the N-level inverter. All the capacitors include to a voltage of Vdc.

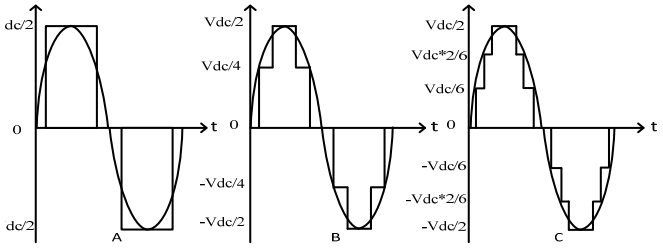

Figure 3. Output Voltage of (a) 2 Levels Inverter (b) 3 Levels Inverter (c) 5 levels Inverters [12]

3. Pulse Width Modulation (PWM) Techniques

In the early 1970s, the majority of PWM inverters using techniques based on the sampling method. Sinusoidal pulse width modulation of the primitive techniques, which are used to suppress the harmonics, present in a quasi-square wave. Over the years, he has developed technical PWM where the objectives were to improve performance, simplify PWM strategies and applications of microprocessors later, to produce a reduction of harmonic distortion and reduce switching losses [7]. Has been extended to several principles support levels based PWM technology as a means of controlling the active devices in a multilevel converter. PWM three techniques commonly used are- the sinusoidal PWM technology [8].

1) High-qualify utilization of a DC power supply that is to deliver a higher output voltage with the same DC supply.

2) Good linearity in voltage and/ or current control.

3) Low harmonic contents in the output voltage and /or currents, especially in the low-frequency region.

3.1. Sinusoidal Pulse-Width Modulation (SPWM)

Control technology is the most popular method of pulse width modulation sine adapter's two traditional levels. The tem sinusoidal PWM reference is made to the production of the PWM output signal with a sine wave as a modulation signal [10]. The on and off instants of a PWM signal ill this case, can be determined by comparing the sinusoidal signal (wave modulation) with a triangular wave frequency (carrier wave), as shown in Figure 4 sinusoidal PWM technology is commonly used in industrial applications and abbreviated here as SPWM [11]. Frequency of the modulating wave determines the frequency of the output voltage. The enlargement of the height of the modulation index of the waveform and determines the composition turn control the RMS value of the output voltage [12].

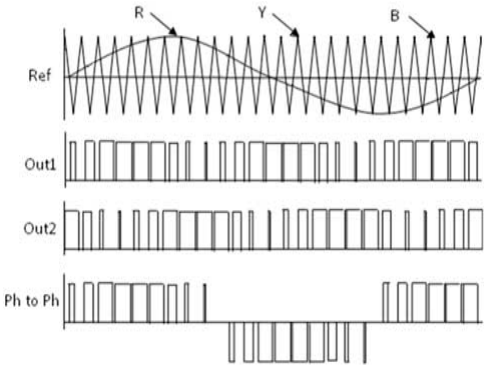

Figure 4. Sinusoidal Pulse Width Modulation for three-phase inverter

The RMS value of the output voltage can be varied by changing the modulation index. The output voltage of the inverter contains harmonics. However, to be paid for the harmonics of

the band around the carrier frequency and its complications [13]. To perform sinusoidal PWM using analog circuit, use a series of bricks:

1) High-frequency triangular wave generator.
2) Sine wave generator.
3) Comparator.
4) Inverter circuits with dead-band generator to generate complimentary driving Signals with required dead band.

3.2. Space Vector Pulse-Width Modulation (SVPWM)

Harmonic content in multilevel inverters can be investigated by generating a space vector pulse width modulation algorithm (SVPWM) signal based on a standard two-level SVPWM. It uses a simple mapping to generate gating signals for the inverter. The circuit structure and switching states of a five-level cascaded H-bridge inverter are introduced. The switching instant of a SVPWM pulse waveform is shown in Figure 6.

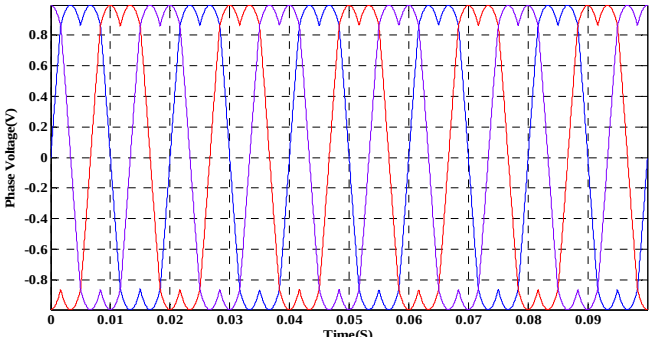

Figure 5. Switching instant of a SVPWM pulse waveform

The proposed modulation is compared in five-level cascaded inverter to reduce high total harmonic distortion, and reduce cost based on five-level cascaded H-bridge that consists of four lookup table 24 switching one DC source inverters. Space vector modulation (SVM) for five-level inverter consists of 16 triangles, in which triangle one has 13 switching states vectors, triangle two-four have 10 switching states vectors, triangle three has 11 switching states vectors, triangle five-seven-nine have 7 switching states vectors, triangle six-eight have 8 switching states vectors, triangle ten-twelve-fourteen- sixteen have 4 switching states vectors and triangle eleven-thirteen-fifteen have 5 switching states vectors [13]. As shown in Figure 6. The algorithm can be easily extended to an ON-level inverter. Its application is for cascaded H-bridge topology as well.

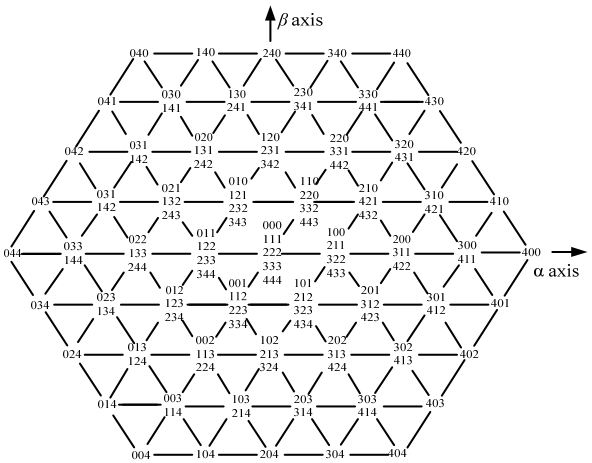

Figure 6. Space vector diagram for five-level inverter [10]

4. Proposed Design of Switching Modulation

4.1. Sinusoidal Pulse Width Modulation (SPWM)

The generations of gating signals with sinusoidal Pulse Width Modulation SPWM are shown in Figure a. there are sinusoidal reference waves ($\upsilon_{ra}, \upsilon_{rb}\ and\ \upsilon_{rc}$) each shifted by 120^0. A carrier wave is compared with the reference signal corresponding to a phase to generate the gating signal for that phase. Comparing the carrier signal with the reference phase $\upsilon_{ra}, \upsilon_{rb}\ and\ \upsilon_{rc}$ produces g_1, g_2 and g_5 respectively as shown in Figure b. the instantaneous line-to-line output voltage is $\upsilon_{ab} = Vs\left(g_1 - g_3\right)$ the output voltage as shown in Figure c, is generated by eliminating the condition that two switching devices in the same arm cannot conduct at the same time. The normalized carrier frequency cf should be odd multiple of three. Thus, all phase-voltage ($\upsilon_{aN}, \upsilon_{bN}\ and\ \upsilon_{cN}$) are identical, but 120^0 out of phase without even harmonics; moreover harmonics at frequency multiple of three are identical in amplitude and phase in all phase. For instance, if the ninth harmonics voltage in phase *a* is:

$$\upsilon_{aN9}\left(t\right) = \upsilon\tilde{}9\sin\left(9wt\right) \tag{1}$$

The corresponding ninth harmonics in phase *b* will be:

$$\begin{aligned}\upsilon_{aN9}\left(t\right) &= \upsilon\tilde{}9\sin\left(9wt - 120\right)) = \upsilon\tilde{}9\sin\left(9wt - 1080\right)) \\ &= \upsilon\tilde{}9\sin\left(9wt\right)\end{aligned} \tag{2}$$

Thus, the ac output line voltage $\upsilon_{ab} = \upsilon_{aN} - \upsilon_{bN}$ does not contain the ninth harmonics. Therefore, for odd multiples of three times the normalized carrier frequency mf , the harmonics in the ac output voltage appear at normalized frequency fh centered around mf and its multiple, specifically, at:

$$n = jmf \pm k \tag{3}$$

$$n = jmf \pm k \pm 1 \tag{4}$$

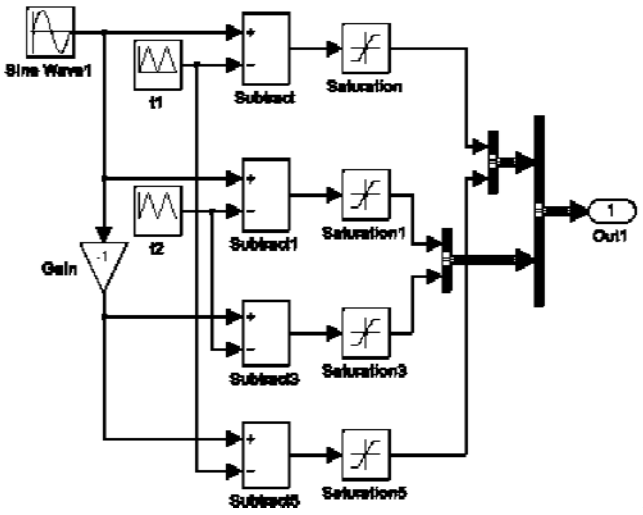

Figure 7. Simulink Five Level of control signal Cascaded H-Bridge Multilevel Inverter

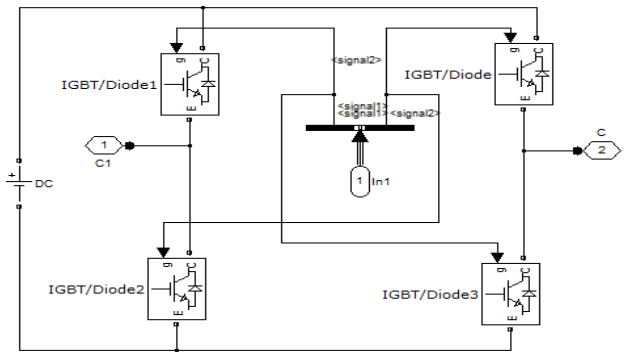

Figure 8 Switching IGBT for Five-Levels Cascaded H-Bridge Multilevel Inverter

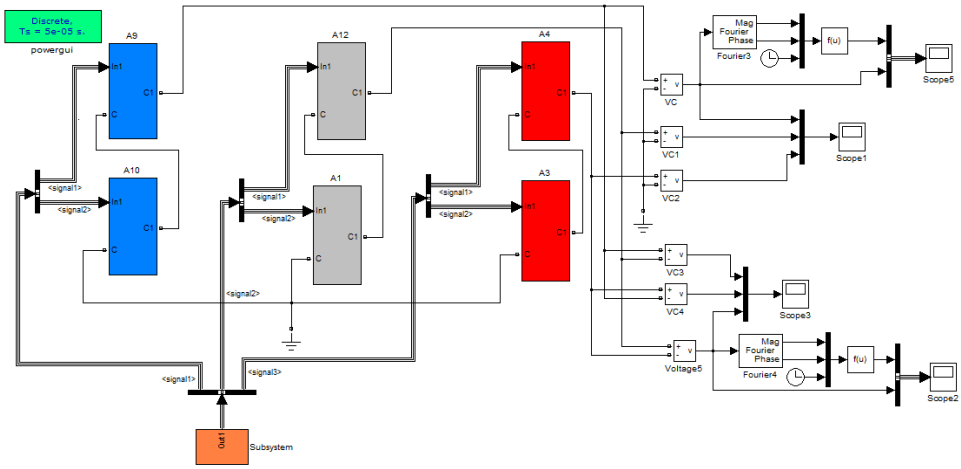

Figure 9. Simulation modeling of SPWM generating Five-level CHB inverter

The considered a good quality of the output voltage if the modulation index (MI) in the range of 0 to 0.95. The five levels that build a multilevel inverters model is exposed out in MATLAB/SIMULINK as shown in Figure 7. Moreover, the simulation diagrams for the seven and nine level similarly are shown in one block. In this simulation, the constant SPWM was used. Each block consists of 4 switches IGBT in Cascaded H-Bridge (CHB) as shown in Figure 8. The value of carrier frequency (fc) used in this designed is about 18 kHz. Figure 9 Simulation modeling of SPWM generating five-level CHB inverter.

4.2. SVPWM Algorithm for CHB-MLI

This section presents the general space vector modulation applied in the presented three-phase n-level CHB inverter. h $(0.866 = \sqrt{3}/2)$ [14] is the height of a sector Si, which is an equilateral triangle of unity side as shown in Figure 10. Space vector selection and switching state sequence of the inverter are discussed. The line-to-line voltage, V_R, V_S, V_T can be obtained through the inverter phase voltage:

$$V_R = m\sin(2\pi\, fs + 90) \tag{5}$$

$$V_S = m\sin(2\pi\, fs + 90 - \frac{2\pi}{3}) \tag{6}$$

$$V_T = m\sin(2\pi fs + 90 + \frac{2\pi}{3}) \quad (7)$$

According the three-phase to two-phase frame transformation, the output voltage of the three-level N-level cascaded H-bridge inverter can be represented by a space vector in the α β frame:

$$\begin{bmatrix} V_\beta \\ V_\alpha \end{bmatrix} = \frac{2}{3}\begin{bmatrix} 1 & \cos\frac{2\pi}{3} & \cos\frac{4\pi}{3} \\ 0 & \sin\frac{2\pi}{3} & \sin\frac{4\pi}{3} \end{bmatrix}\begin{bmatrix} V_R \\ V_S \\ V_T \end{bmatrix} \quad (8)$$

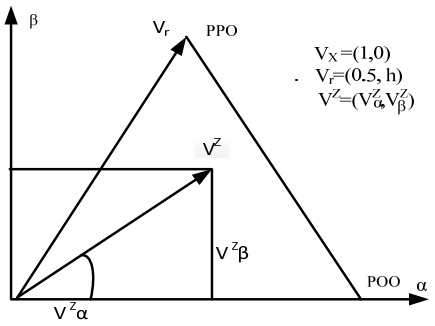

Figure 10. Sector one for two-level inverter [14]

Where V_α and V_β are the real and imaginary components of the space vector respectively. $/\vec{V}/$ is the magnitude and γ is the phase angle of the space vector. The space vector, reference vector, two-level inverter, on-time calculation within a sector $Si,\ i = 1, 2, .., 6.$ for a two-level inverter volt-second equation is Has been discussed in [15]: To apply SVPWM technique, first, the angle (γ) and sector (S_i) of $Vref$ need to be determined by using:

$$\gamma = rem \left(\frac{\theta}{\pi/3}\right) \quad (9)$$

$$S_i = int \left(\frac{\theta}{\pi/3}\right) + 1 \quad (10)$$

In Equation (9) and (10), $0(0^\circ \le 0 \le 360^\circ)$ is the angle of the reference vector with respect to α axis, $\gamma(0^\circ \le \gamma \le 60°)$ is the angle within the sector and $S_i(1 \le S_i \le 6)$ is its sector operation, and *int* and *rem* are standard mathematical functions of integer and reminder, respectively [8]. The space vector diagram of a three-phase voltage source inverter is a hexagon, consisting of six sectors. The purpose of SVPWM algorithm is to identify the triangle in which the tip of the reference vector is located. Each triangle can be treated as a vector of a two-level inverter. The ON-time can be calculated using the small vector analogy of the ON-time equation of a two-level inverter are discussed [8]. In this simulation, the diagram for a five-level inverter using SVPWM technique to generate a cascaded H-Bridge inverter consisted of 24 IGBT switches and four DC source Instead of six Dc source previous work in CHB inverter, as shown in Figure 11. The harmonic and THD profiles of the output voltage and current of the CHB inverters have been investigated. THD for voltage five-level output Cascaded H-Bridge in

multilevel inverters was measured when Modulation Index (MI) was equal to 0.5 to 0.6, 0.75, 0.8 and 0.95. The fundamental frequency, *f* was 50Hz and the inverter switching frequency was 18 kHz.

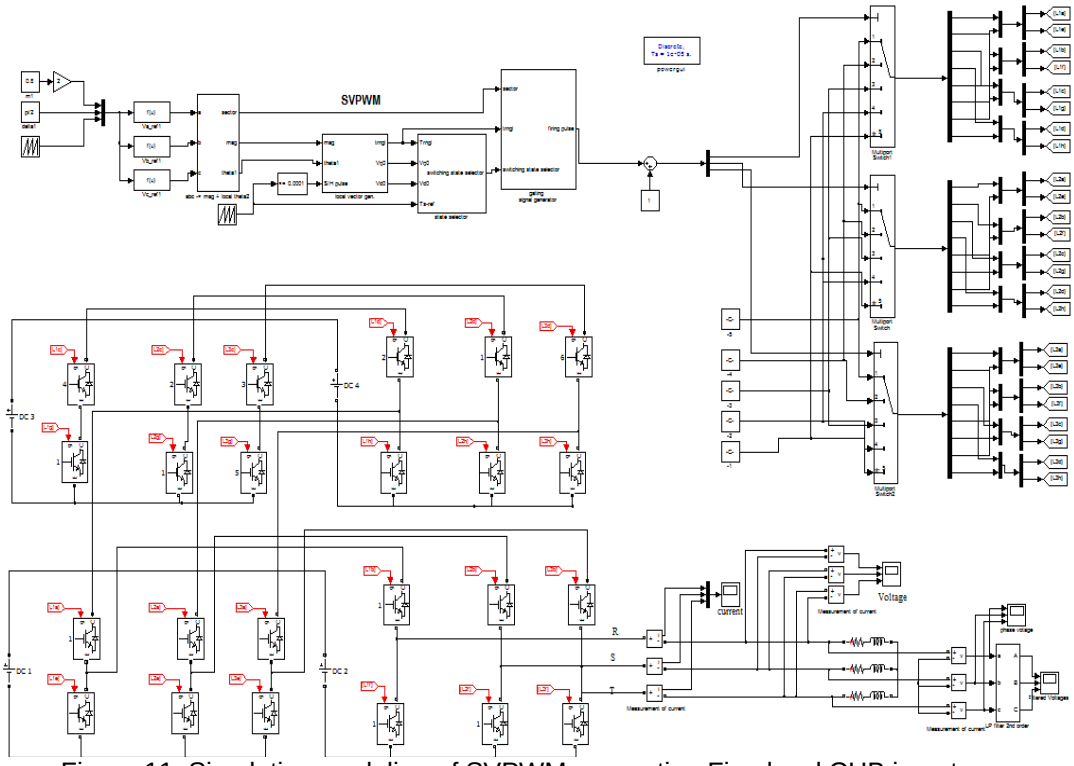

Figure 11. Simulation modeling of SVPWM generating Five-level CHB inverter

5. Simulation Result

5.1. Sinusoidal Pulse Width Modulation (SPWM)

In this paper will present data and result gathered from discussed in preceding papers. In this work of multilevel inverter cascaded H-Bright (CHB) three phase based are using on sinusoidal pulse width modulation (SPWM) control inverter, a simulation module by MATLAB/ Simulink three phase multilevel inverters, Based on the simulation results, a Five-level SPWM inverter is Presented to alleviate harmonic components of output voltage. The simulation results for the five-level cascaded H-Bridge multilevel inverter output voltage line to line (V_{L-L}) waveform, as shown in Figure 12 with modulation index (MI) equals to 0.6 the full wave with modulation index (MI) equals to 0.75, 0.8 and 0.9 as shown in Figure 13, 14 and 15 respectively.

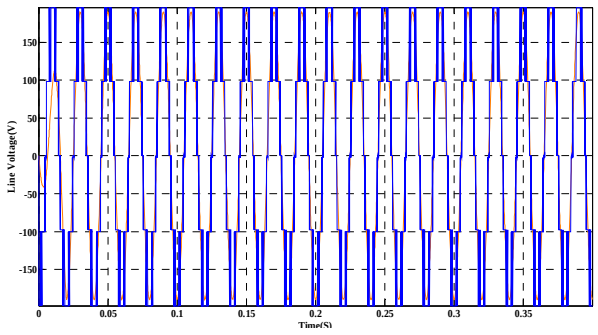

Figure 12. Line Voltage SPWM, MI=0.6

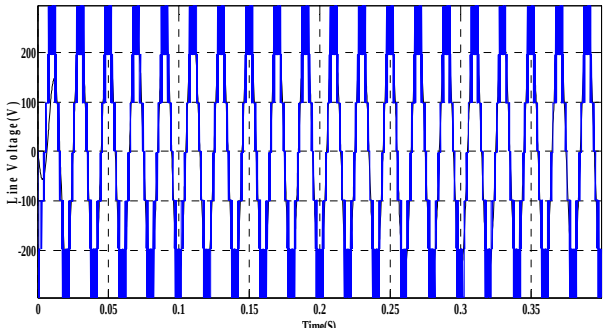

Figure 13. Line Voltage SPWM, MI=0.75

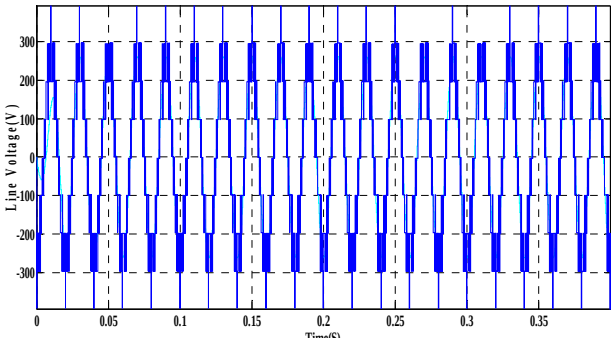

Figure 14. Line Voltage SPWM, MI=0.8

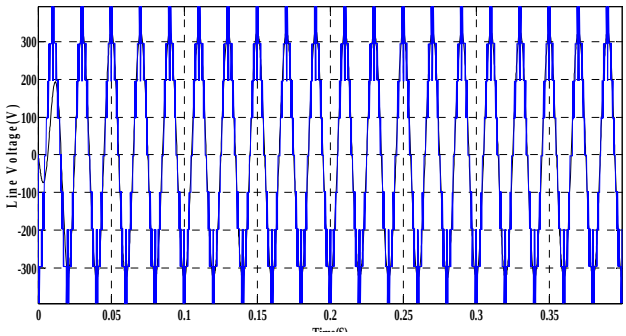

Figure 15. Line Voltage SPWM, MI=0.95

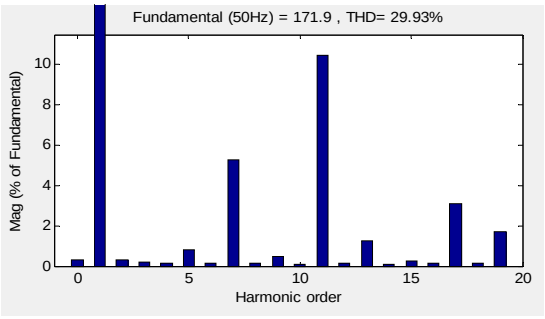

Figure 16. Harmonic Voltage SPWM, at MI=0.6

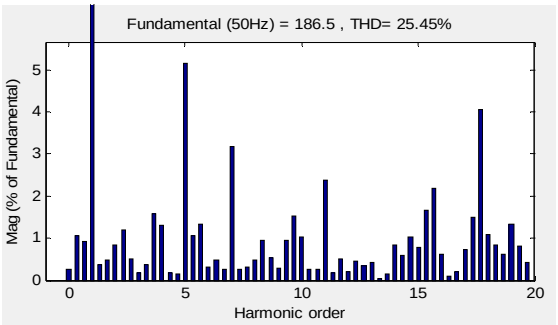

Figure 17. Harmonic Voltage SPWM, at MI=0.75

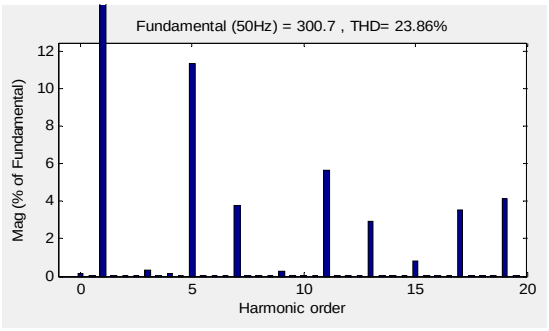

Figure 18. Harmonic Voltage SPWM, at MI=0.8

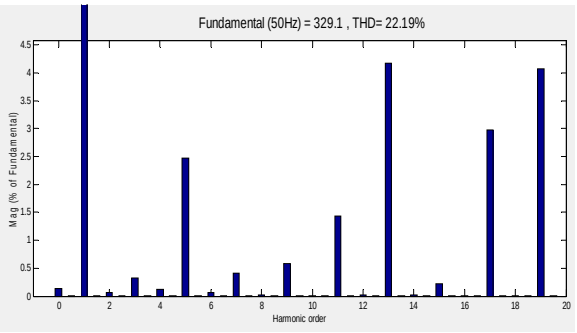

Figure 19. Harmonic Voltage SPWM, at MI=0.95

FFT analysis of the SPWM five levels cascaded H-Bridge multilevel inverter output are shown in Figure 16, 17, 18, and 19 continuously. The THD_V for voltage obtained of the output cascaded H-Bridge multilevel inverter when modulation index equals to 0.6, 0.75, 0.8 is lower when the modulation index equals to 0.95.

5.2. Space Vector Pulse-Width Modulation (SVPWM)

In order to validate the performance of the proposed schemes, a simulation model for three-phase CHB multilevel inverters was developed. Line voltage for the three-phase cascaded H-Bridge five-level inverter with modulation index of 0.6-0.75, 0.8 and 0.95 are shown in Figure 20, 21, 22 and 23 continuously.

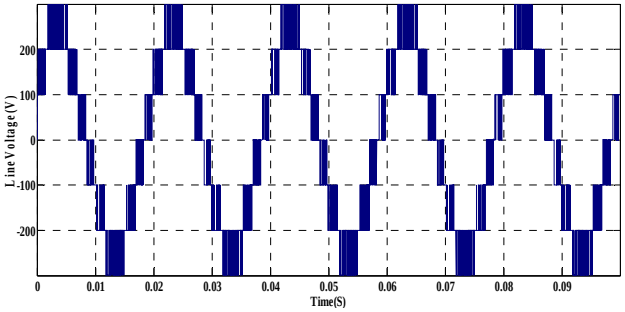

Figure 20. Line Voltage SVPWM MI=0.6

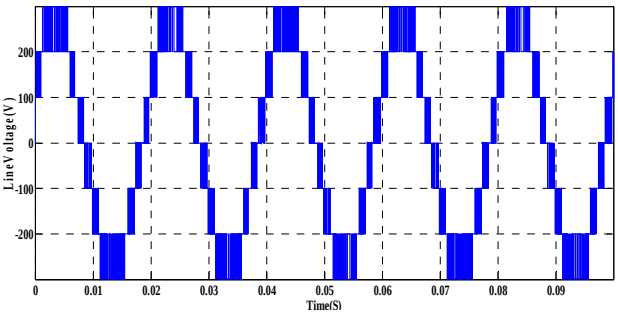

Figure 21. Line Voltage SVPWM MI=0.75

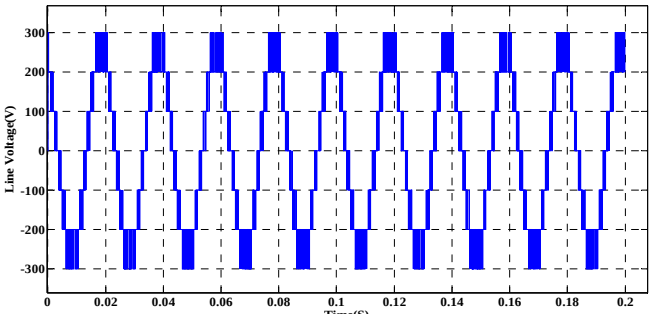

Figure 22. Line Voltage SVPWM MI=0.8

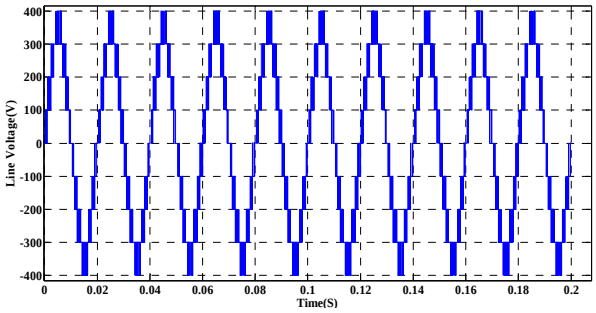

Figure 23. Line Voltage SVPWM MI=0.95

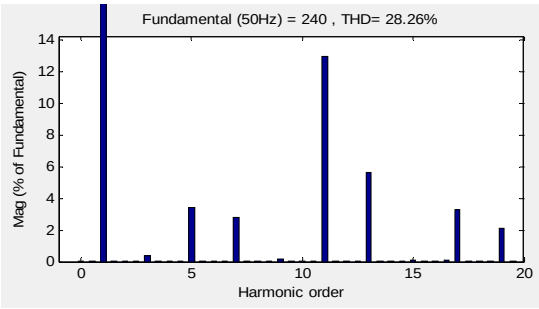

Figure 24. Harmonic Voltage SVPWM, at MI=0.6

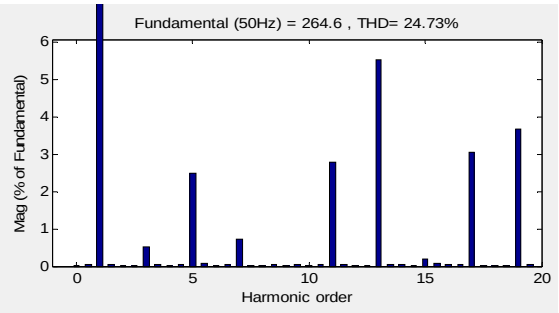

Figure 25. Harmonic Voltage SVPWM, at MI=0.75

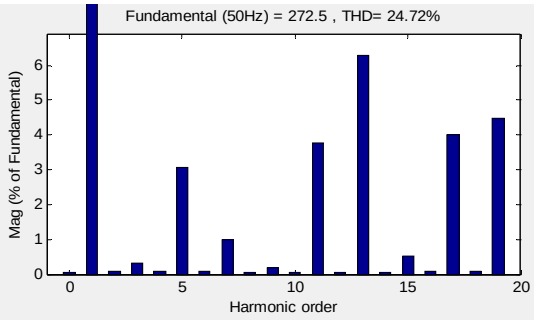

Figure 26. Harmonic Voltage SVPWM, at MI=0.8

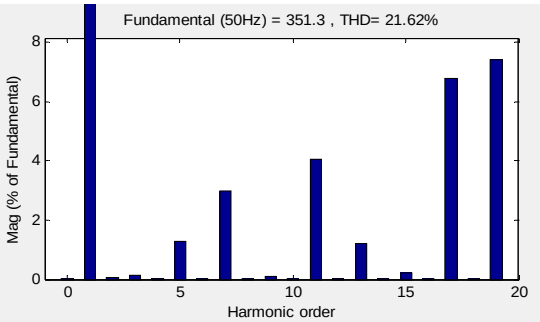

Figure 27. Harmonic Voltage SVPWM, at MI=0.95

FFT analysis of the SVPWM five levels cascaded H-Bridge multilevel inverter output are shown in Figure 24, 25, 26, and 27 continuously. The THD_V for voltage obtained of the output cascaded H-Bridge multilevel inverter when modulation index equals to 0.6, 0.75, 0.8 is lower when the modulation index equals to 0.95.

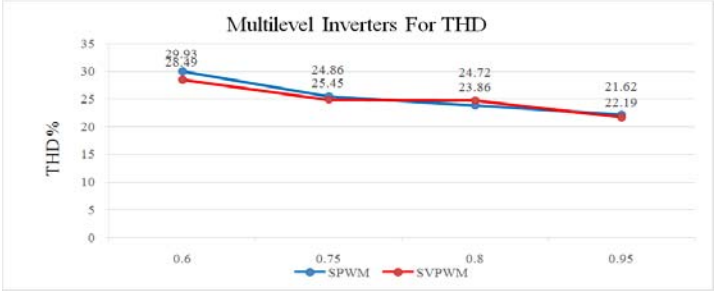

Figure 28. Modulation Index Five Level inverter for Harmonic Reduction

6. Conclusion

In this paper presents a comparative study between sinusoidal pulse width modulation (SPWM) and space vector pulse width modulation (SVPWM) technique, based on generate signal five level of cascaded H-bridge for reduction harmonics in the multilevel inverter output. Simulink models were developed for the space vector modulation and sinusoidal pulse width modulation CHB inverter. The proposed modulation was compared five-level cascaded inverters to reduce high total harmonic distortion, high reduce cost based on CHB are implemented. For space vector modulation Simulink is reduce the component get better harmonic distortion then sinusoidal pulse width modulation from the study, better performance is obtained when the modulation index increases.

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