COMPARATIVE STUDY OF ENCODERS FOR PARALLEL-TYPE ADCs

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Abstract - *Analog-to-digital converters (ADCs) for high sampling frequencies have parallel-type architectures, where the output of the comparators is the so-called "thermometer code". The digital part of such ADCs can be just an encoder from the thermometer code to binary code; however, different types of error correction can be implemented to enhance the ADC overall performance. In this paper we compare three different types of encoders: without error correction; with 1st order error correction; with nth order error correction. These encoders are compared with respect to the yield of the ADC with the different encoders, assuming the use of an identical analog part. The yield is defined by four different criteria: monotonicity, absence of missing codes, and either integral or differential nonlinearity below a specified value.*

Keywords - Analogue-to-digital converters, Parallel ADCs, Thermometer code-to-binary Encoders, Digital error correction.

1. INTRODUCTION

High-speed ADCs with sampling frequencies in the tens (or hundreds) of MHz have parallel-type architectures. The full-parallel architecture is the most used architecture when speed is the most important requirement, although this architecture requires a large number of comparators (2^N-1 for N bits), which leads to large area and power consumption [1]. Due to this constraint and also to the comparators' offset voltage, the resolution is usually limited to 8 bit. Alternatives to the full-parallel architecture are the two-step and the pipeline architectures [1], where full-parallel ADCs with a reduced number of bits are used as sub-circuits.

The comparators' offset voltage (V_{os}) is of particular importance because it is responsible for the static nonideal performance: it imposes limits on the integral and differential nonlinearity and may originate missing codes or even be responsible for non-monotonic behaviour [1]. V_{os} , due to mismatches, is a random variable which is assumed to have a normal distribution [1]. Although, V_{os} can be reduced by circuit design techniques, this usually leads to an increase of power consumption and area. The latched comparators output is the so-called thermometer code ("…000111…") and the offset voltage of the comparators can cause "bubbles" (e.g., "…010111…") in this thermometer code originating errors in the output code. The encoders can be designed to correct large errors, that appear as non-monotonicity of the transfer characteristic of the ADC or as missing codes, or even to reduce large nonlinearity errors, using digital correction schemes.

We have divided the encoders into three different classes: without error correction; with 1st order error correction, where simple bubbles can be corrected with a minor modification to the basic encoder; and with n^{th} order error correction, where n^{th} order bubbles can be corrected.

The n^{th} order error correction encoders considered are the Mangelsdorf [2], the *bit swapping* [3], and the *Wallace tree* [4] encoders. The first two use a thermometer code corrector, between the comparators and the encoder input to make the correction of the thermometer code. A different approach is used by the *Wallace tree* method: instead of correcting the thermometer code the number of "1s" is evaluated.

These different classes of encoders are compared for the cases N=8 bits and N=4 bits. These are practical values, respectively, for full-parallel ADCs and for sub-converters in a two-step architecture. The expected yields of an ADC are compared, for different encoders, using as criteria the requirement of monotonicity, absence of missing codes, and either integral or differential nonlinearity below a specific value.

2. PARALLEL-TYPE ADCs

In a full-parallel ADC (Fig. 1) the input voltage v_I is applied to a bank of latched comparators, where it is compared with

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the equally spaced reference voltage levels obtained from the resistor ladder. The reference voltage levels are the transition voltage levels in the transfer characteristic of an ideal ADC (Fig. 1). All the comparators with reference voltage below v_I exhibit a logic level and all the comparators with reference voltage above v_I exhibit the complementary logic level resulting in the so called thermometer code ("…0001111…"). This code is encoded to binary form by an encoder block.

The full-parallel ADC uses 2^N-1 comparators (hence large area and high power consumption); alternative architectures like two-step parallel (Fig.2), are used to reduce the number of comparators. Two-step or multi-step architectures usually use full-parallel ADC sub-circuits.

The subject of ADC characterization is still under discussion. In this paper we will consider that the ideal ADC transfer characteristic has equal code bin widths, and the static parameters used are defined as follows [5]:

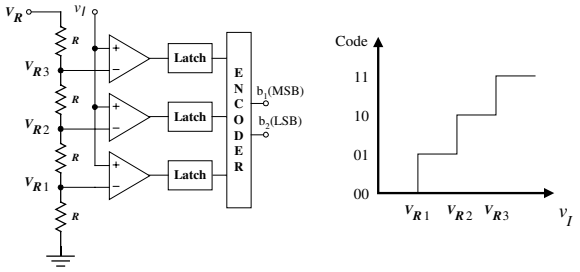


Fig. 1- Full-parallel ADC and transfer characteristic.

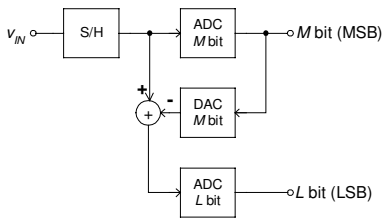


Fig. 2- Two-step parallel ADC.

Monotonic ADC: the output codes do not decrease (increase) for a uniformly increasing (decreasing) input signal, disregarding random noise.
Missing Code (MC): a code that does not occur for any value of the input signal.
Integral nonlinearity (INL): Maximum difference between the ideal and the actual code transition levels after correcting for gain and offset.
Differential nonlinearity (DNL): Maximum difference between the ideal and the real code bin width.

3. DIFFERENT TYPES OF ENCODERS

(1) Basic Encoder

The simplest circuit to convert the thermometer code to binary code uses a decoder with XOR gates to detect the 0→1 transition in the thermometer code and then address a ROM for the proper binary encoding (Fig. 3). The ROM can be implemented with NMOS transistors and pull-up devices (pull-up resistors are represented in Fig. 4). This encoder does not perform any error correction, so a bubble in the thermometer code will cause that at least three lines are addressed in the ROM, resulting in the AND of the corresponding three output codes. This will cause a non-monotic transfer characteristic for the ADC and the existence of a missing code.

(2) Encoder with 1st Order Error Correction

By using 3-input XOR gates, instead of the 2-input XOR gates in the simple encoder just presented, 1st order errors (*bubbles*) in the thermometer code can be partially corrected, thus avoiding the addressing of several lines in the ROM: a non-monotonic transfer characteristic is avoided but a missing code may occur.

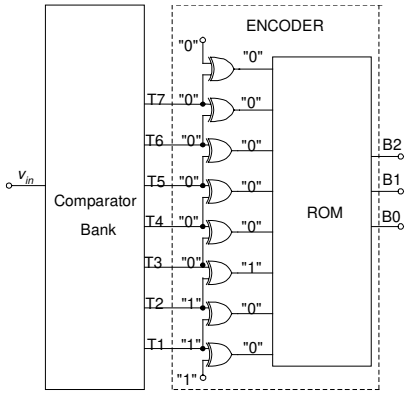


Fig. 3 - Basic Encoder.

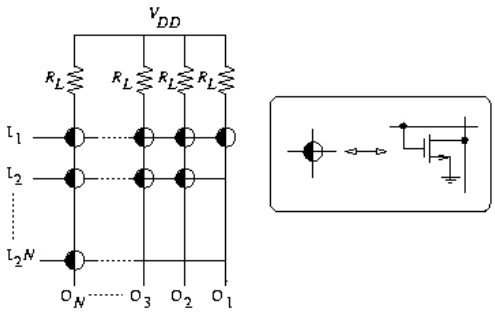


Fig. 4 - NMOS ROM with pull-up resistors.

(3) Encoder with n^{th} Order Error Correction

A higher order error correction encoder using the *Mangelsdorf* [2], the *bit swapping* [3] or the *Wallace tree* [4] methods can improve the correction, with respect to the previous correction scheme, and can perform correction of higher order bubbles, depending on the method chosen.

(a) Mangelsdorf method

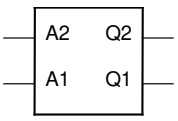
The Mangelsdorf method corrects the thermometer code before encoding. The output of each comparator is compared with the outputs of the two adjacent comparators and changed if it is different from both. Each comparator corrected output is T'_N:

$$T'_N = T_{N-1} \cdot T_N + T_N \cdot T_{N+1} + T_{N-1} \cdot T_{N+1}$$

where T_N: is a comparator output without correction. This method corrects one digit bubble in any position (e.g., "…000100111…") but not bubbles that are more than one digit long (e.g., "…00011001111…").

(b) Bit swapping method

The bit swapping method also corrects the thermometer code and then uses a basic encoder. The logic operation represented in Fig.5 is performed between each two consecutive comparators and bubbles in the thermometer code descend if they are "1s" or ascend if they are "0s".



A1	A2	Q1	Q2
0	0	0	0
0	1	1	0
1	0	1	0
1	1	1	1

Fig. 5 - Bit swapping latching element and truth table.

In order to perform correction of n^{th} order bubbles it is necessary to use n columns of bit swapping latches, and therefore the order of error correction to be performed should be carefully evaluated.

(c) Wallace tree method

If the *bit swapping* method is implemented with its maximum order (2^N) the algorithm is equivalent to counting the number of "1s". The *Wallace tree* method implements the same algorithm directly, without moving the "1s" through the thermometer code (this method is used to implement high speed multipliers in computer arithmetic units). The *Wallace tree* method is different from the previous; instead of correcting the thermometer code and then using a basic encoder, it uses a single block where both operations are performed. An example for a three bit encoder is presented in Fig.6 where the basic cell is a summing circuit of "1´s". The truth table of this basic cell is presented in Table 1 where *a*, *b* and *c*, are the bits to be summed, *S* is the sum result and *C* is the "*carry*". If the result is presented with the format "*CS*" then it represents the number of ones at the input in binary form.

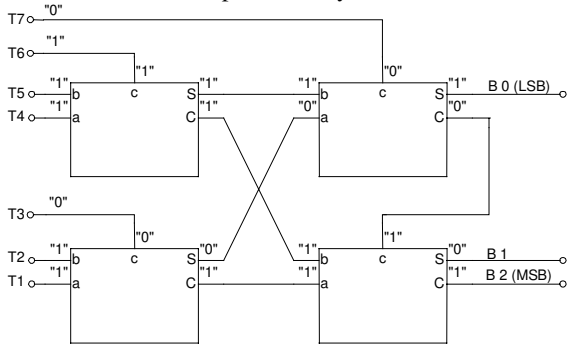


Fig.6: Wallace Tree Encoder (example for 3 bit).

Table I - Summing block truth table.

abc	000	001	010	011	100	101	110	111
CS	00	01	01	10	01	10	10	11

The tree structure means that there is an increase in the number of stages with the number of bits; however the internal nodes are all low capacitance node ensuring a fast response.

4. COMPARATIVE STUDY

To compare the three classes of encoders we have simulated two full-parallel ADCs (with N= 8 bit and N= 4 bit) imposing an offset at each transition point of the transfer characteristic. This offset is a random variable with normal distribution [1], and models the offset voltage of the latched comparator which is assumed to have zero mean and to be independent for different comparators. The most significant results are presented in Fig. 7, where the yield is the percentage of ADCs that meet the specific criteria. The results for the monotonicity criterion are obtained from 2000 samples; for the missing code and INL ≤ 1.5 LSB criteria the results are obtained after discarding the samples that have failed the monotonicity criteria.

The results plotted for "n^{th} order error correction encoder" correspond to the highest order correction (2^N) level.

Our comparative study leads to the following general conclusions:

I. The non-monotonic behaviour can be totally eliminated by the use of an n^{th} order error correction encoder. For the basic and the 1st order error correction encoders the yield reduction due to non-monotonicity is significant, even for very low values of the offset voltage.

II. The missing code criteria shows that the n^{th} order error correction encoder can again be very effective in improving the yield. The basic encoder can be apparently better than the encoder with 1st order error correction, but it should be noted that we have only considered the yield due to absence of missing codes after excluding the non-monotonic ADCs.

III. The results concerning INL and DNL lead to the same general conclusions. For nonlinearity lower than 1 the n^{th} order error correction encoder shows a slight improvement over the other encoders, but it should be noted that these results are based on the samples that have passed the monotonicity criterion; for nonlinearity greater than 1, the n^{th} order error correction encoder shows a significant improvement over the other encoders, and this improvement is more important for higher resolution or

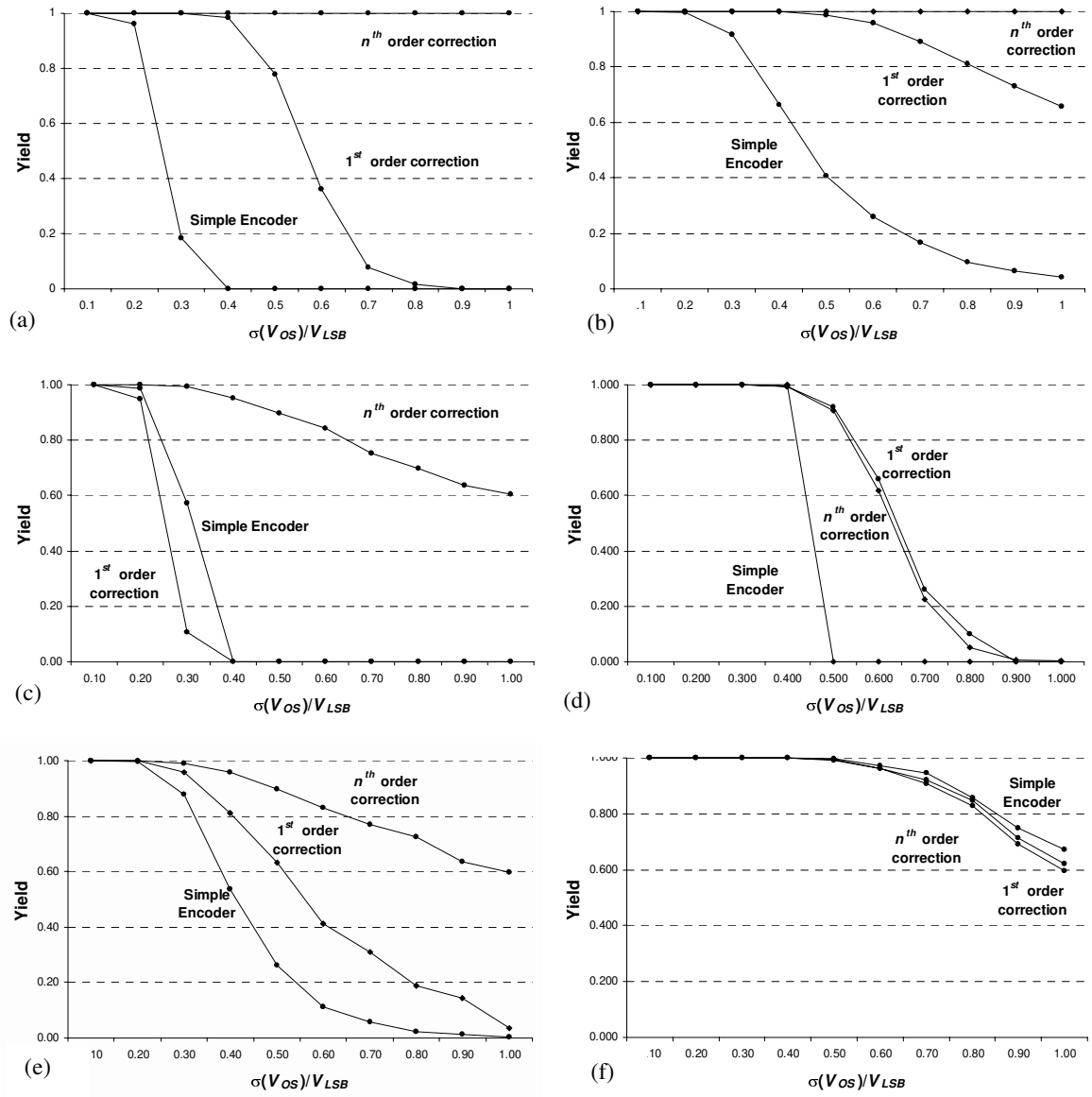


Fig.7 - ADCs Yield for (a) N=8 bit, Monotonicity; (b) N=4 bit, Monotonicity; (c) N=8 bit, Missing codes; (d) N=4 bit, Missing codes; (e) N=8 bit, INL ≤ 1.5 LSB; and (f) N=4 bit, INL ≤ 1.5 LSB

higher $\sigma(V_{OS})/V_{LSB}$.

These conclusions show that is desirable to use a 1st order error correction encoder, a Mangelsdorf encoder, or a low order *bit swapping* encoder, because the yield is significantly enhanced without a high cost with respect to the simple encoder. The Wallace tree encoder or a higher order bit swapping encoder improve the ADC Yield for all the criteria and can be justifiable when the resolution increases (lower V_{LSB} and higher number of transition levels), or when the offset voltage increases. The choice between these two encoders depend on the order of error correction. If higher order error correction is needed the Wallace tree encoder is the most suitable, but it may be too costly for high resolutions. In this case, a medium (3rd or 4th order) order error correction using the bit swapping encoder can be the best solution, since it is a good compromise between efficiency and added circuitry.

5. CONCLUSIONS

In this paper we consider three types of thermometer-to-binary code encoders: without error correction; with 1st order error correction and with n^{th} order error correction. These encoders are studied and compared with respect to the expected yield of the ADC, with the different encoders, defined by four different criteria: monotonicity, absence of missing codes, and either integral or differential nonlinearity below a specific value.

The results show that low order error correction produces a significant increase in yield with a small increase in circuitry. For medium resolution ADCs, the Wallace tree is the most effective because it leads to an increase of performance (not only of the yield) with acceptable added circuitry. For higher resolution ADCs the Wallace tree encoder can become too costly and the use of a medium order error correction using bit swapping can be a compromise between improved performance without to much added circuitry.

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