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Comparator-based switched-capacitor pipelined analog-to-digital converter with comparator preset, and comparator delay compensation

Carsten Wulff · Trond Ytterdal

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Abstract We present a differential comparator-based switched-capacitor (CBSC) pipelined analog-to-digital converter (ADC) with comparator preset, and comparator delay compensation. Compensating for the comparator delay by digitally adjusting the comparator threshold improves the ADC resolution from 2.5-bit to 7.05-bit. The ADC is manufactured in a 90 nm CMOS technology, with a core area of 0.85 mm × 0.35 mm, a 1.2 V supply for the core and 1.8 V for the input switches. It has an effective number of bits (ENOB) of 7.05-bit, and a power dissipation of 8.5 mW at 60 MS/s.

Keywords Analog-to-digital converter · Comparator-based switched-capacitor circuit

1 Introduction

Scaling down CMOS technology into the nano-scale range (below 100 nm gate-length) creates new challenges for the analog designer. Gone are the days of transistors with high output resistance and high voltage tolerance. With a power supply of 1.2 V in a 90 nm CMOS technology, and a threshold voltage up to 0.5 V in a low-power flavor there is not much headroom to stack transistors, and when the transistor intrinsic gain[1] worsens with each technology node—down to a gain of around 16 times in 90 nm—it makes a high performance operational transconductance amplifier (OTA) harder to design. This presents a challenge because OTAs are the key component in most switched-capacitor circuits, and switched-capacitor circuits are the de facto standard for implementing ADCs. The challenges in nano-scale CMOS has caused a flurry of research into removing the OTA, where one of the research avenues has led to the comparator-based switched-capacitor circuits (CBSC) [1, 2]. In this paper we'll present a pipelined ADC based on this technique.

This paper is organized as follows, we'll introduce comparator-based switched-capacitor circuits in Sect. 2. Sections 3 and 4 describe in detail the implementation of the ADC. The test setup is detailed in Sect. 5 and the measurement results explained in Sect 6.

2 Comparator-based switched-capacitor circuits

A nice thing about the switched-capacitor circuit is that it does not matter how it arrives at the output voltage. We just have to make sure that the output voltage is correct when the next stage samples. Back in 2006 an idea was put forth for a new method of implementing switched-capacitor circuits [1]. Instead of an OTA, they used a current source and a comparator, and called it CBSC, that name has later transformed into zero-crossing-based switched-capacitor circuits (ZBSC), but we'll use the original name, CBSC, in this paper, because this work was based on the original publication.

An example of a single-ended CBSC amplifier in the charge transfer phase is shown in Fig. 1. In the sampling phase (not shown) the input voltage is sampled across both capacitors. At the start of the charge transfer phase the output is reset to the lowest voltage in the system. This

C. Wulff (✉) · T. Ytterdal
Norwegian University of Science and Technology, Trondheim, Norway
e-mail: carsten@wulff.no

[1] The intrinsic gain is the transconductance divided by the output conductance, or g_m/g_{ds}.

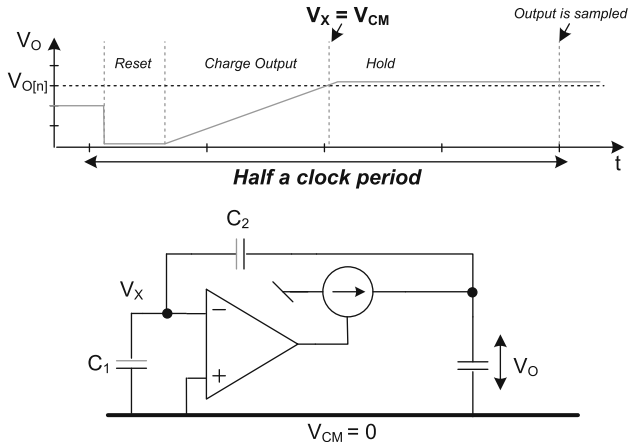

Fig. 1 Comparator-based switched-capacitor circuit. The sampling phase is equivalent to OTA-based switched-capacitor, and is not shown in the figure. At the start of the charge transfer phase the output is reset, after a delay the current source begins to charge the output. When a voltage of zero is detected between V_X and V_{CM} the current source is turned off

ensures that V_X start below the virtual ground. The current source is turned on at the start of reset and use reset to settle. When reset ends the current source charges the output capacitance. The voltage at V_O and V_X rises until the comparator detects virtual ground ($V_X = V_{CM} = 0$), and turns off the current source.

2.1 Sampling of stage output

In our ADC the next stage samples at the end of the charge transfer phase. This is different from the original sampling in [1], where they used the signal from the comparator to sample in the next stage, thus ensuring no problems with charge leakage. The reason for our method was that we believed it would give us increased speed, we wanted our ADC to run at 100 MHz, not 10 MHz as in [1], so we believed that it would be better to use the clock phases to sample, and not the comparator output. This was an error, and as a result we had to run the ADC above 10 MS/s. Below 10 MS/s the change in voltage from the ramp stopped, to the output was sampled, became significant. Accordingly, we recommend that others use the comparator signal for sampling in the next stage, as suggested in [1].

2.2 Comparator delay compensation

Since any real comparator has a delay it takes a moment for the current source to turn off, which results in a overshoot of the output voltage. Methods to compensate for this overshoot exists, in [1, 3] they used a dual ramp system, first a fast ramp to estimate the output voltage, then a slow ramp to fine tune the output voltage. Since the ramp was slow the comparator delay caused an insignificant voltage change. A dual ramp system was also used in [4], but they included an additional compensation for overshoot using a switched-capacitor circuit. In [5] an analog signal was globally adjusted to compensate for the offset of the ADC. The scheme used in [6] (presented February 2009) is similar to the scheme we choose for our ADC, which was taped out July 2007, but we compensate for the comparator delay differently.

2.3 Non-linearity caused by switches

In an OTA based switched-capacitor circuit the voltages settle, and the current through the feedback network asymptotically approaches zero. In a CBSC circuit this does not happen, the current through the feedback network is almost constant until it is turned off. As a result, switch resistance causes an offset and a non-linearity [3, 5]. But effects can be minimized by splitting the current source [5], or reducing switch resistance. In our implementation low-threshold voltage transistors were used in critical switches to get low resistance.

3 The ADC architecture

A system level diagram of the ADC is shown in Fig. 2. The ADC has seven 1.5-bit pipelined stages and a 1.5-bit flash-ADC. The target specification of the ADC was 10-bit, 100 MHz, and 10 mW. So the ADC was designed as a 10-bit ADC with eight 1.5-bit stages and a 2 bit flash-ADC. But measurements showed more noise than expected (the noise was dominated by the digital IO). To reduce the noise coupling we disconnected the output from the flash ADC, and turned off currents in Stage 8. The sub-ADC in Stage 8 was used for the LSB.

Bias current was controlled with a on-board variable resistor. External reference voltages were used to save design time, so the power consumed by the references is not included in reported power dissipation. The digital outputs from the SADCs are brought off-chip by CMOS logic IO buffers. Synchronization, recombination and digital error correction of the output bits was performed in software. An offline calibration algorithm, which will be explained later, was used to find the correct comparator offset correction and current source current. An on-chip non-overlapping clock generator made the clock phases needed by the pipelined stages.

3.1 Pipelined stage

The first stage (Stage 1) is shown in Fig. 3 during sampling and charge transfer. Stages 2–7 are identical to Stage 1

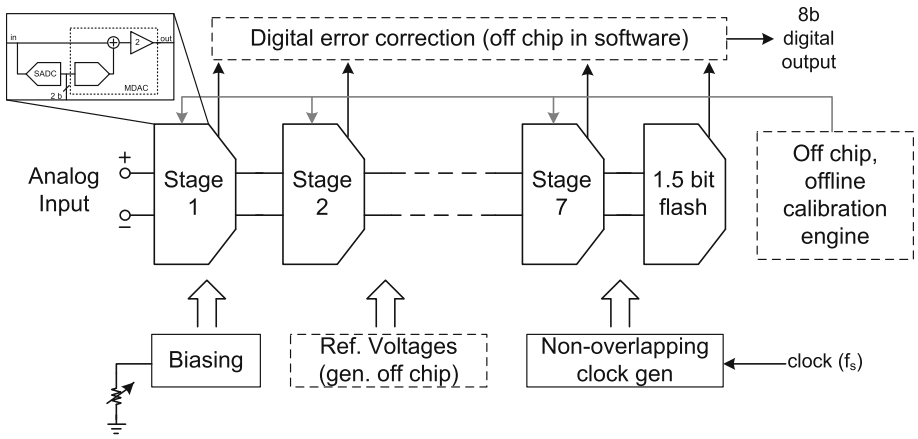

Fig. 2 System level diagram of the pipelined ADC

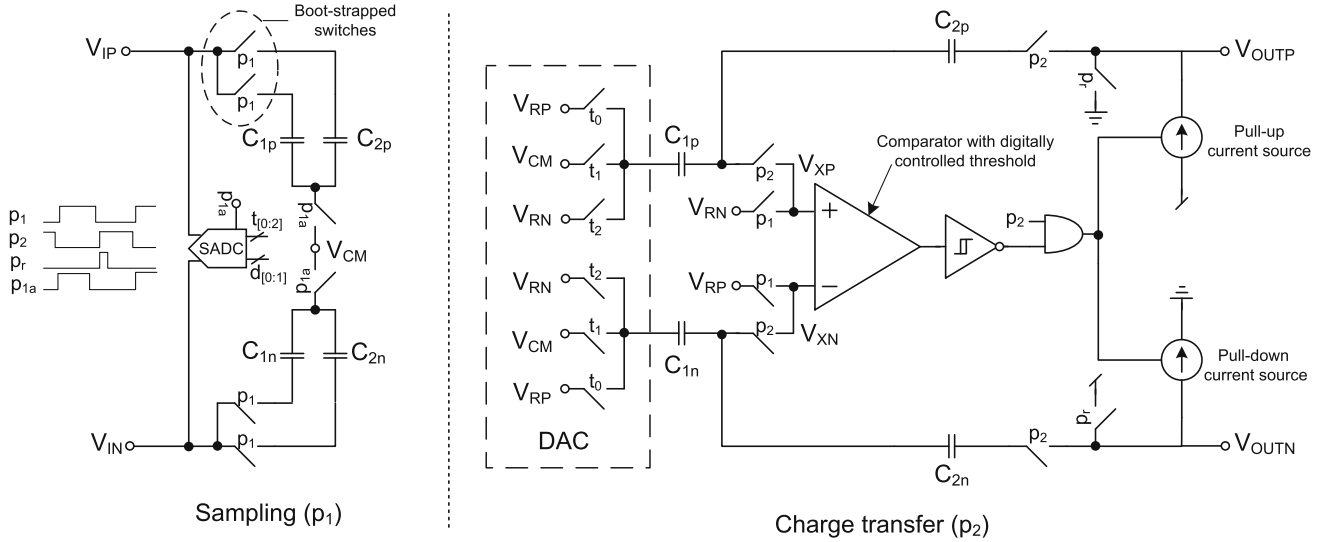

Fig. 3 Stage one shown during the two phases, sampling and charge transfer

with the exception of the input switches and capacitor size. The input switches are bootstrapped in the first stage, but regular transmission gates in later stages. Each pipelined stage has a 1.5-bit analog-to-digital converter (SADC). The signals t_0, t_1 and t_2 are the digital outputs of the SADC that controls the DAC during charge transfer. The stage operates on four clock phases: p_1, p_2, p_r and p_{1a}. An advanced (as in transitions before) clock phase (p_{1a}) samples the input signal before p_1 turns off, this reduces the problem of signal dependent charge injection from p_1 switches. The voltages V_{CM}, V_{RN}, V_{RP} are the common mode voltage, negative reference voltage, and positive reference voltage, respectively.

4 ADC components

An ADC has several components, it has comparators, clock generators, digital IO, bias distribution and switches. In a CBSC ADC the key components are the high output-resistance current sources and the comparator to turn them off. In this section we'll go through the key components.

4.1 Current sources

The current sources in a CBSC ADC must have high output resistance and they must tolerate high swing to get a linear voltage ramp. A standard current mirror in a 90 nm CMOS technology has a low output resistance, on the order of 100 kΩ. A cascode can increase the output resistance around 10 times, up to 1 MΩ. To further increase the output resistance we used gain boosting, also called active cascode, or regulated cascode [7]. With a one stage amplifier used as a gain booster the output resistance can increase 10 times, up to 10 MΩ. A simplified schematic of the pull-down current source can be seen in Fig. 4, for the actual schematics see [8].

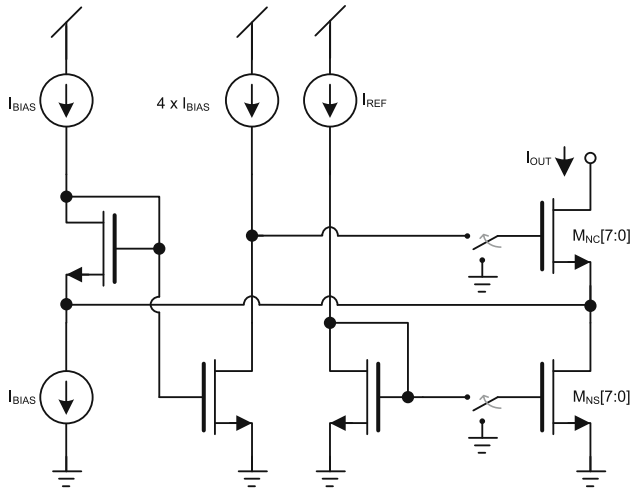

Fig. 4 NMOS current source. M_{NX}[7:0] is a notation for a digitally controlled transistor size. A transistor pair (for example M_{NC}[0] and M_{NS}[0]) can be disabled by a calibration bit. The enabled transistor pairs gates are pulled to ground when the comparator output in Fig. 3 is high

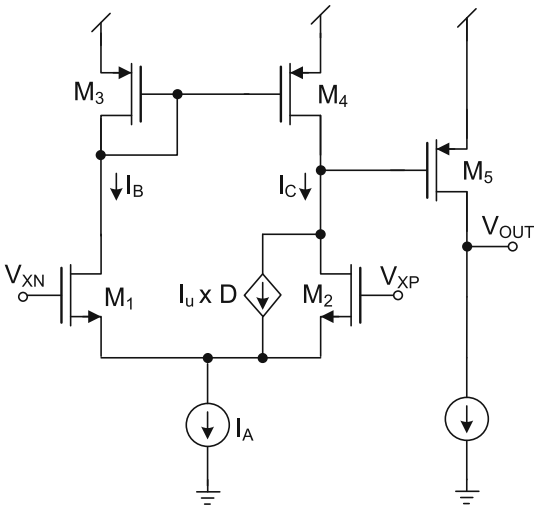

Fig. 5 Comparator with adjustable threshold

The size of the cascode and current source transistor can be digitally controlled (transistor width M[7:0]) by calibration bits. The current scaling is controlled by an 8-bit word. With this architecture the gain booster will see a varying load, but this was not a significant design challenge.

4.1.1 *Output common mode in CBSC circuits*

Assume that the current sources are symmetric, and that we reset V_{OUTN} to VDD and V_{OUTP} to VSS. When the comparator turns off the current sources the common mode output will be at VDD/2. A delta current between the pull-up and pull-down current sources will change the output common mode voltage. The output voltage of the stage is given by $dV = \frac{I(t)\times dt}{C}$, where we assume $I(t)$ is constant. With an output capacitance of 600 fF, a delta current of 5 µA, and a charge-transfer phase of 8 ns, the common mode will change 67 mV. This is within acceptable limits, so our circuit did not include any common mode feedback circuit. For a detailed discussion of CBSC output common mode and power supply rejection ratio see [9].

4.2 Comparator with adjustable threshold

A two-stage continuous-time amplifier with a differential first stage and single ended common source second stage was used as the comparator. A simplified schematic of the comparator is shown in Fig. 5.

In phase p_1 the comparator inputs are reset to V_{RN} and V_{RP} (as shown in Fig. 3), so the output is known at the end of sampling phase (p_1). With this preset the control logic to turn off the current source at the right time consist of a single Schmitt trigger and an AND gate. The preset also ensures that the comparator does not need to slew when we enter the charge transfer phase (p_2), where we have very little time to do anything more than strictly necessary.

In the charge transfer phase the stage outputs are reset (p_r), forcing a slight increase in V_{XN} and decrease in V_{XP}, the amount of change depends on the stage input voltage (see Fig. 6 for a visualization). When reset is complete (p_r goes low) the current sources charge the output, and V_{XN} falls and V_{XP} rises. When they meet we want to turn off the current sources, because that is when we have zero charge across capacitors C_{1p} and C_{1n} (assuming the DAC output is connected to V_{CM}), and all the charge is transferred to C_{2p} and C_{2n}.

Figure 6(a)–(c) shows V_{XN} and V_{XP} as a function of time for different comparator thresholds (V_{ct}). The comparator should turn off current sources when $V_{XP} = V_{XN}$, but because the comparator has a delay (t_c) the current sources turn off later, causing an overshoot (Fig. 6(a)). Adjusting the threshold of the comparator changes the amount of overshoot. If V_{ct} is adjusted optimally there is no overshoot (Fig. 6(b)). If V_{ct} is lower than the optimal value the output undershoots (Fig. 6(c)). From the figure we see that a non-optimal threshold cause an offset in the stage output, as shown in [10].

To control the comparator threshold we use a 6-bit current DAC in parallel with M_2, shown as a controlled source in Fig. 5. In the figure I_u is a unit current and D is an integer given by $D = 2^0b_0 + 2^1b_1 + 2^2b_2 + 2^3b_3 + 2^4b_4 + 2^5b_5$. The current in the current source I_A is the sum of the two branch currents ($I_A = I_B + I_C$). The comparator threshold is defined as the differential input voltage when

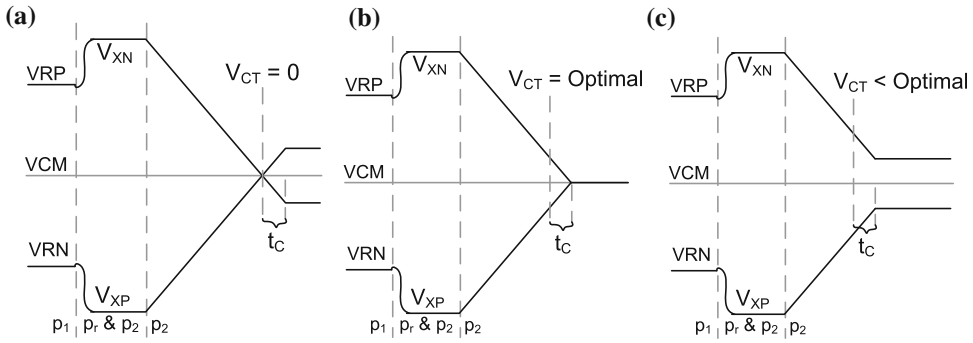

Fig. 6 Voltage versus time for the nodes V_{XN} and V_{XP} as a function of comparator threshold. **a** Comparator threshold equal to zero. **b** Optimal comparator threshold. **c** Comparator threshold less than the optimal value

the branch currents are equal ($I_B = I_C$). Equal currents occur when

$$\beta V_{EFF,1}^2 = \beta V_{EFF,2}^2 + I_u \times D \tag{1}$$

where $\beta = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}$ and $V_{EFF,1|2}$ is the effective gate overdrive of transistors $M_{1|2}$.[2] If $D = 0$ the currents are equal when the effective gate overdrives are equal, which occurs when the inputs are equal. If $D > 0$ the currents are equal when the effective overdrive of M_1 is larger than the effective overdrive of M_2, which occurs when $V_{IN} > V_{IP}$.

The nominal delay of the comparator (including Schmitt trigger and logic gates) is $t_c = 0.5$ ns. With the 6-bit DAC the effective delay of the comparator can be controlled from $t_c = -0.9$ to $t_c = 0.5$ ns.

4.3 Bootstrapped switches

The input switches in the first stage of a pipelined converter feel the full force of a sinusoidal input signal, which means that the voltage dependent switch resistance affects the linearity of the converter. To ensure high linearity the switch resistance must be low, but in nano-scale technologies the difference between the power supply and the sum of the threshold voltages is low (around $1.2\text{ V} - 2 \times 0.5\text{ V} = 0.2\text{ V}$ for an low-power 90 nm CMOS technology, compared to around $1.8\text{ V} - 2 \times 0.5\text{ V} = 0.8\text{ V}$ in an 0.18 µm CMOS technology), so the overdrive of a transmission-gate is low, and the resistance high when the input signal is mid-rail. A transmission gate becomes prohibitively large at sufficiently low resistance. To reduce the switch size we can use a constant overdrive (constant $V_{gs} - V_{th} = V_{eff}$), and to achieve a constant overdrive we can use bootstrapped switches. There are two basic types of bootstrapped switches, continuous time bootstrapped switches and switched-capacitor bootstrapped switches. Examples of the switched capacitor kind can be seen in [11]. We've used a type of continuous time bootstrapped

[2] Here we assume a square law model for the transistors, and that the transistors are in strong inversion and saturation

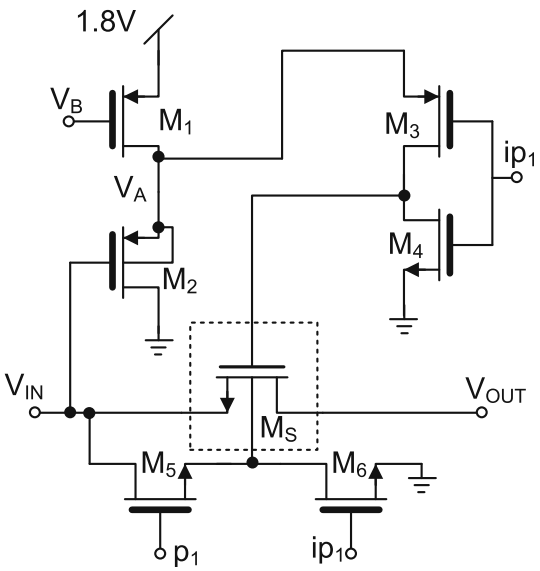

Fig. 7 Continuous time bootstrapped switch. The transistors with thick gates are thick oxide devices. The switch transistor (M_S) is a thin oxide, low threshold voltage, device

switches [12]. In our implementation a source follower tracks the input signal, and the gate-source voltage of the source follower sets the gate-source voltage of the switch. Figure 7 shows the continuous time bootstrapped switch. We've modified the switch from [12] by adding M_3. Without M_3 the source of M_2 is reset to zero when we turn off the switch, and thus has to slew when we turn the switch on. By turning off the switch with M_3 and M_4 we get a faster turn-on time, because the source of M_2 is no longer reset to zero. To avoid reliability problems we've used thick oxide transistors in the switch. If we were to use standard oxide transistors the V_{DS} of M_3, M_4 and M_2 would be too large. At high V_{DS} the transistors can be damaged by hot-carrier injection [13]. Using thick oxide transistors removed this challenge, but for the switch transistor we've used a low-threshold thin oxide device to reduce the switch resistance. To reduce the switch resistance even more we connect the bulk to the source when the switch is on, removing the body effect. When the switch is off M_6 shorts

the bulk to ground to avoid forward biasing the bulk-drain PN junction.

4.4 Sub analog-to-digital converter

The stage sub analog-to-digital converter (SADC) used dynamic comparators. The comparators in the SADC can have large offsets (up to ± 100 mV in our implementation), because the pipelined architecture can correct the offset [14]. Since we can have large offsets we used a dynamic comparator referred to as a resistive divider [15].

5 Test setup and calibration

A custom PCB was made to test the ADC. The ADC needed a clock signal, an input signal, digital control signals, and references. The test setup can be seen in Fig. 8. We used two Rode & Schwarz SML03 signal sources for the clock signal and high frequency input signal. To remove signal source harmonics we used fifth-order passive filters. The input signal was fed through a DC block capacitor, a 10 nH inductor and a RF transformer (Mini-Circuits ADT1-1WT) to do single ended to differential conversion. The common mode was set at VDD/2 with a resistor ladder. The resistors and capacitors before the ADC input form a low pass filter, with a cut off of around 40 MHz. To get fast clock edges a high speed comparator (MAX 961U) was used for sinusoid to square wave conversion. To power the chip we used low-dropout CMOS regulators (ADP1715), one regulator for each of the power domains. The PCB has five power domains, one analog 1.2 V supply, an analog 1.8 V supply, a 1.2 V digital supply for on-chip buffers, a 1.2 V digital supply for on-board output buffers, and a 3.3 V supply for clock generation and optocouplers.

One of the major limitations in the current ADC and PCB design is excessive coupling of noise from digital outputs. The on-chip CMOS IO buffers are fed directly from the internal SADCs. The outputs, running at 60 MS/s, change value each half period, which generates significant on-board noise. Since the references for the ADC are on-board, and not on-chip they have limited noise immunity, and thus the ENOB suffers. To reduce the noise injection we reduced power supply of the digital buffers (on-board, and on-chip) to 0.85 V, this limited our speed to 60 MS/s, but allowed us to get an ENOB of 7.05-bit.

To calibrate the ADC we shift in a 272-bit calibration string. Each pipelined stage has 6-bits for the comparator, 8-bits per current source, 2-bits for additional current in

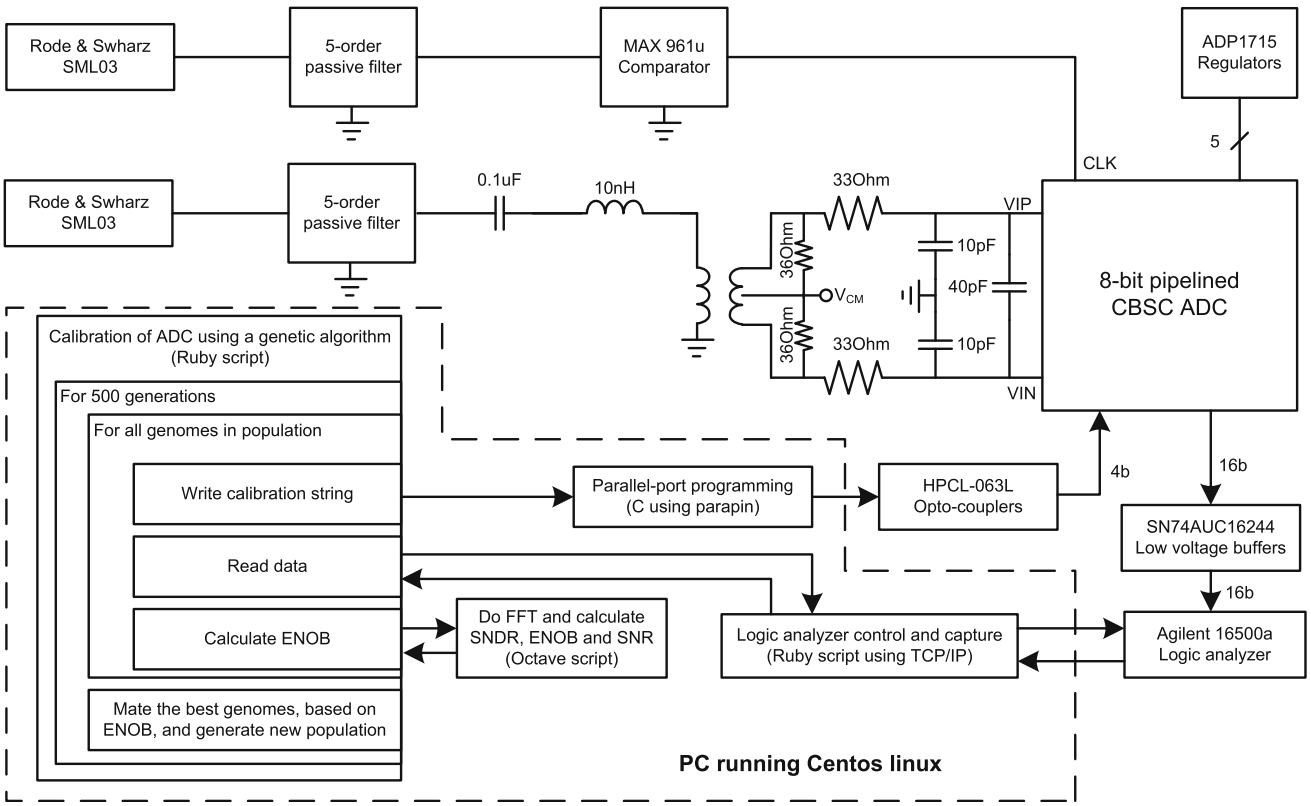

Fig. 8 ADC test setup

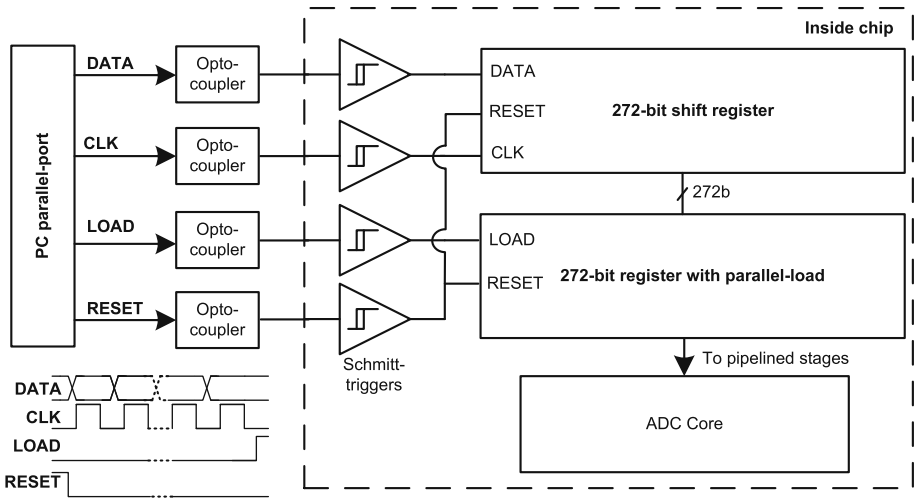

Fig. 9 The ADC calibration string serial interface. The calibration string is shifted into a 272-bit register, and when the shift is complete the calibration string is loaded in parallel into a second register that is connected to the calibration lines for each stage

current source gain boosters, and 8-bits to control an in-stage analog test-mux, in total 32-bits per stage. There are 8-stages of 32-bits and a 16-bit string to control test-muxes, in total 272-bits. In the ADC we only use seven of the pipelined stages, so for calibration 154-bits are used. The calibration string is prepared in a Ruby script and passed to a C-program that writes the bits to the ADC with the PC parallel port (using the parapin library [16]) through optocouplers (HCPL-260L) into the serial interface of the ADC, shown in Fig. 9.

The output of the ADC (2-bits per stage times 7-stages + 1.5-bit flash = 16-bits) were buffered by low voltage buffers (SN74AUC16244) and captured by an Agilent 16500a logic analyzer. The data was read via an Ethernet connection to a PC, and post-processed there.

5.1 Calibration of ADC

The calibration algorithm described here is not suitable, nor is it intended, for a commercial ADC, it is too slow. The calibration algorithm is only suitable for lab testing to prove that there is a calibration setting that compensates for the comparator delay. We did not focus on implementing an efficient algorithm, our plan was to make the comparator and current sources digitally controllable, and prove that there is a calibration setting that can compensate for the comparator delay.

To find a suitable calibration string we used an algorithm inspired by evolution. The algorithm belongs to a class of algorithms often referred to as a "genetic algorithms" [17]. We start by generating 30 calibration strings (individuals) , which make up our first population. The initial population was based on a solution found by hand tuning. Each of the individuals were tested in the ADC, and the effective number of bits (ENOB) was calculated. During this test the ADC had an input signal of 29.4 MHz. Each of the individuals in the population were ranked according to their ENOB. The two best individuals were transferred to the new population directly. The rest of the new population was filled by mating the best individuals from the previous population. Each individual undergoes mutation after mating, and the site of mutation is random (for example bit one of the six-bit comparator string in pipelined stage four switches from 0 to 1). Mutation ensures that the algorithm does not get stuck with similar individuals in the whole population. For each new population (generation) we repeat the process, and this goes on for five hundred generations (roughly 15,000 calibration strings tested), which takes around 7 h. As time progresses each generation improves, and the population converges towards a solution. An example of a calibration run can be seen in Fig. 10. The starting point for the calibration was a hand calibrated ENOB of 5.8-bit. The best solution gave an ENOB of 7.05-bit at 60 MS/s. The best calibration string was used for all measurements in the next section.

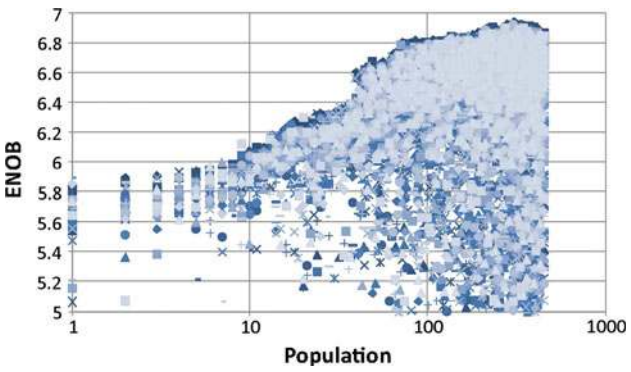

Fig. 10 Evolution of the ENOB for a calibration run, initial solution was 5.8-bit ENOB

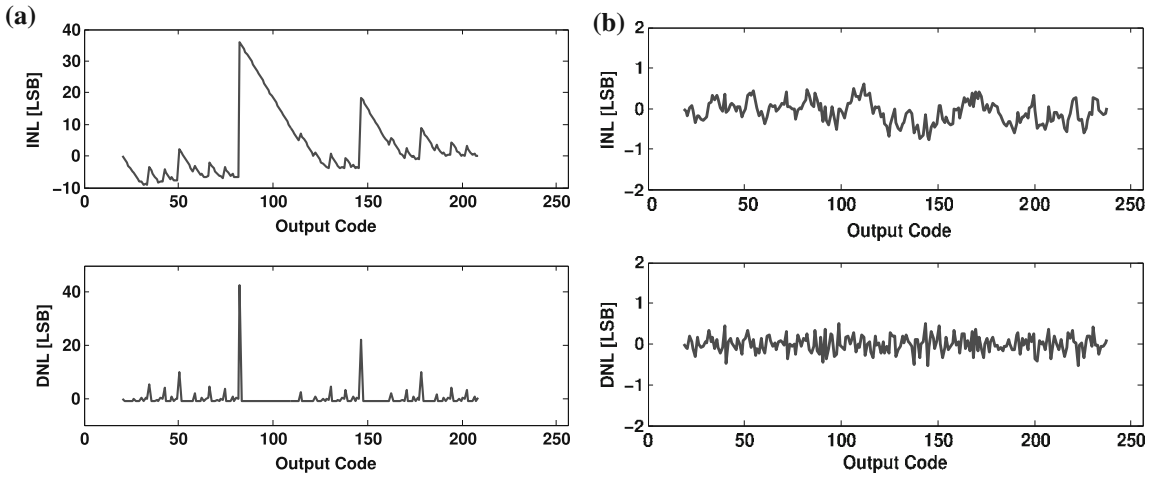

Fig. 11 INL and DNL for uncalibrated, and calibrated ADC. **a** No calibration, default values set before production. **b** After calibration of comparator offset and current source current

Table 1 Summary of calibrated ADC performance

Technology	1.2 V/1.8 V 90 nm CMOS
Sampling frequency	60 MS/s
Resolution	8 bits
Full scale input	0.8 V
Area	0.85 mm × 0.35 mm
DNL (LSB)	0.52/−0.54
INL (LSB)	0.6/−0.77
SNR (29.4 MHz input)	44.5 dB
SNDR (29.4 MHz input)	44.2 dB
SFDR (29.4 MHz input)	60 dB
ADC core power	5.9 mW
Clock power	2.3 mW
Input switches (1.8 V)	0.3 mW

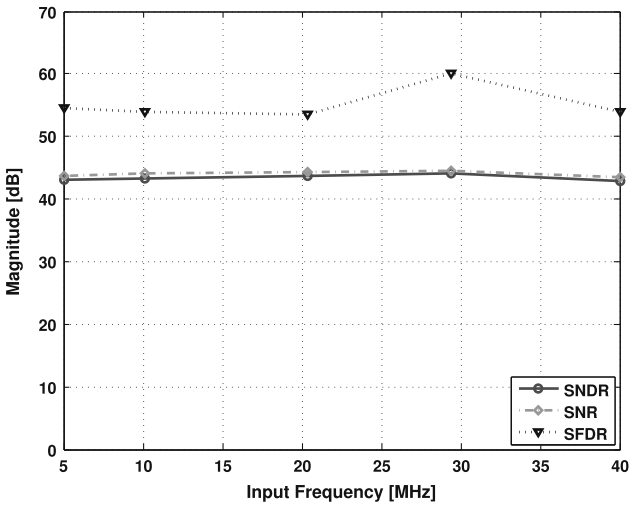

Fig. 12 SNDR, SNR and SFDR versus frequency, sampling frequency is 60 MS/s

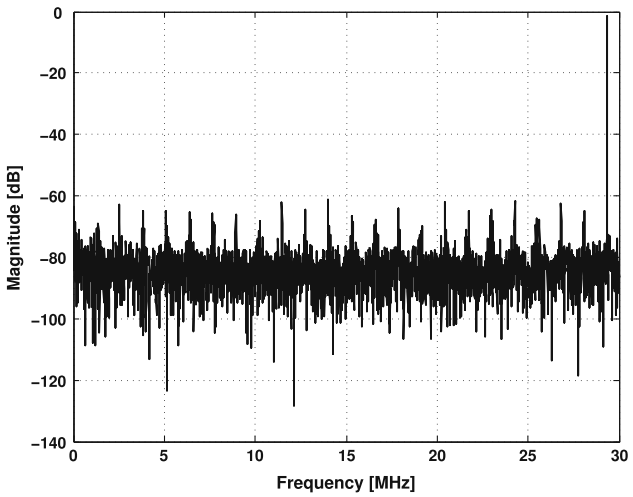

Fig. 13 A 8192 point FFT of the ADC output

6 Measurement results

The essence of this paper is the digitally controlled comparator threshold that compensates for the comparator delay. The development of an efficient calibration algorithm has been left for future research.

The default comparator threshold and current source current set before production caused an excessive overshoot, as a result the maximum integral non-linearity (INL) is 36 LSB (seen in Fig. 11(a)), and the ADC has an ENOB of 2.5-bit. After calibration, with optimal comparator threshold and current source current the ADC has an ENOB of 7.05-bit and a maximum INL of 0.7 LSB. This demonstrates that the variations caused by processing can be canceled by digitally adjusting the threshold of the comparator.

A summary of the ADC performance is shown in Table 1. It achieves a *signal-to-noise and distortion ratio* (SNDR) of 44.2-dB (7.05-bit) with a sampling frequency

Table 2 Comparison to state-of-the-art

Process (nm)	Power (mW)	ENOB @ Nyquist bits	Sampling rate (MS/s)	Thermal FOM (fJ/step)	Walden FOM (pJ/step)	Architecture	Reference
90	70	6.56	770	10.1	0.96	Sub-ranging	[20]
90	34	7.0?	300	6.9	0.89	Sub-ranging	[19]
90	2.6	6.85	10	19.5	2.17	Pipelined	[21]
130	21	7.60	125	4.5	0.86	Sub-ranging	[22]
180	30	7.68	200	3.5	0.73	Pipelined	[23]
180	8.5	6.40	200	6.0	0.5	Pipelined	[5]
90	8.5	7.05	60	8.1	1.07	Pipelined	This work

(f_s) of 60 MS/s, an input signal of $f_s/2$, and a power dissipation of 8.5 mW (5.9 mW for ADC core, 2.3 mW for clock generation and distribution, and 0.3 mW for input switches). An input signal amplitude of −1 dBFS was used during measurement. The ADC has a *spurious free dynamic range* (SFDR) of 60-dB. The SNDR and SNR change little with input frequency, and the effective resolution bandwidth extend well beyond $f_s/2$ (as seen in Fig. 12).

A 8192 point FFT of the ADC output is shown in Fig. 13. Coherent sampling and a Hanning window was used to avoid spectral leakage.

6.1 Comparison to state-of-the-art

A comparison of our converter to other 8-bit ADCs with sample rate above 1 MS/s is shown in Table 2. One of the figure of merits used is the Thermal FOM [13], which can be calculated from the equation

$$\text{FOM} = \frac{\text{Power dissipation}}{2^{2\times\text{ENOB}} \times \text{Sampling frequency}}, \quad (2)$$

which differs from the more conventional Walden FOM of

$$\text{FOM} = \frac{\text{Power dissipation}}{2^{\text{ENOB}} \times \text{Sampling frequency}}. \quad (3)$$

The Thermal FOM is more correct when comparing ADCs with different ENOB [18].

From the Thermal FOM in Table 2 we can see that the performance of our converter is good compared to other 8-bit converters in 90 nm, only beaten by [19].

7 Conclusion

We presented a differential comparator-based switched-capacitor (CBSC) pipelined ADC with comparator preset, and comparator delay compensation. Compensating for the comparator delay by digitally adjusting the comparator threshold improves the ADC resolution from 2.5-bit to 7.05-bit. The ADC was manufactured in a 90 nm CMOS technology, with a core area of 0.85 mm × 0.35 mm, a 1.2 V supply for the core and 1.8 V for the input switches. It has an ENOB of 7.05-bit, and a power dissipation of 8.5 mW at 60 MS/s.

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Carsten Wulff received the M.Sc. and Ph.D. degrees in Electrical Engineering from the Department of Electronics and Telecommunication, Norwegian University of Science and Technology (NTNU), in 2002 and 2008, respectively. During his Ph.D. work at NTNU, he worked on open-loop sigma-delta modulators and analog-to- digital converters in nanoscale CMOS technologies. In 2006–2007, he was a Visiting Researcher with the Department of Electrical and Computer Engineering, University of Toronto, Toronto, ON, Canada. He is currently a Research and Development Engineer with Nordic Semiconductor ASA, Trondheim, Norway. His present research interests includes analog and mixed-signal CMOS design and design of high-efficiency analog-to-digital converters.

Trond Ytterdal received the M.Sc. and Ph.D. degrees in Electrical Engineering from the Norwegian Institute of Technology in 1990 and 1995, respectively. He was a Research Associate with the Department of Electrical Engineering, University of Virginia (1995–1996), and as a Research scientist with the Electrical, Computer and Systems Engineering Department, Rensselaer Polytechnic Institute, Troy, NY (1996–1997). From 1997 to 2001, he was a Senior ASIC Designer with Nordic Semiconductor, Trondheim, Norway. In 2001, he became a Professor at the Department of Electronics and Telecommunication, Norwegian University of Science and Technology (NTNU). His present research interests include design of analog integrated circuits, behavioral modeling and simulation of mixed-signal systems, modeling of nanoscale transistors, and novel device structures for application in circuit simulators. He has published more than 130 scientific papers in international journals and conference proceedings. He is a Coauthor of Semiconductor Device Modeling for VLSI (Englewood Cliffs, NJ: Prentice-Hall, 1993), Introduction to Device Modeling and Circuit Simulation (New York: Wiley, 1998), and Device Modeling for Analog and RF CMOS Circuit Design (New York: Wiley, 2003) and has contributed to several other books published internationally. He is also a Codeveloper of the circuit simulator AIM-Spice. Prof. Ytterdal is a member of The Norwegian Academy of Technological Sciences.