# Comparison Between CCM Single-Stage And Two-Stage Boost PFC Converters*

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## ABSTRACT

**In this paper, the analysis of the major-component ratings of the continuous current mode (CCM) single-stage power-factor-correction (PFC) and the CCM boost two-stage PFC converters is given. The results of the analysis are summarized in a number of design plots generated for different output power levels. Finally, merits and limitations of these two approaches are discussed.**

## 1. INTRODUCTION

Conventional off-line power converters with diode-capacitor rectifier front-end have distorted input current waveform with high harmonic content. Typically, these converters have a power factor lower than 0.65. As a result, they cannot meet neither the European line-current harmonic regulations defined in the IEC 1000-3-2 document nor the corresponding Japanese input-harmonic current specifications. To comply with these standards, input power-factor correction (PFC) of off-line power supplies has to be introduced. So far, a variety of passive and active PFC techniques have been proposed. While the passive techniques may be the best choice in many low-power, cost-sensitive applications, the active PFC techniques are used in the majority of applications due to their superior performance [1].

The active PFC converters can be implemented using either the two-stage approach or the single-stage approach. The two-stage approach is the most commonly used approach [2]. In this approach, an active PFC stage is employed as the front-end to force the line current to track the line voltage. Additionally, the PFC stage establishes a loosely regulated high-voltage dc bus at its output, which serves as the input voltage to a conventional dc/dc stage with a tightly regulated output voltage. While the two-stage approach is a cost-effective approach in high-power applications, its cost-effectiveness is diminished in low-power applications due to the additional PFC power stage and control circuit. A low cost alternative solution to this problem is to integrate the active PFC input-stage with the isolated dc/dc output stage. A number of active single-stage PFC techniques have been introduced in recent years [3[-[7]. In all of these approaches, the PFC switch and controller are saved. However, unlike in the two-stage approach, the dc voltage on the energy-storage capacitor in a single-stage PFC converter is not regulated. As a result, in universal-line applications (90 – 265 Vac), the energy-storage-capacitor voltage varies with the load and line. This increases the ratings, size, and cost of the components, and it also reduces the overall efficiency.

In this paper, a detailed comparison study between the CCM single-stage PFC converter and the CCM boost two-stage PFC converter for universal-line applications with the hold-up time requirement is presented. The merits and limitations of these two approaches are also discussed.

## 2. REVIEW OF TWO PFC APPROACHES

### *1.1 Two-stage Approach*

The generalized structure of the two-stage PFC converters is shown in Fig. 1. In this approach, there are two independent power stages. The front-end PFC stage is usually a boost or buck/boost (or flyback) converter. The boost converter front-end consists of a boost inductor, boost switch, and rectifier. The PFC controller senses the line voltage waveform and forces the input current to track the line voltage to achieve the unit input power factor. Since the voltage of energy-storage bulk capacitor $C_B$, $V_B$, is loosely regulated, $V_B$ is a dc voltage which contains a small second order harmonic. This bus voltage is typically regulated at around 380 Vdc in the entire line input voltage range from 90 Vac to 265 Vac. The high bus voltage $V_B$ minimizes the bulk capacitor value for a given hold-up time. In addition, the narrow-range-varying $V_B$ improves the efficiency of an optimized dc/dc output stage. The dc/dc output stage is the isolated output stage that is implemented with at least one switch, which is controlled by an independent PWM controller to tightly regulate the output voltage.

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Figure 2(a) shows the input current and voltage waveforms of a two-stage PFC converter, whereas Fig. 2(b) shows the duty-cycle variations of the front-end PFC stage and the dc/dc output stage during a rectified-line cycle. Since the input and output voltage of the dc/dc converter are constant, the duty cycle of the dc/dc converter, $d_{dc/dc}$, is also constant, as shown in Fig.2 (b).

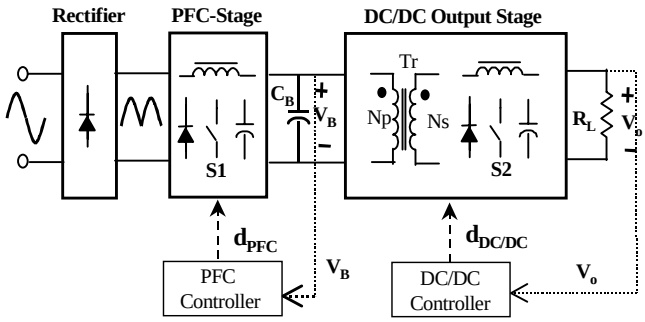


Fig. 1 Conceptual structure of two-stage PFC converter.

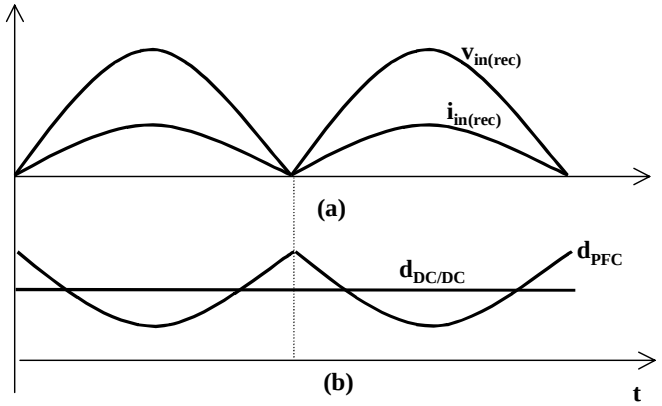


Fig. 2 Ideal waveforms of the two-stage PFC converter:
(a) rectified input voltage and current;
(b) duty cycle of the PFC and DC/DC switches.

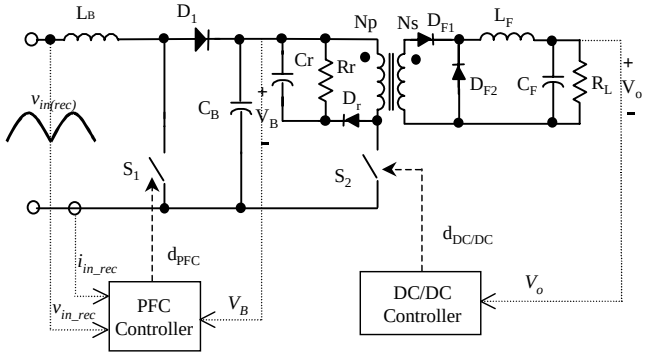


Fig. 3 CCM boost PFC front-end with forward output stage.

Figure 3 shows the circuit diagram of the two-stage PFC converters consisting of a CCM boost PFC converter as the front-end stage and a forward converter as the dc/dc output stage.

### *2.2 Single-Stage Approach*

The conceptual structure of the single-stage PFC converter is shown in Fig. 4. Compared to the two-stage approach, the single-stage approach uses only one switch and controller to shape the input current and to regulate the output voltage. The controller is used for a fast regulation of the output voltage. As a result, when the converter in Fig. 3 works in a steady state, the switch duty-cycle is almost constant during a line cycle. With a constant duty cycle, the boost inductor provides a natural PFC of the input current. Although for a single-stage PFC converter attenuation of input-current harmonics is not as good as for the two-stage approach, it is good enough to meet the IEC 1000-3-2 requirements.

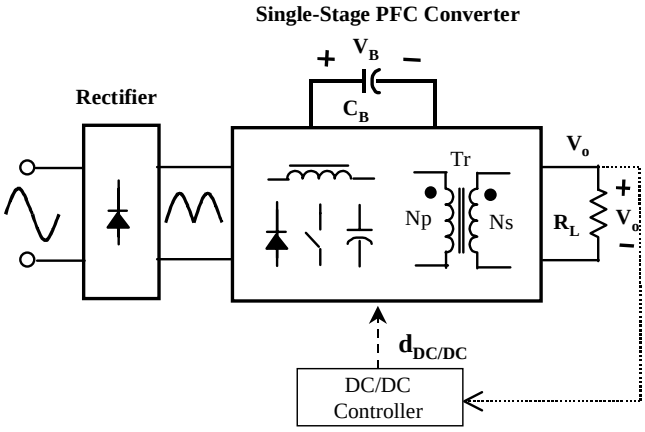


Fig. 4 Conceptual structure of single-stage PFC converter.

Generally, for any PFC converter, the instantaneous input power during a line cycle is pulsating, while the output power is constant. Therefore, in any PFC circuit, there must be an energy-storage capacitor to store the unbalanced energy. However, in a single-stage PFC converter, unlike in a two-stage PFC converter, energy-storage-capacitor voltage $V_B$ is no longer loosely regulated at a constant value because the controller is used to regulate the output voltage, not $V_B$. As a result, in the single-stage PFC converters, $V_B$ varies with the line voltage. For universal line input (90 Vac – 265 Vac), $V_B$ is typically around 130 V at the low line and higher than 400 V at the high line [3]-[7]. The wide voltage range has detrimental effect on the conversion efficiency, and it requires an energy-storage capacitor with a large capacitance and high voltage rating (>400 Vdc) to meet the hold-up time requirement. Since the cost and size of an electrolytic capacitor increase with its capacitance, there is a strong trade-off between the cost and size savings brought about by using a single switch and controller and the increased cost and size of a larger capacitor. As a result, in universal-line application with a hold-up time requirement, the single-stage

PFC approach may not be more cost effective than the conventional two-stage approach.

According to the continuity of the input inductor current, the single-stage PFC converters can be classified into DCM and CCM converters. Typically, the DCM single-stage PFC converters are simpler than their CCM counterparts. As a result, the DCM implementations have a lower cost, but they require a larger input EMI filter and have lower efficiency due to higher current stresses. Thus the DCM implementations are usually only suitable for low power applications. The comparisons carried out in this paper have been performed on CCM single-stage PFC converters.

Figure 5 shows the circuit diagram of a single-stage PFC converter with forward output [4]. This converter uses an additional inductor $L_1$ to achieve the CCM operation. In the circuit in Fig. 5, an active clamped (ACL) reset circuit [8] is employed to achieve a maximum duty cycle of the switch so that energy-storage-capacitor voltage $V_B$ is minimized.

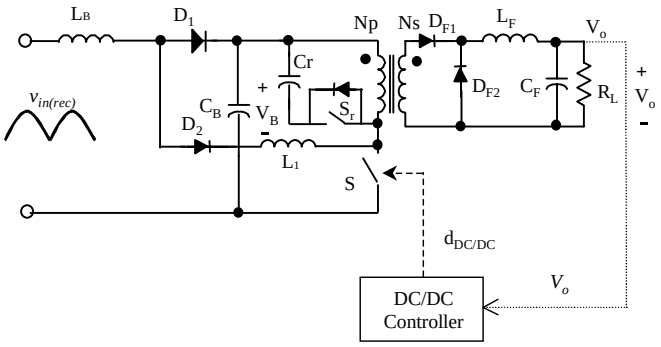


Fig. 5 CCM single-stage PFC converter with forward output stage.

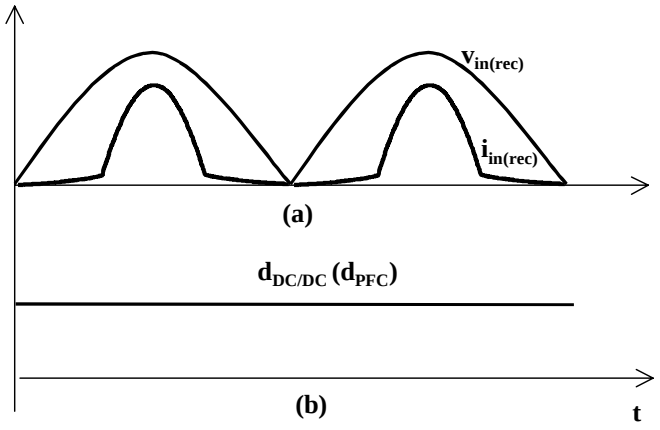


Fig. 6 Waveforms of the single-stage PFC converter:
(a) rectified input voltage and current;
(b) duty cycle of the integrated switch S.

Figure 6 shows typical input voltage and current waveform of a single-stage PFC circuit. Although, the input current is not sinusoidal, it meets the IEC 1000-3-2 PFC requirement. The duty cycle of the switch in a single-switch PFC converter is constant during a line cycle.

## 2. COMPARISON OF TWO PFC APPROACHES

The comparison of the two-stage and single-stage PFC approaches was performed under the following assumptions:

- Input voltage is universal line voltage from 90 Vac to 265 Vac.
- Output voltage is 5Vdc, and output power levels are 50 W, 100 W, 200 W, 300 W and 400 W, respectively.
- Hold-up time is also a requirement.
- The switching frequency was assumed to be 100 kHz for both the PFC switch and the switch in the dc/dc power stage. Also, it was assumed high frequency MOSFET devices were used for all the switches.
- In the two-stage PFC converter, the PFC stage efficiency $\eta_{PFC}$ of 0.9 was assumed, whereas the dc/dc stage efficiency $\eta_{DC}$ of 0.8 is assumed, for an overall efficiency $\eta$ of around 0.72. For the single-stage PFC converter, it was assumed that the overall efficiency $\eta$ is about 0.7.
- It was also assumed that, in the two-stage PFC converter, the energy-storage-capacitor voltage is regulated at 400 Vdc. The energy-storage-capacitor voltage of single-stage PFC is in the 130-400 Vdc range for the line voltage variation from 90 Vac to 265 Vac.

### *3.1. Comparison of Bulk Capacitors*

In a majority of computer-related applications a hold-up time is a very important requirement. Generally, the hold-up time is the time during which a power supply needs to maintain its output voltages within the specified range after a dropout of the line voltage. This time is used to orderly terminate the operation of a computer or to switch over to the UPS operation after a line failure. For example, the majority of today's desktop computers and computer peripherals require power supplies that are capable of operating in the 90-270 Vac range and can provide a hold-up time of at least 10 ms. The required energy to support the output during the hold-up time is obtained from a properly sized energy-storage capacitor $C_B$. The rating of the hold-up capacitor significantly impacts the total size and cost of power supply. Generally, capacitance $C_B$ is determined by Eq. (1), where $V_{B(90)}$ is the low line full-load capacitor voltage, and $V_{B(min)}$ is the minimum designed capacitor voltage. $P_{o(max)}$ is the maximum output power, $t_{hold}$ is the hold-up time, and $\eta_{dc}$ is the forward stage efficiency.

$$C_B = \frac{2 \cdot \frac{P_{o\_\max}}{\eta_{dc}} \cdot t_{hold}}{V_{B\_90}^2 - V_{B\_\min}^2} \quad (1)$$

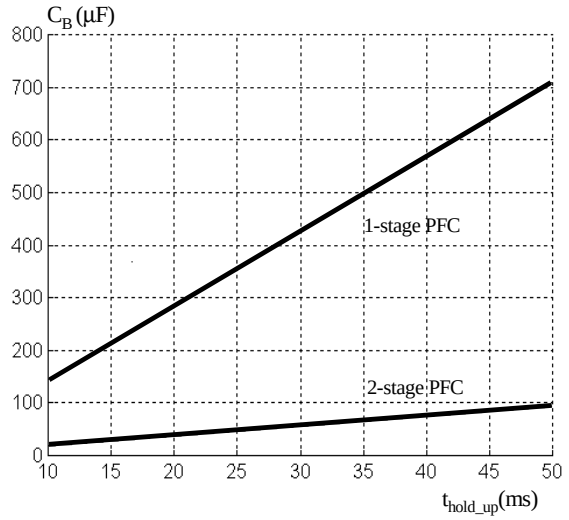


Fig. 7 Energy-storage-capacitance $C_B$ vs. hold-up time for Po=100W.

If, for a two-stage PFC power supply, the bus voltage $V_{B(90)}$ is regulated at 400 V and the minimum voltage $V_{B(min)}$ =300 V is selected, a relatively small bulk capacitor is required. For example, for $t_{hold}$=10 ms, $P_{o(max)}$=100 W, $C_B$ is only 37.8 μF based on the calculation. However, for a single-stage PFC, the low line bus voltage is not regulated, but typically it is around 130 V when the input line voltage is 90 Vac. Therefore, if $V_{B(min)}$ is selected at 90 V, $C_B$ must be at least as high as 284 μF to maintain the same hold-up time. This capacitance value is seven times larger than the corresponding two-stage PFC capacitor value. Figure 7 shows the relationship between $C_B$ and hold-up time $t_{hold}$ for the output power of 100 W for two different PFC approaches. As can be seen in Fig. 7, the single-stage PFC converter requires much larger hold-up capacitance than the two-stage PFC converter does. In both cases, the capacitor voltage rating is 450 Vdc. Figures 8(a) and 8(b) show the dependence of $C_B$ as a function of output power $P_{O(max)}$ for the two-stage and single-stage PFC converters, respectively. As can be seen in Fig. 8(a) and 8(b), the single-stage PFC requires a larger capacitance than the two-stage PFC converter for all power levels. In addition, for both converters, the capacitance always increases as the hold-up time increases.

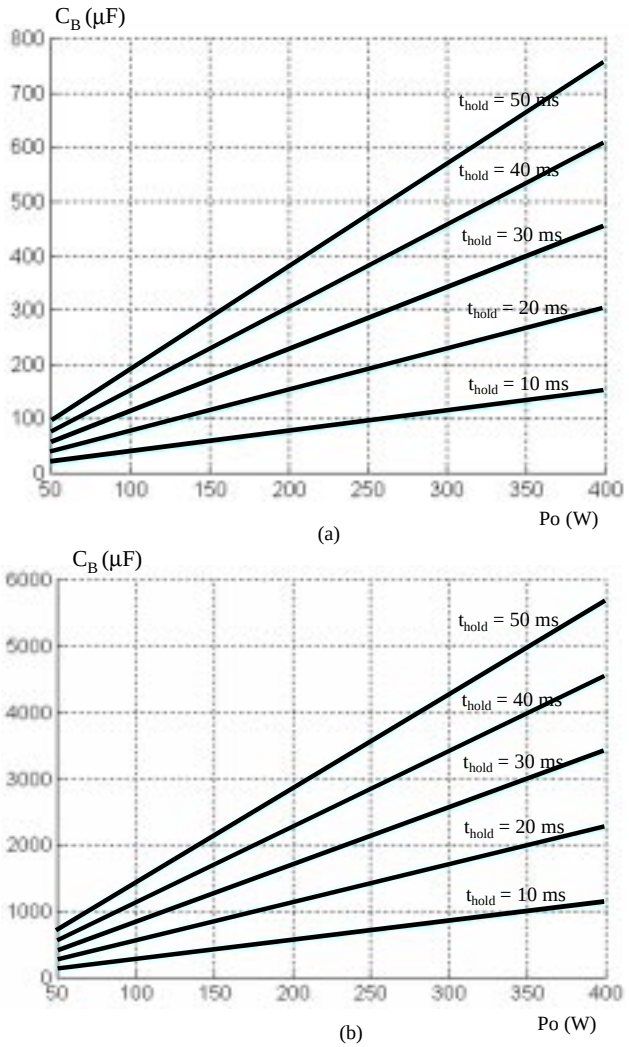


Fig. 8 Energy-storage-capacitor size $C_B$ vs. output power $P_O$ for different hold-up time $t_{hold}$ requirements:
(a) two-stage PFC;
(b) single-stage PFC.

### *3.2 Comparison of semiconductors*

In the two-stage PFC converter, the PFC switch handles the PFC current, whereas the switch in dc/dc converter handles the dc/dc converter's current. The single-stage PFC converter combines these two switches into one, thus saving a switch. However, the combined single switch handles both the PFC current and the dc/dc stage current so it is subjected to a higher current stress. In addition, since at low input line the energy-storage-capacitor voltage in a single-stage PFC converter is much lower than the corresponding voltage in a two-stage PFC converter, the switch current in the single-stage PFC converter is higher than the switch current in the two-stage PFC converter with the same output power. The current through the switch determines the size of the switch and the loss on the switch.

Generally, the rms current of the PFC switch in the two-stage PFC converter is given by Eq. (3).

$$I_{in\_pk} = \sqrt{2} \cdot \frac{P_{o\max}/\eta}{V_{in\_\min}} \tag{2}$$

$$I_{S1} = \sqrt{\int_0^{\pi} (1 - \frac{\sqrt{2} \cdot V_{in\_\min}}{V_B} \cdot \sin(x)) \cdot I_{in\_pk}^2 \cdot \sin(x)^2 dx} \tag{3}$$

The switch current $I_{S2}$ of the forward dc/dc converter can be calculated by Eq. (4).

$$I_{s2} = \frac{P_{o\max}/V_o}{N} \cdot \sqrt{D_{FWD}} \tag{4}$$

Where N is the turns ratio of the forward transformer, and $D_{FWD}$ is the duty-cycle.

For a single-stage PFC converter, the input current cannot be expressed by a close-form equation because the input current has an irregular waveform. Therefore, the rms current of the switch in a single-stage PFC converter, $I_{S(rms)}$, has to be obtained by simulations.

Figure 9 shows the comparison of the current ratings between the two-stage PFC converter and the single-stage PFC converter. It shows that the rms switch current in the single-stage PFC is higher than the sum of the currents of both switches in the two-stage PFC converter. Therefore, the single-stage PFC implementation requires a larger switch compared to the switches in the two-stage PFC converters. In fact, to achieve the same efficiency, the single-stage PFC approach requires more silicon than the two-stage PFC approach.

Figure10 shows the comparison of the average current of the boost rectifiers. As can be seen, the single-stage PFC converter has a higher rectifier current than the two-stage PFC converter at all power levels. The rectifier voltage stress in both cases is 400 Vdc, *i.e.*, it is equal to output voltage $V_O$.

Finally, Fig. 11 shows the average current of the forward output rectifiers as a function of the output power. As can be seen, the single-stage PFC converter also has a higher current through the output rectifiers than the two-stage PFC converter. At the same time, the voltage stress on the output rectifier in the single-stage PFC converter is higher than the voltage stress in the two-stage circuit For the 5 V output, the reverse voltage on the output (secondary side) rectifiers is 35 V, whereas the corresponding voltage in the two-stage PFC converter is only 12 V. Because of the higher reverse voltage on the output rectifiers, the power loss in the output rectifiers in the single-stage PFC converter is larger than in the two-stage PFC converter.

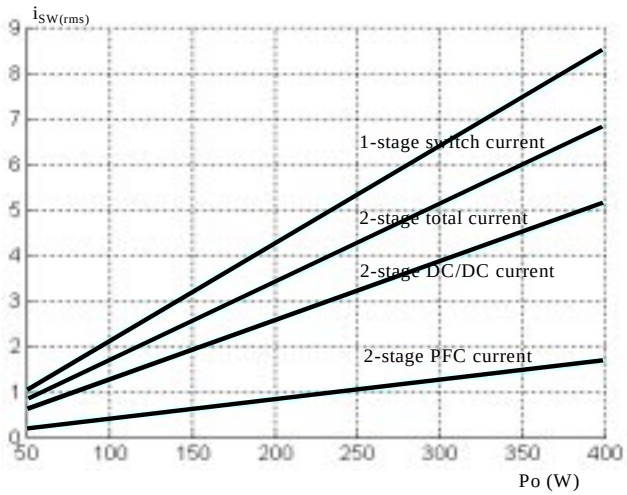


Fig. 9 Switch rms current vs. output power.

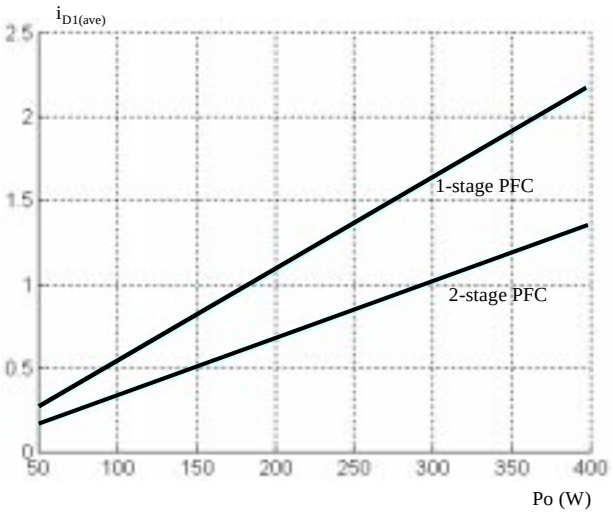


Fig. 10 Boost rectifier average current vs. output power.

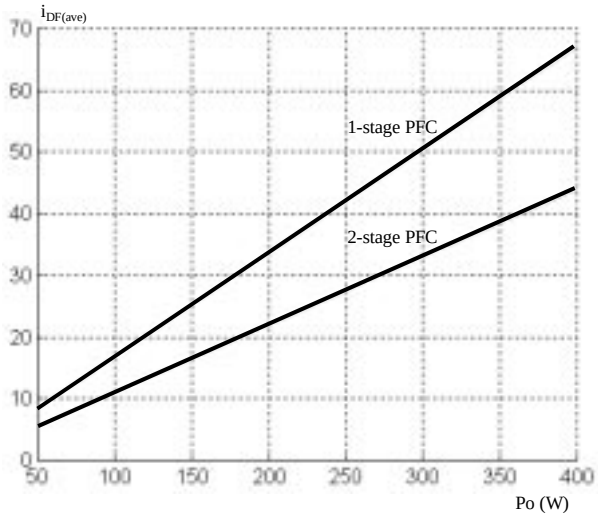


Fig. 11 Output rectifier average current vs. output power.

In summary, although the single-stage PFC converter saves one PFC switch, the current ratings of all the switches and rectifiers in the single-stage PFC converter are higher than in the two-stage PFC converters, which adversely affects the cost and efficiency of the single-stage PFC.

### *3.3 Comparison of inductors*

#### a) *PFC Inductor*

The input inductance in the two-stage PFC converter is determined by the maximum ripple and PFC duty cycle [2]. However, in the design of a single-stage PFC converter, the inductor current ripple is not the major concern [3]. In fact, the bus voltage stress, the input-current power factor, and the overall efficiency are more important design concerns than the current ripple. Therefore, in the following comparisons, it is assumed that the PFC inductors in the single-stage and two-stage circuits have the same inductance. Despite having the same PFC inductances, the input-inductor peak currents in these two implementations are different.

Figure 12 shows the comparison of the peak input-inductor currents. As can be seen from Fig. 12, the single-stage PFC converter has a higher peak inductor current than the two-stage PFC converter.

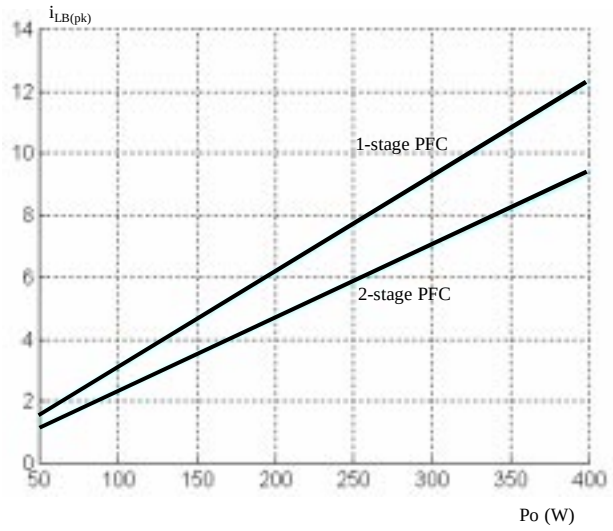


Fig. 12 Input-inductor peak current vs. output power.

#### *b). Output filter inductor rating*

To compare the output inductors, it was assumed that the inductor-current ripples are the same; i.e., the peak currents through the output filter inductors in both cases are the same. However, because the energy-storage-capacitor voltage $V_B$ varies in a wide range in the single-stage PFC converter, the switch duty cycle changes with the line changes. As a result, the single-stage PFC converter requires a larger output inductance than the two-stage PFC converter, as shown in Fig. 13.

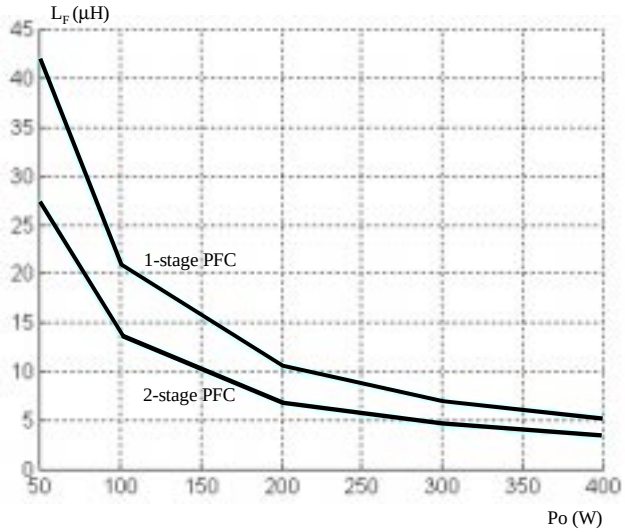


Fig. 13 Output-filter inductor vs. output power.

Finally, Table 1 summarizes the comparison results between the single-stage and two-stage converter at $P_O$=100 W and $t_{hold}$= 10 ms.

Table 1.

Comparison between two-stage and single-stage PFC converters at $P_O$=100 W (5V/20A) and for $t_{hold}$=10 ms.

| | Two-Stage PFC | 1-Stage PFC |
|---|---|---|
| Reset Circuit | RCD Clamp Reset | Active Clamp Reset |
| Forward Switch Duty Cycle | $D_{oper}$ = 0.45<br>$D_{max}$ =0.60 | $D_{90V}$ = 0.49<br>$D_{265V}$ = 0.16<br>$D_{max}$ = 0.7 |
| Input inductor peak current | 2.34 A | 3.08 A |
| Bus voltage | Vmin = 300 V<br>Voper = 400 V | Vmin = 90 V<br>Voper = 130-400 V |
| Forward Trans. Turns Ratio | 32.5 | 11.5 |
| PFC Switch Rating | 1.287 A / 400 V | NA |
| PFC Diode Rating | 0.339 A / 400 V | 0.544 A/ 400 V |
| Forward Switch Rating | 0.42 A/ 727 V | 2.134 A/ 574 V |
| Output diode rating | 11.0 A / 12 V | 16.8 A/ 34.9 V |
| Bus Capacitor | 37.8 uF / 450 V | 284 uF / 450 V |
| Output Inductor | 13.7 uH / 22 A | 21.0 uH / 22 A |

According to the above comparisons, the following general conclusion can be obtained:

- Because, for universal-line applications, the single stage PFC converter exhibits a wide variation of the energy-storage-capacitor voltage, it requires higher rating components compared to the two-stage PFC converter.
- The total loss in the single-stage PFC converter may be higher than in the two-stage PFC converter. Therefore, the efficiency of the single-stage PFC circuit may be lower than that of the two-stage PFC circuit.
- The single-stage PFC converter reduces the number of components by eliminating a need for the PFC switch and control circuit. However, because the single-stage PFC converter requires components with higher ratings, the single-stage approach may be attractive for applications at lower power levels (< 100 W) where the component rating difference is not significant. At lower power levels, the overall cost of the single-stage PFC converter still may be lower than that of the two-stage PFC converter. However, for higher power levels, the two-stage PFC approach is more attractive.

## 3. SUMMARY

In this paper, the two-stage PFC converter and single-stage PFC converter are reviewed, analyzed and compared. The comparison is done for different output power levels. The component values and their voltage and current ratings are given in a number of plots to illustrate the difference between these two PFC approaches.

Generally, the single-stage PFC converter has a simpler power stage and simpler control circuits. However, it requires higher-rated components and may exhibit a lower efficiency compared with the two-stage PFC converter. Nevertheless, for lower-power, cost-sensitive applications, the single-stage PFC approach may be more attractive. For higher-power applications, the two-stage PFC approach is the best choice.

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