Comparison of Current Limiting Strategies During Fault Ride-through of Inverters to Prevent Latch-up and Wind-up

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***Abstract*—Transient stability of a power network requires that generators remain synchronized and return to normal power export once a fault is cleared. For inverter-interfaced generators, one must ensure that current and voltage limiters do not latch-up and that controller integrators do not wind-up. A comparison of current-limiting strategies during fault ride-through of inverters to prevent latch-up and wind-up is presented. A voltage-controlled inverter with an inner current controller is used in the study. Instantaneous limiting (saturation) and latched limiting with a variety of reset strategies are tested to check for correct operation when a fault is applied and cleared. All cases were tested on an experimental system using 10 kVA inverters and low impedance 3-phase faults. The experimental results showing the current and voltage waveforms of the inverter are presented to test whether each strategy correctly transitioned from current-limiting to normal operation once the fault was cleared and to examine the extent to which controller wind-up was a problem. Conclusions are drawn as to which current-limiting strategies provide good performance in ride-through and recovery from faults.**

***Index Terms*—current control, current limiters, fault current limiters, fault currents, inverters, transient response**

I. Introduction

As the penetration of distributed generation increases, there is a need for distributed generation to remain connected when the grid experiences a fault and also provide voltage support during the fault and good recovery when the fault is cleared. The control of distributed generation to provide voltage support during faulted operation of a network is discussed in [1] - [3].

The output current of an inverter should be limited to avoid damage to the semiconductors. For an inverter to remain connected during a network disturbance, a control strategy that limits the current is required such as proposed in [4] - [8]. After the protection has operated to clear the fault, the inverter then needs to return back to normal operation as described in [9] and [10]. How the current-limiting of inverters affects the network when a fault is present has been discussed in literature [5], [11] - [13]. However, the design of the limiting strategy and the ability of the inverter to transition from normal operation to fault-mode operation (i.e. current limiting) and back again has not been discussed in control designs that utilize cascaded control loops. The need to provide limiting and anti-wind-up of multiple control loops can lead to complex fault management logic that contains latch-up conditions which prevent proper release from the fault mode.

For a typical inverter exporting power to a distribution network or microgrid which employs cascaded control loops different designs have been published. In many designs the inner controller is a closed-loop controller that controls the current through an inductor, however the outer controller may be open-loop or closed-loop. An example of an outer open-loop controller is in [12] where the outer loop is a power controller. Examples of an outer closed-loop controller are in [14] and [15] where the outer loop is a power and voltage controller respectively. For this discussion, it is not important if the outer loop is a power controller or a voltage controller, however it is important if the outer loop is of a closed-loop design or open-loop design. If the outer controller is of an open-loop design, then a simple set and reset strategy on the output of the outer controller for the transition from normal-operation to current-limiting and then back to normal-operation can be used. However, if the outer controller is of a closed-loop design, then possible latch-up of the limiters at the output of the closed-loop controllers must be considered.

This paper discusses current limiting strategies that supply current without interruption to a network when a fault is experienced and cleared for an inverter with an inner current controller and outer voltage controller. Methods of releasing the inverter controller once the fault has cleared are discussed with each proposed reset strategy. The paper draws conclusions on how limiting strategies can be designed in order to prevent latch-up of the limiter and wind-up of the controller that provides the input to the limiter.

II. Limiting the Export Current of Inverters

A. Control of Inverter Sources

Inverter sources can be controlled in the synchronous reference frame (DQ-frame), stationary reference frame ($\alpha\beta$-frame), or in the natural reference frame (ABC-frame).

The advantage of control in the synchronous reference frame is that it allows the use of a simple proportional-integral (PI) controller, shown and modelled in [16]. However, these controllers experience a degradation in performance when the load becomes unbalanced. DQ controllers are typically designed to be used with only positive sequence voltage and current

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This work was supported by a Power Networks Research Academy scholarship (http://www.theiet.org/about/scholarshipsawards/pnra/). The PNRA is brought together by the IET and funded by four UK power network companies, EA Technology and the EPSRC.

measurements. When there is an unbalance in the load, the voltage and current measurements have positive and negative sequence components. The DQ measured currents and voltages become oscillatory unless a filter is used to separate the positive and negative components of the unbalanced voltage and current measurements. For control of unbalanced loads with DQ controllers, one solution is to implement a positive sequence DQ loop and a negative DQ loop. Other designs the enable DQ controllers to supply unbalanced loads are discussed in [17]. When DQ controllers experience an unbalanced fault, the inverter output experiences an over-voltage in the un-faulted phase or phases [13]. One solution to compensate the over-voltage is to emulate an output-impedance in parallel with the filter capacitor [11].

Using the stationary ($\alpha\beta$) reference frame allows for the use of a less complex transform than that used for control in the DQ reference frame. Only a Clarke transform is required instead of a Park-Clarke transform. The reference signals in $\alpha\beta$ retain the rotation of the fundamental frequency and require a more complex controller. A proportional-resonant (PR) controller, as shown in [18], can be tuned to the nominal system frequency and is effective. Unlike DQ controllers, $\alpha\beta$ control is able to compensate both positive and negative sequence components with only two phases and without loss of performance. However, if the zero sequence component is present (which may happen in 4-wire systems) then a third control signal is required which is known as the λ signal. Supplying a balanced fault current in $\alpha\beta$ requires a fault-current vector that is circular. For an unbalanced fault current a more complex fault-current vector, that is elliptical, is required to prevent any over-voltages in the healthy phase or phases.

Control in the natural (ABC) reference frame also requires the use of PR controllers however, the advantage is that ABC has independent control of each phase and is effectively three single phase controllers. The control of each phase allows for both positive and negative sequence components (and zero sequence in 4-wire systems) to be compensated simultaneously [19]. ABC control does not require the use of transformations that $\alpha\beta$ and DQ controller require. Since ABC is effectively three single phase controllers, the same current limiting strategy can be used for single-phase and three-phase faults without causing over voltages in the un-faulted phase or phases, or without the requirement for different fault-current reference signals for three-phase and single-phase faults. For these reasons control in the ABC reference frame is chosen over control in the $\alpha\beta$ or DQ reference frames.

A PR controller in the ABC reference frame has been shown to have a good response for providing fault current for three-phase balanced faults, single-phase faults and phase-to-phase faults in [20]. Since the aim of this paper is only to consider how inverter controllers reset from current-limit to normal operation, this paper will only consider three-phase balanced faults.

B. Current Limiting

Inverters have a low thermal inertia and the current that they pass has to be constrained even on very short time-scales. If the current is too high, damage may be caused to the semiconductors [21]. Any control designed to operate during abnormal grid conditions must adhere to the physical current limit of the semiconductors. Two approaches to achieve this are to use instantaneous saturation limits or a latched limit, as discussed in [12].

Instantaneous saturation limits prevent a signal or output value increasing beyond a pre-determined value. They are simple to implement and provide an easy method to control signals within a controller. However, if the signal is sinusoidal, they clip the crest and the resulting magnitude is not pre-determinable.

A latched limit measures the signal and when the signal is above a pre-determined threshold, the latch changes the signal flow to a limit that is determined. However, these limits require consideration on how the reset is operated.

A proposal for current limiting in static synchronous compensators is to calculate the controller set point with respect to the maximum current that the inverter can safely deliver [22] [23]. This strategy allows the device to naturally limit the current without exceeding the compensator's safe operating region and without producing a distorted current. In cases where it is desirable to provide a current limit that is different to the normal export current, a latched-limit design may be chosen. For this reason, it is important to study how these limits should be reset in order to ensure correct operation during fault ride-through.

C. Wind-up

When the output of a controller is inhibited by a limiting circuit, any integrators within the controller may experience wind-up. Wind-up can be prevented by conditional integration or by tracking integration as presented in [24] - [27]. Conditional integration disables the integrator within the controller when there is a difference between the output of the controller and the output of the limiting circuit. Tracking integration measures the difference between the output of the controller and the output of the limiting circuit. This difference is fed-back to compensate the input to the integrator.

Conditional integration and tracking integration were initially designed for PI controllers and have been applied to PR controllers. Conditional integration is applied in [28] and tracking integration is applied in [28] – [30]. When a limit is triggered, tracking anti-wind-up is used in all studies presented in this paper to ensure that the integrator of the controller that provides the input to the limiter does not experience wind-up.

D. Latch-up

Latch-up is defined in this paper as occurring when the limiting strategy holds the output either in current-limit or voltage-limit and does not release the limit and return to normal-operation after the event on the network, that caused the limit-event to happen, has cleared.

III. Inverters with Multiple Control Loops

Typically, inverter control designs use a cascaded structure to control current, voltage or power. The controller used within

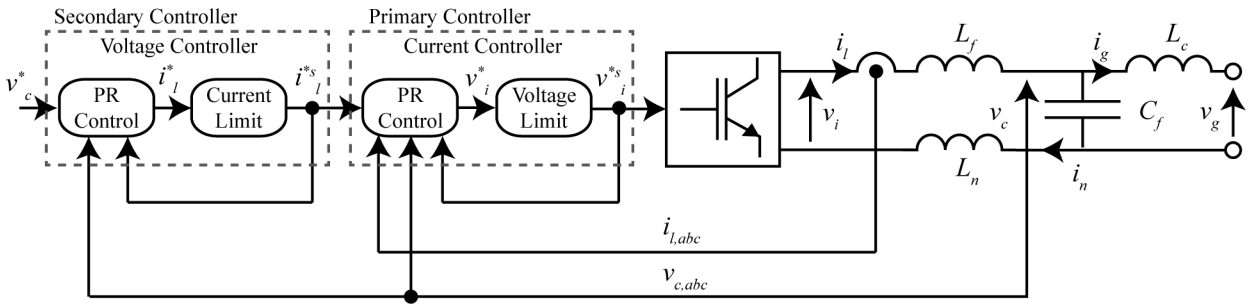

Fig. 1. Control of the inverter source used in all studies presented in this paper. The controller has multiple control loops, of which both are closed-loop. The inverter used is operated in island and does not require a PLL. One of three phases and neutral is shown.

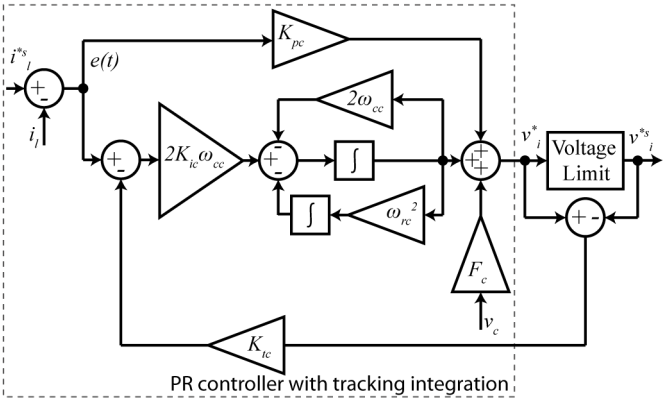

Fig. 2. Schematic of the current controller which is indicated by the dotted-box called current controller in Fig. 1. The current controller is a non-ideal PR controller with tracking integration anti-wind-up. The anti-wind-up is designed to compensate the integrator when the limiter algorithm limits the output of the controller. The voltage limit design is dependent on the case being investigated which is listed in Table I. The reset signal of the voltage limiter is not shown because it depends on the design of the limiting strategy.

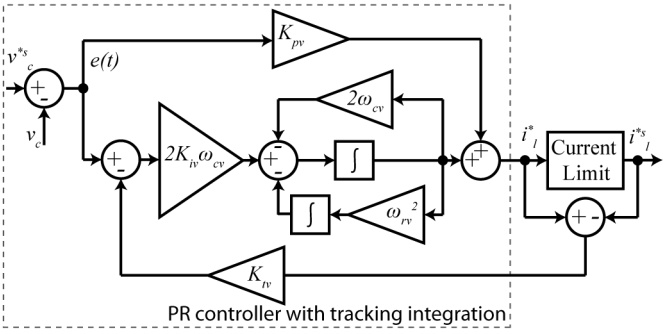

Fig. 3. Schematic of the voltage controller which is indicated by the dotted-box called voltage controller in Fig. 1. The voltage controller is a non-ideal PR controller with tracking integration anti-wind-up. The anti-wind-up is designed to compensate the integrator when the limiter algorithm limits the output of the controller. The current limit design is dependent on the case being investigated which is listed in Table I. The reset signal of the current limiter is not shown because it depends on the design of the limiting strategy.

this study comprises of two control loops, as shown Fig. 1. The inner control loop is designed to control the current through the inductor between the switching-bridge and the filter capacitor which is shown in Fig. 2. It has the highest bandwidth and is there to provide good power quality and to enable explicit limiting of the export current from the inverter. The outer

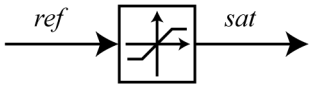

Fig. 4. Schematic of instantaneous limit used in the current and voltage limits as stated in Table I (cases 1, 2a and 3a). Each phase is limited independently.

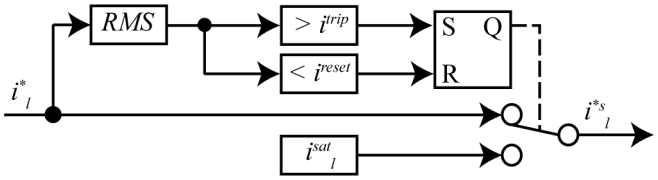

Fig. 5. Schematic of Current-Trip Current-Reset limit used in the current limit as stated in Table I (cases 2a, 2b and 2c). Each phase is limited independently.

control loop is designed to control the voltage across the capacitor which is shown in Fig. 3. The references to the outer control loop may be fixed set-points or be varied by Q/V droop functions or a remote dispatcher as in [31]. In this paper the references to the outer control loop will be fixed.

The outputs of the inner and outer control loops need to be constrained to ensure that the inverter does not operate outside of the circuits physical limits. The output of the inner controller is the voltage reference for the switching-bridge. This is limited by the modulation limit of the switches and the DC-bus voltage. The output of the outer voltage controller is the current reference for the inner current controller. The current reference is limited by the current rating of the semiconductors within the switching-bridge.

The inverter in Fig. 1 may be required to connect to an LV feeder and serve an unbalanced load. To supply current to unbalanced loads, a neutral leg was required and thus the inverter used in this study was a four-wire design. The neutral leg of the inverter was designed to allow a neutral current to flow for all unbalanced cases without damage to the neutral leg. Therefore, current limiting in the neutral has not been considered.

Seven combinations, listed in Table I, of instantaneous saturation limits and latch limits with different reset signals for the inner and outer controllers were investigated. All strategies were designed with tracking integration anti-wind-up.

Instantaneous saturation limits, as shown in Fig. 4, were built using saturation blocks in Simulink and are only active

TABLE I
DIFFERENT LIMITING STRATEGIES INVESTIGATED

Case	Current Limit		Voltage Limit	
	Output of Voltage Controller	***Trip and Limit Current***	***Output of Current Controller***	***Trip and Limit Voltage***
1	Instantaneous	30 Apeak	Instantaneous	325 Vpeak
2a	Current-Trip Current-Reset	30 Arms	Instantaneous	325 Vpeak
2b	Current-Trip Current-Reset	30 Arms	Voltage-Trip Current-Reset	229 Vrms
2c	Current-Trip Current-Reset	30 Arms	Voltage-Trip Voltage-Reset	229 Vrms
3a	Current-Trip Voltage-Reset	30 Arms	Instantaneous	325 Vpeak
3b	Current-Trip Voltage-Reset	30 Arms	Voltage-Trip Current-Reset	229 Vrms
3c	Current-Trip Voltage-Reset	30 Arms	Voltage-Trip Voltage-Reset	229 Vrms

TABLE II
PROPERTIES OF THE INVERTER SOURCE

Inverter Circuit			
Parameter	***Value***	***Parameter***	***Value***
L_f	1.35 mH	L_c	0.35 mH
L_n	0.45 mH	C_f	50 μF
Voltage Controller			
Parameter	***Value***	***Parameter***	***Value***
K_{pv}	0.05	ω_{cv}	2π0.1 rad/s
K_{iv}	46.8	ω_{rv}	2π50 rad/s
K_{tv}	1.5		
Current Controller			
Parameter	***Value***	***Parameter***	***Value***
K_{pc}	5	ω_{cc}	2π0.1 rad/s
K_{ic}	4,000	ω_{rc}	2π50 rad/s
K_{tc}	0.1	F_c	0.5
Maximum Operating Conditions			
Parameter	***Value***	***Parameter***	***Value***
Phase Current Limit	30 Arms	Phase Voltage Limit	229 Vrms
Nominal Operating Conditions			
Parameter	***Value***	***Parameter***	***Value***
Nominal Phase Voltage	220 Vrms	Nominal Frequency	50 Hz

when the reference signal is above the limit. Latch limits, Fig. 5 – Fig. 8, use a trip and reset signal to transition between two states, normal-operation and limit-operation. Normal operation is when the output of the limiter is equal to the input of the limiter. Limit-operation is when the input to the limiter is ignored and the output of the limiter is equal to an internal reference signal which is known as the limit-reference and is independent from the threshold of when the trip or reset signals are true. When the trip signal transitions from false to true, the limiter will transition from its previous state to limit-operation. When the reset signal transitions from false to true, the limiter will transition from its previous state to normal-operation. If both the reset and trip signals transition from false to true, the reset signal will take priority. When both signals are false or transition from true to false, the limiter will not change state.

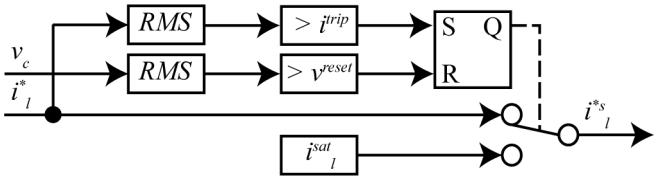

Fig. 6. Schematic of Current-Trip Voltage-Reset limit used in the current limit as stated in Table I (cases 3a, 3b and 3c). Each phase is limited independently.

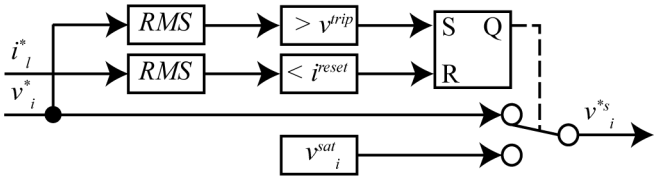

Fig. 7. Schematic of Voltage-Trip Current-Reset limit used in the voltage limit as stated in Table I (cases 2b and 3b). Each phase is limited independently.

The current-trip latch-limits, Fig. 5 and Fig. 6, were arranged to trip when the RMS value of the current reference signal from the output of the voltage controller increases above the phase current limit defined in Table II. The fault current that was exported had the same magnitude as the trip current and was at a phase of zero degrees. The voltage-trip latch-limits, Fig. 7 and Fig. 8, were arranged to trip when the RMS value of the PWM voltage reference signal from the output of the current controller increases above the phase voltage limit as defined in Table II. The voltage that was controlled after the limiter was tripped had the same magnitude as the trip voltage and was again at a phase of zero degrees.

Both of the current and voltage latch limits that use a current-reset, Fig. 5 and Fig. 7, were arranged to reset when the RMS value of the current reference signal from the output of the voltage controller decreases below 90% of the phase current limit, as defined in Table II. The reason to reset on 90% of the phase current limit is to add hysteresis so that the limiter is prevented from oscillating in and out of the limiting state when the current is near the limit value. For voltage-reset, two strategies were used. The current-trip and voltage-reset limit, Fig. 6, was arranged to reset from the measured RMS value of the filter capacitor voltage when the voltage was above the nominal phase voltage, as defined in Table II. The voltage-trip voltage-reset latch limit, Fig. 8, was arranged to reset from the RMS value of the PWM voltage reference signal from the output of the current controller when the reference signal was below the phase voltage limit, as defined in Table II. No hysteresis was added to the voltage limit because the limit is only 9 Vrms above the nominal nominal voltage of 220 Vrms.

The RMS values are calculated by first squaring the input which is a sinusoidal current or voltage signal. Next a moving-average filter with a 10 ms window is used to calculate the mean. Finally, the square-root of the mean is calculated to calculate the RMS. Due to the filtering, if the sinusoidal current or voltage input experiences a step change, there will be a small time-delay before the correct RMS is calculated.

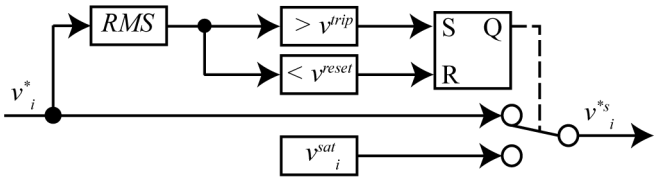

Fig. 8. Schematic of Voltage-Trip Voltage-Reset limit used in the voltage limit as stated in Table I (cases 2c and 3c). Each phase is limited independently.

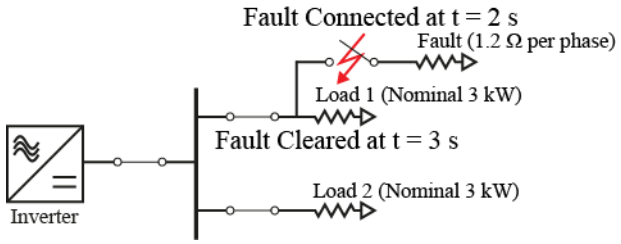

Fig. 9. Schematic diagram of the experimental setup of the inverter which as two loads and a low impedance fault that can be switched in parallel with Load 1 and then cleared by a circuit breaker.

The controller will measure the difference between the output of the controller and the output of the limiter at the output of the controller. When there is a difference, the anti-wind-up strategy will be active in order to prevent the output of the integrator from changing.

In the experimental test, the current limit was chosen based on the maximum current before the inverter would damage and the voltage limit was chosen based on the maximum possible voltage that the inverter could generate from the fixed DC-bus voltage. When setting limits in a network, the engineer would need to respect the physical limits of the inverter hardware and yet still provide enough fault current to ensure that the protection relays can detect and discriminate faults. In low current fault current environments, this might require a combination of voltage and current measures [32]. The purpose of this paper is not to discuss the setting of the limits, but to discuss strategies to reset the inverters once a limit has been activated. To calculate the fault current in a network with inverter generation a method that is presented in [12] and [20] could be used. In a network with separation of generation ownership and network operation, a connection agreement would be required that specifies the amount of fault current an inverter should export.

IV. Experimental Results of Limiting in Inverters with Multiple Control Loops

It is expected that when a low impedance fault is applied to the network, the inverter output voltage will reduce. The outer voltage controller will increase the current reference to the inner controller in an attempt to maintain the system voltage. The increase in current reference will be above the maximum current allowed for the inverter and so a current limit should activate. When the fault clears, the network impedance seen by the inverter will rise suddenly and the voltage controllers will start reducing the current reference. In cases 2 and 3, there may be a short time-delay before the current limit of the inverter is removed which is caused by the time required for the RMS to be calculated. There may also be a delay in the current controllers caused by the current reference changing from the fault reference to a new lower reference. During this period, the voltage command of the inverter can become large (because a higher than normal current is being injected into a normal network impedance). The inverter will voltage limit naturally because of the limited DC link voltage but it is advisable to apply a voltage limit at the output of the current-controller (input to the PWM reference) such that the over-voltage is controlled. If the period of over-voltage is shorter than the time required for the voltage limit to detect an over-voltage, then the voltage will be limited because of the DC link voltage.

Three aspects of control system operation during fault ride through are of interest: the period immediately after the fault (known to power system engineers as the sub-transient period) during which we want the faults currents to be brought under control; the steady-state fault response during which we desire well defined sinusoidal fault currents to flow that will allow the protection system to operate and the fault recovery period in which we desire the current to rapidly return to normal levels and the voltage controllers to rapidly regain normal control over the inverter voltages. The inverter's response to faults is achieved by activating limiters at the output of the existing controllers rather than switching to an alternative control structure although it should be noted that a limiter effectively opens one of the control loops and applies a contestant control reference to an inner controller instead.

An experimental test system as shown in Fig. 9 was built around a 10 kVA inverter constructed by TriPhase with a control structure of Fig. 1 and parameters of Table II. TriPhase is a company that supply rapid-prototyping inverters for use in laboratories. The controllers of the inverters are programed in Simulink and then uploaded to the equipment using a C compiler in Matlab. The controller of the inverters are run on a real-time computer and the inputs and outputs of the inverter are interfaced with Simulink. The real-time voltage and current data from the inverter are saved to a network storage device and can be plotted in any graphical software. Matlab is chosen to plot the real-time data. An explanation of the TriPhase equipment is at [33] and an example of the equipment being used is in [34] and [35].

The inverter was connected to two resistive loads where each load was rated at 3 kW (1 kW per phase). This is to represent being connected to two feeders, each with identical load. A 63 A contactor and a 1.2 Ω impedance were arranged to close across one of the two loads to present a low impedance fault in one of the two feeders. A second 63 A contactor was arranged in series with the load to clear the fault which represents a circuit breaker clearing the faulted feeder. The healthy feeder remained connected during and after the fault. A National Instruments Compact Rio was used to control the fault which was initiated 2 s into the test and cleared at 3 s.

Results of the experiments are shown in Fig. 10 to Fig. 16 and will be discussed in the subsections to follow. Each

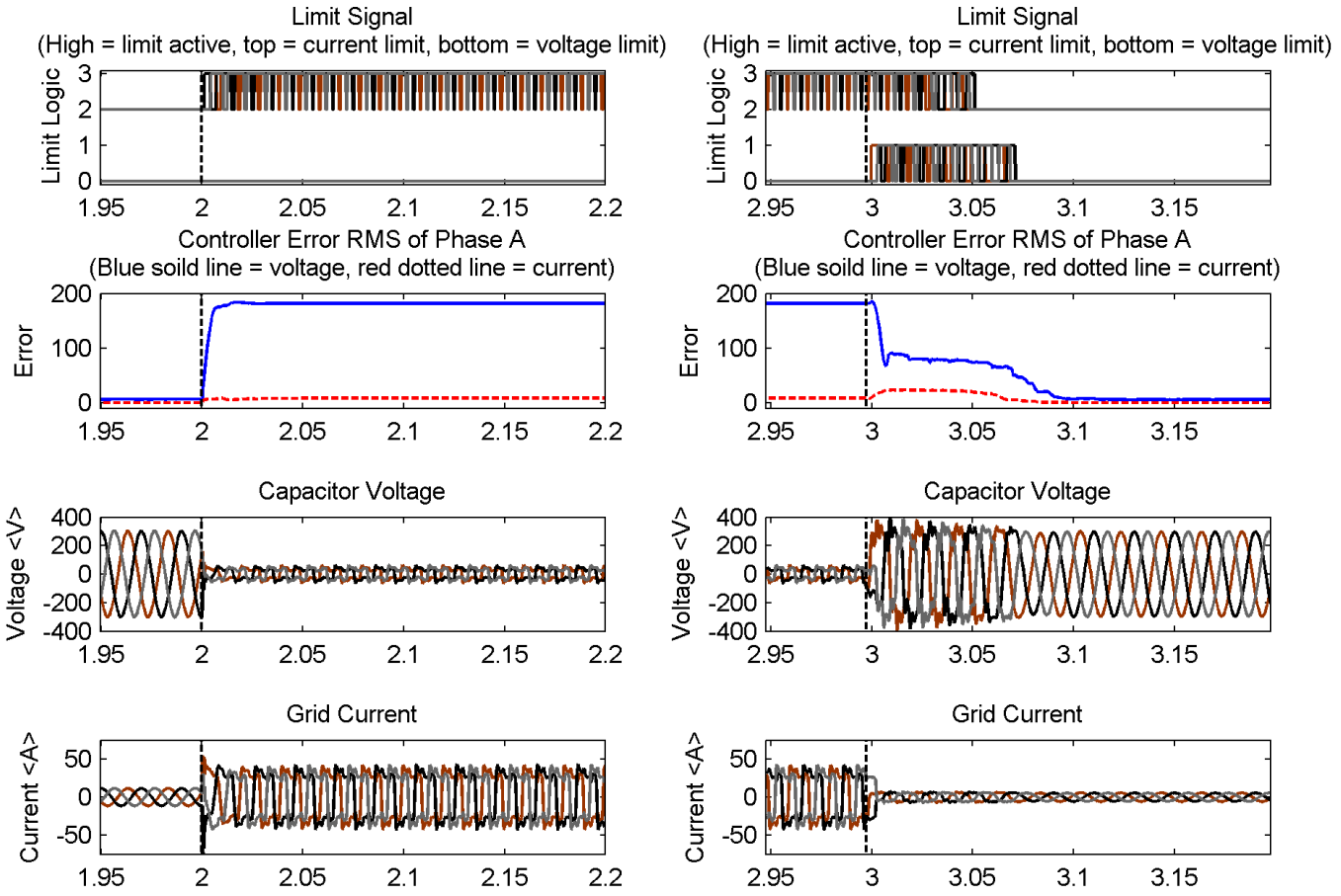

Fig. 10. Experimental results of case 1 (instantaneous) for when the fault is applied at t = 2s and when the fault clears at t = 3s as shown by the vertical black dotted line. Plots show the state of the limiting circuits, the error in the controllers, the capacitor voltage and the grid current.

figure shows results for one of the seven cases in Table I. In each figure, the left-hand plot shows fault inception with the controller entering current limit mode and exporting a fault current. The right-hand plot in each figure shows the controller returning from current limit mode to normal operation once the fault has been cleared. Each figure shows the fault timings with a vertical black dotted line.

A. Instantaneous Saturation Limiting (Case 1)

Examining the capacitor voltage and grid current in Fig. 10, it can be seen that during the fault, the capacitor voltage and grid currents were distorted. The crest of the current reference was over the saturation block threshold and was subsequently limited. This caused the crest to became flat and the limited current reference to resemble a square wave.

Once the fault had been cleared, within five cycles the controller is supplying a regulated voltage to the load. Evidence of this can be seen in all three of the right-hand plots of Fig. 10. The current-limit signal and voltage-limit signals return to false at 3.045 and 3.066 seconds respectively and the error signal in the voltage controller, shown by the blue line in Fig. 10 returns back to zero at 3.112 seconds.

There is a brief period after the fault has been cleared during which the voltage error is still very large and the the output of the voltage controller is still subject to a current limit because it exceeds 30 A. In this condition, the current controllers attempt to drive a current with a 30 A saturation level into an un-faulted (relatively high impedance) network and to do so attempts to apply a relatively large voltage. This action subsequently triggers the voltage limit, which is seen at 3 seconds in the figure, and this continues until 3.066 seconds. In this case the voltage limit only clips the crest of the voltage which causes the voltage to become distorted. Once the output of the controller returns to below the saturation level, the voltage and current are no longer distorted. The over-voltage was expected and is explained at the beginning of this section (Sec. IV). The distortion of the voltage during the over-voltage is caused by the limiting design.

It can be seen that the limit signals change independently of each other. This confirms that three-phase control in ABC is equivalent to three single-phase controllers. For this reason, it would be expected that the response of the inverter for a chosen faulted phase (for example phase a) would be the same if the fault was a single-phase on that particular phase (phase a) or if the fault were a three-phase fault.

The advantage of using instantaneous saturation limiting is that it is simple, easy to implement and not computational intensive. The main disadvantage is that the fault current is

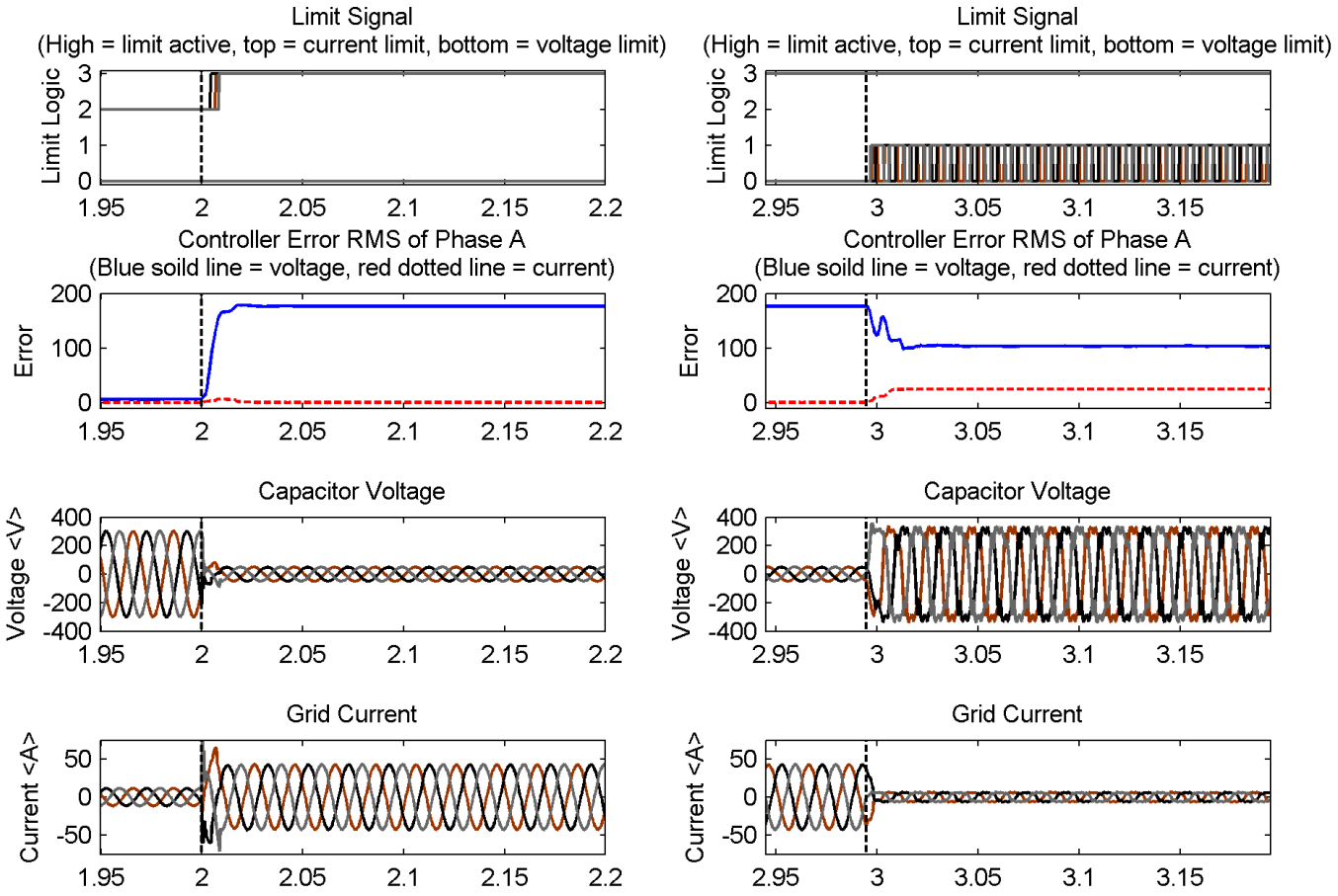

Fig. 11. Case 2a: Current-trip, current-reset current limit and instantaneous voltage limit. The fault timings are shown by the vertical black dotted line.

distorted. Another disadvantage is that it is not possible to supply a lower or higher fault current once the current limiter has been triggered. For example, in a fault constrained network it may be necessary for the inverters to limit the output at 1 pu current but supply 0.5 pu of fault current. Or in a network where the fault level is low, it may be necessary to limit at 1 pu current but supply 2 pu of fault current.

B. Current-Trip and Current-Reset i_l Limiter

At the start of the fault, the current reference from the output of the voltage controller increases to hold up the volts and causes the limiter to trip as seen in the left-hand plots of Fig. 11 – Fig. 13. Each left-hand plots of Fig. 11 – Fig. 13 was the same because they use the same method to limit the current. The anti-wind-up causes the integrator of the voltage controller to saturate at a current which is greater than the limit threshold. The voltage controller was no longer in 'control' as shown by the blue-solid line exhibiting a high error in the error plot for the duration of the fault. The fault current exported by the inverter shown in Fig. 11 – Fig. 13 was not distorted. This is because the fault-current reference-signal is independent from the current reference-signal that caused the limiter to trip. As in case 1 and with the same explanation, the voltage limit was triggered once the fault had been cleared.

1) Instantaneous v_i limiter (Case 2a): When the system voltage was above the limit threshold, as seen in the voltage limit signal in Fig. 11, the output voltage from the inverter became distorted due to the instantaneous limit clipping of the crest of the PWM reference RMS voltage. The distortion can be seen in the capacitor-voltage plot of Fig. 11.

It can be seen from the right-hand-plots of Fig. 11 that the current limiter never reset after the fault had been cleared. This is because the output of the voltage controller (input to the current limiter) remained greater than the reset threshold of the current limiter. An explanation for this is that the feedback from the tracking integration kept the output of the integrator, within the voltage controller, above the current limit threshold. This feedback prevents the limiter from resting and thus the current-limiter has experienced latch-up. For the inverter to supply the fault current across the non-fault load, the inverter would need to increase the output voltage to beyond the voltage limit. For this reason the output of the current controller (input to the voltage limiter) was limited.

Neither the current controller or the voltage controller regain control (error would return to zero in the right-hand side of Fig. 11) of the inverter once the fault had been cleared.

2) Voltage-trip and current-reset v_i limiter (Case 2b): In Fig. 12 after the fault had been cleared, as with case 2a, the current limiter did not reset. The explanation for this is

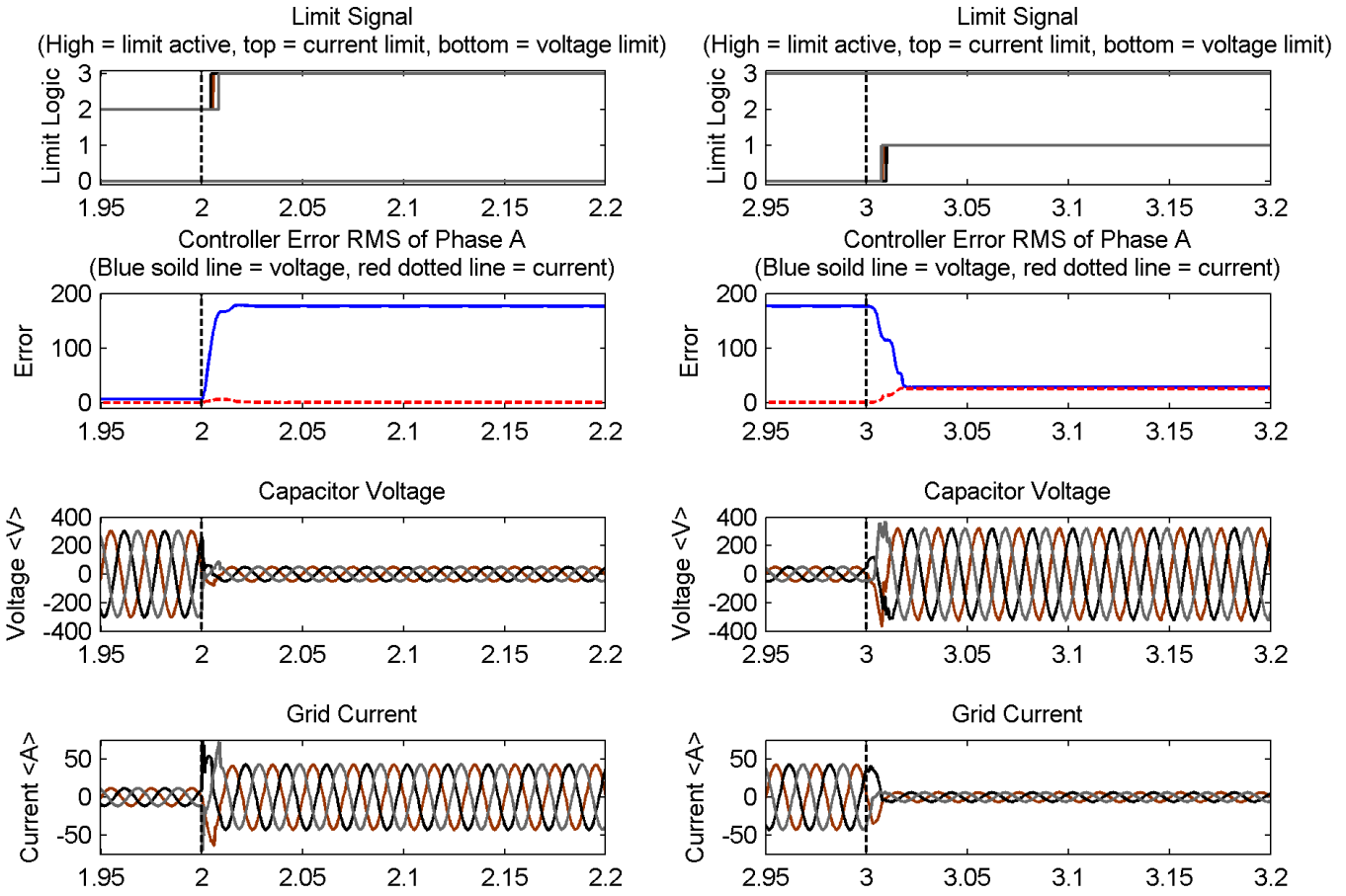

Fig. 12. Case 2b: Current-trip, current-reset current limit and voltage-trip, current-reset voltage limit. The fault timings are shown by the vertical black dotted line.

identical to case 2a. The feedback from the tracking anti-wind-up is preventing the current limiter from resetting and the current limiter has latched-up.

Since the output of the voltage controller (input to the current limiter) remained high, the current reset was never activated and the voltage limit was inhibited from resetting. If the voltage limiter were to be reset from the measurement of output current, then in this case the voltage limiter would have reset. However, the inverter is physically limited by the DC bus voltage and the output would be similar to when the PWM voltage reference was limited by an instantaneous saturation limit. Also, since the tracking integration for the current controller would no longer be active, the current controller may experience wind-up.

3) Voltage-trip and voltage-reset v_i limiter (Case 2c): For the same reason as the previous two cases (cases 2a and 2b) with a current-trip and current-reset current-limiter, the tracking integration inhibited the limiter from resetting. Since the current limiter did not reset, the reference to the current controller was much higher and this caused the output of the current controller, the PWM voltage reference, to remain high and prevent the voltage limiter from resetting.

4) Current-trip and current-reset conclusion: In all cases, the current limiter experienced latch-up because the output of the voltage controller was kept high from the feedback of the tracking integration anti-wind-up. The design of the voltage limit did not assist the reset of the current limit.

A possible solution to allow the current limiter to reset would be to increase the gain of the tracking integration. This would decrease the output of the integrator and allow the reduction of the error signal once the fault had been cleared to lower the output of the voltage controller (current reference) to a level that is below the reset threshold of the limiter. However, an increase in gain may cause the integrator to become unstable.

Another possible solution to allow the current limiter to reset could be to change the anti-wind-up strategy and use conditional integration. However, if the output of the proportional gain was much lower than the threshold of the limit for both during and after the fault, then the current limiter would reset once the output of the integration had been forced to zero. Next the current output of the inverter would increase, because of the fault impedance, until the limiter was activated again. This limit oscillation would continue until the fault had been cleared.

When the outer controller uses integrators within the design, this set of experiments has shown that the limiter to the output of the outer controller should not be reset from the output

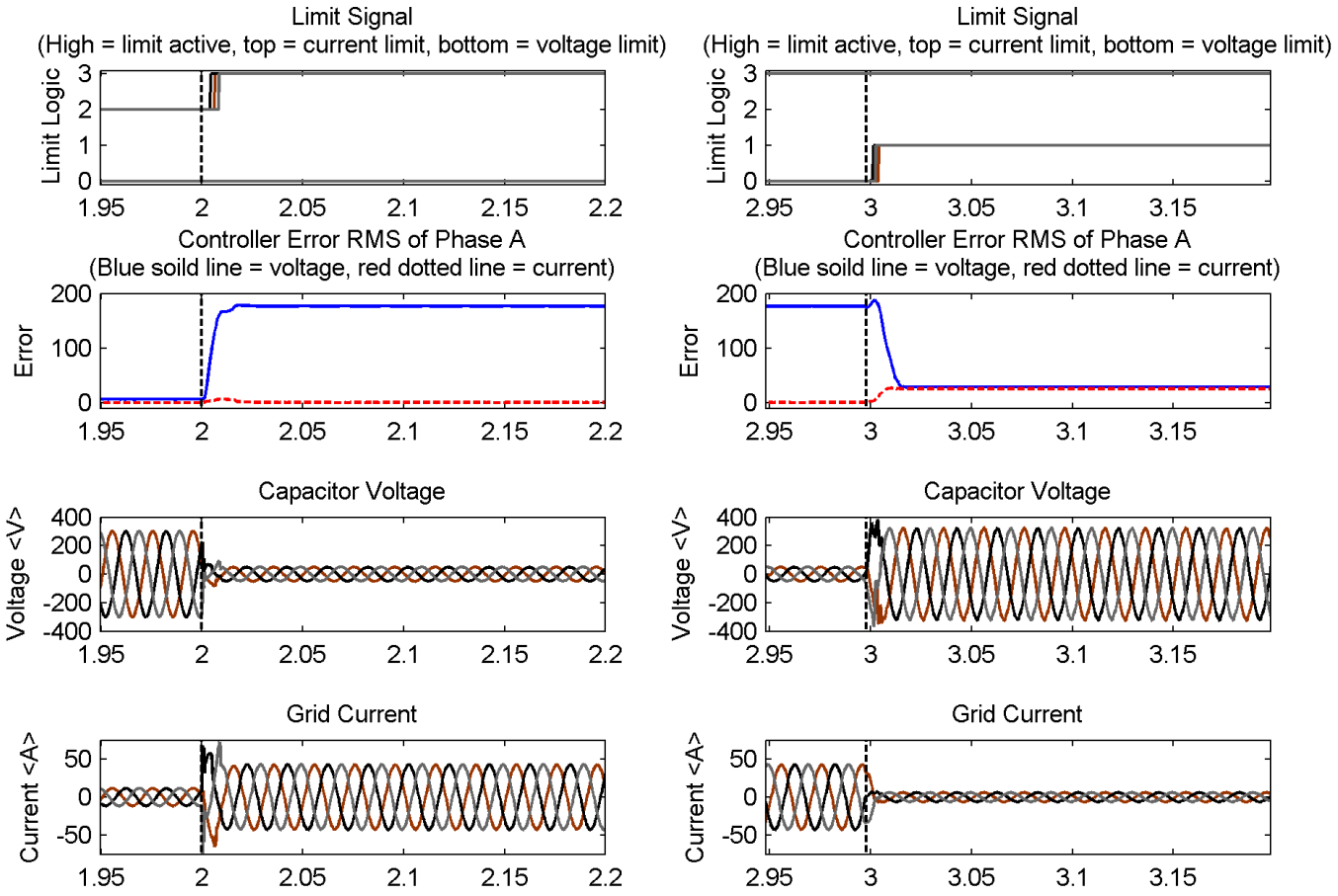

Fig. 13. Case 2c: Current-trip, current-reset current limit and voltage-trip, voltage-reset voltage limit. The fault timings are shown by the vertical black dotted line.

of the outer controller. This then allows for the limiter to successfully reset once the fault has cleared and that either tracking integration or conditional integration could be used for the anti-wind-up strategy of the outer controller.

C. Current-Trip and Voltage-Reset i_l Limit

As with the cases 2a – 2c that use a current-trip and current-reset current-limit, the fault current, as seen in Fig. 14 – Fig. 16, is not distorted. Once the fault has been cleared, the voltage will increase if the inverter continues to supply fault current. Therefore when the voltage rises after the current limit has been activated, it would be a reasonable to assume that the fault has been cleared and the inverter should return from current-limit to normal-operation. To comply with this logic, the current-limiter in cases 3a – 3c will be tripped when the output of the voltage controller (current reference) is above a pre-defined threshold and will be reset when the measured capacitor voltage has increased above a pre-defined threshold, as shown in Fig. 6.

1) Instantaneous v_i limiter (Case 3a): As expected, the instantaneous limit at the output of the current-controller triggered because there was a small time between the current limit resetting and the controllers returning to steady-state. This event is seen in the right hand plot of Fig. 14. There was no latch-up or wind-up and the controller operated correctly once the fault had been cleared, as shown by the controller error signal returning to zero. However, the transition time for the voltage controller to re-establish an undistorted voltage was 6 cycles as seen in the capacitor-voltage of Fig. 14. This is caused by the output of the voltage controller having to decrease from the tracking integration anti-wind-up. A reduction in time from the fault clearing to the controller returning to steady-state could be achieved by resetting the integrator in the voltage controller once the current limit reset is operated, or by using condition integration anti-wind-up instead of tracking integration anti-wind-up.

2) Voltage-trip and current-reset v_i limiter (Case 3b): Once the voltage limit is triggered, it does not reset as seen in the voltage limit signal of Fig. 15. After the current limit reset, the voltage controller wound-up because the output of the current controller was being held by the voltage limit as seen in the limit signals of Fig. 15. The wind-up of the voltage controller causes the input to the current controller to increase which is seen by the increasing current-error plot in Fig. 15. Since the limiter is deactivated, the output of the limiter is equal to the input to the limiter (output of the voltage controller). This did not happen when the voltage limiter was an instantaneous saturation limit. An explanation is because the voltage limiter

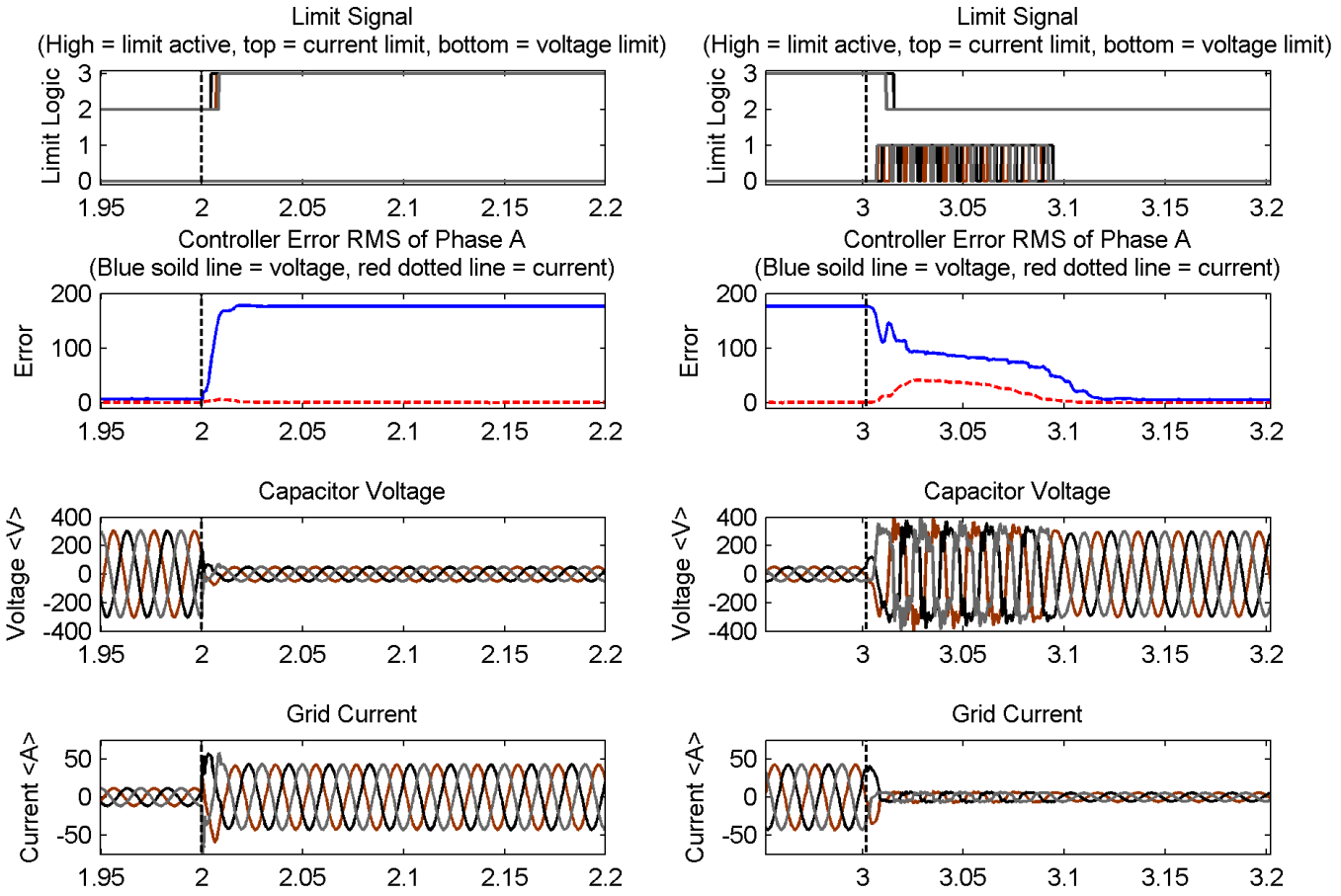

Fig. 14. Case 3a: Current-trip, voltage-reset current limit and instantaneous voltage limit. The fault timings are shown by the vertical black dotted line.

only clipped the output and did not hold the output constant. This allowed the controller to regain 'control' of the inverter. A positive comment is that the transient of the current and voltage of the inverter once the fault had cleared in Fig. 15 was less-distorted than when the voltage limiter was using saturation limits as in case 3a and seen in Fig. 14.

3) Voltage-trip and voltage-reset v_i limiter (Case 3c): As with the previous case, this case presented in Fig. 16 does not distort the capacitor voltage after the fault had cleared. However, the strategy failed for the same reason as case 3b. Again, when the current limiter was reset, the output of the voltage controller experienced wind-up as shown by the increasing current-error signal in the right-hand plot of Fig. 16.

4) Current-trip and voltage-reset conclusion: When the output of the current-controller (limited by the voltage limit) used instantaneous saturation limiting, the controller successfully returned to normal operation after the fault had cleared as shown by the right-hand side plots in Fig. 14. Cases 3b and 3c both failed because the output of the current-controller (voltage limit) remained in limit-mode when the output of the voltage-controller had reset. Therefore, it is concluded that the voltage-limiter should not be designed to latch and a saturation limit with anti-wind-up should be used.

In all current-trip and voltage-reset current limit, cases 3a – 3c, the current during the fault has low distortion and the current limiter reset after the fault had been cleared. To ensure the current limit resets correctly when the outer controller (voltage controller in all 7 cases) uses an integrator, the reset signal for the current limiter should not be the output of the voltage-controller to ensure that the limiter correctly resets after the fault has cleared.

V. Conclusion

This paper has investigated how current and voltage limiting should be implemented in inverters with cascaded control loops with particular reference to preventing latch-up of the limiters and wind-up of the controllers. A further consideration was the desire to avoid high levels of distortion of current and voltage waveforms during the fault.

The results of the study here show that to avoid high levels of distortion of current and voltage waveforms during the fault the current limit (applied to the current reference at the output voltage controller) should be a set and reset function. The set and reset limiting of the current reference preserves sinusoidal current references during the majority of the fault and recovery period and avoids high levels of harmonic distortion.

Providing the current limiter correctly resets after the fault has been cleared, the results show that the best transient stability performance is obtained when the voltage limit (applied to the inverter voltage command at the output of the

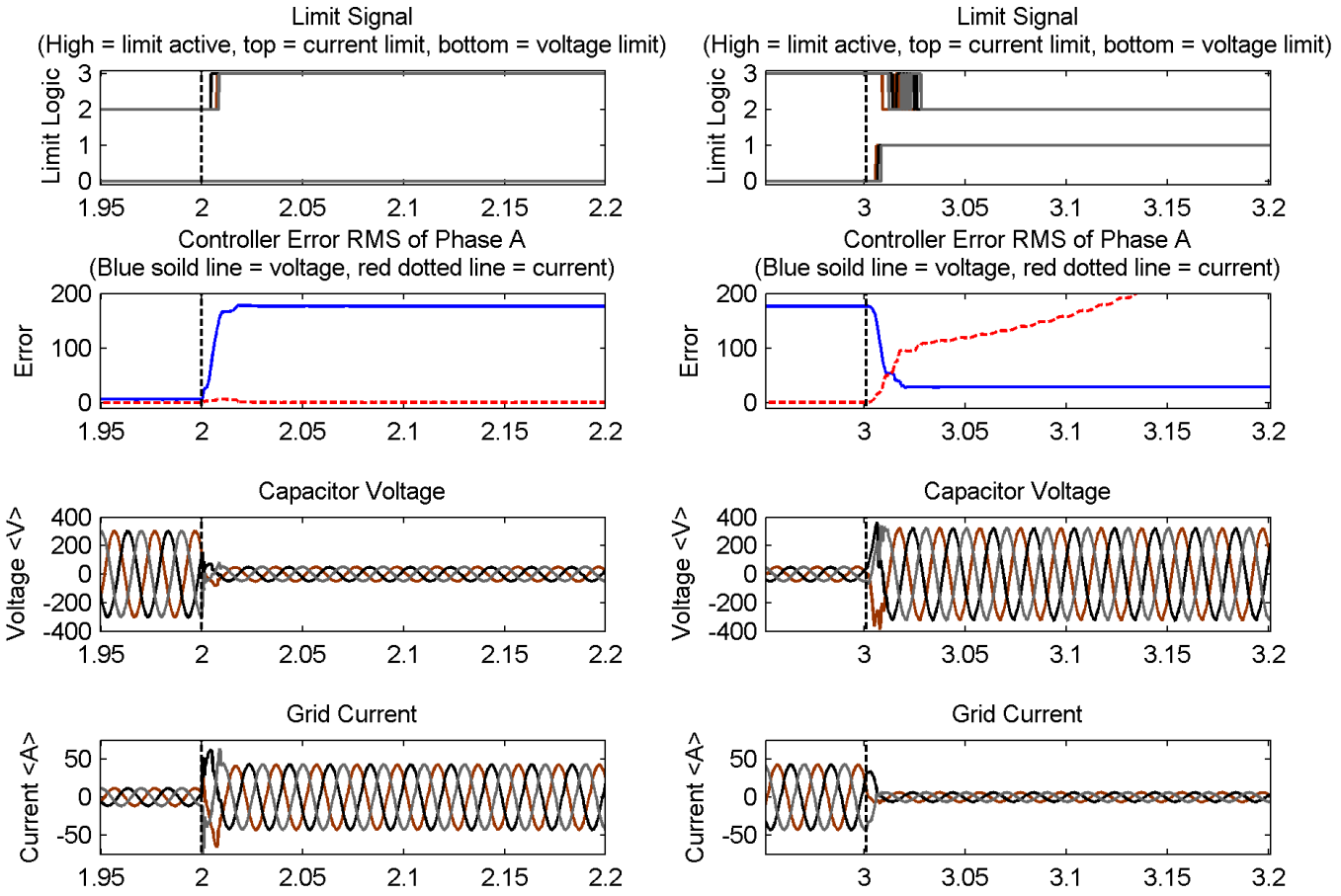

Fig. 15. Case 3b: Current-trip, voltage-reset current limit and current-trip, voltage-reset voltage limit. The fault timings are shown by the vertical black dotted line.

current controller) is an instantaneous (saturation) function, as shown in cases 1 and 3a. The instantaneous limiting of the inverter voltage command helps prevent wind-up of the outer controllers (in this study was a voltage controller) once the current limit is reset. Although this does cause distorted voltage waveforms to appear for a short period after fault clearance as the voltage controller establishes control of the capacitor voltage. If the current limit (output of the voltage controller) is reset and the voltage limit (output of the current controller) is set, these experimental results have shown the outer voltage controller to experience wind-up.

For avoiding latch-up of the set/reset current limit, it is important that the reset signal is not derived from the output of the outer controller as in cases 2a – 2c. These experimental result have also shown that using a set/reset voltage limiter at the output of the inner controller did not assist in the resetting of the current limiter at the output of the outer controller. The set and reset design for case 3a which used the current reference (output of the voltage controller) to initiate a set and the measured inverter capacitor voltage to initiate a reset was the only latched current limiter to reset when used with an instantaneous voltage limiter. For case 3a to function correctly in other networks, the capacitor voltage would only recover (and cause a reset) provided the network impedance seen when the fault clears is sufficiently high. For a micro-grid, this will be true if the total post-fault load power demand is within the capacity of the generators remaining on the system.

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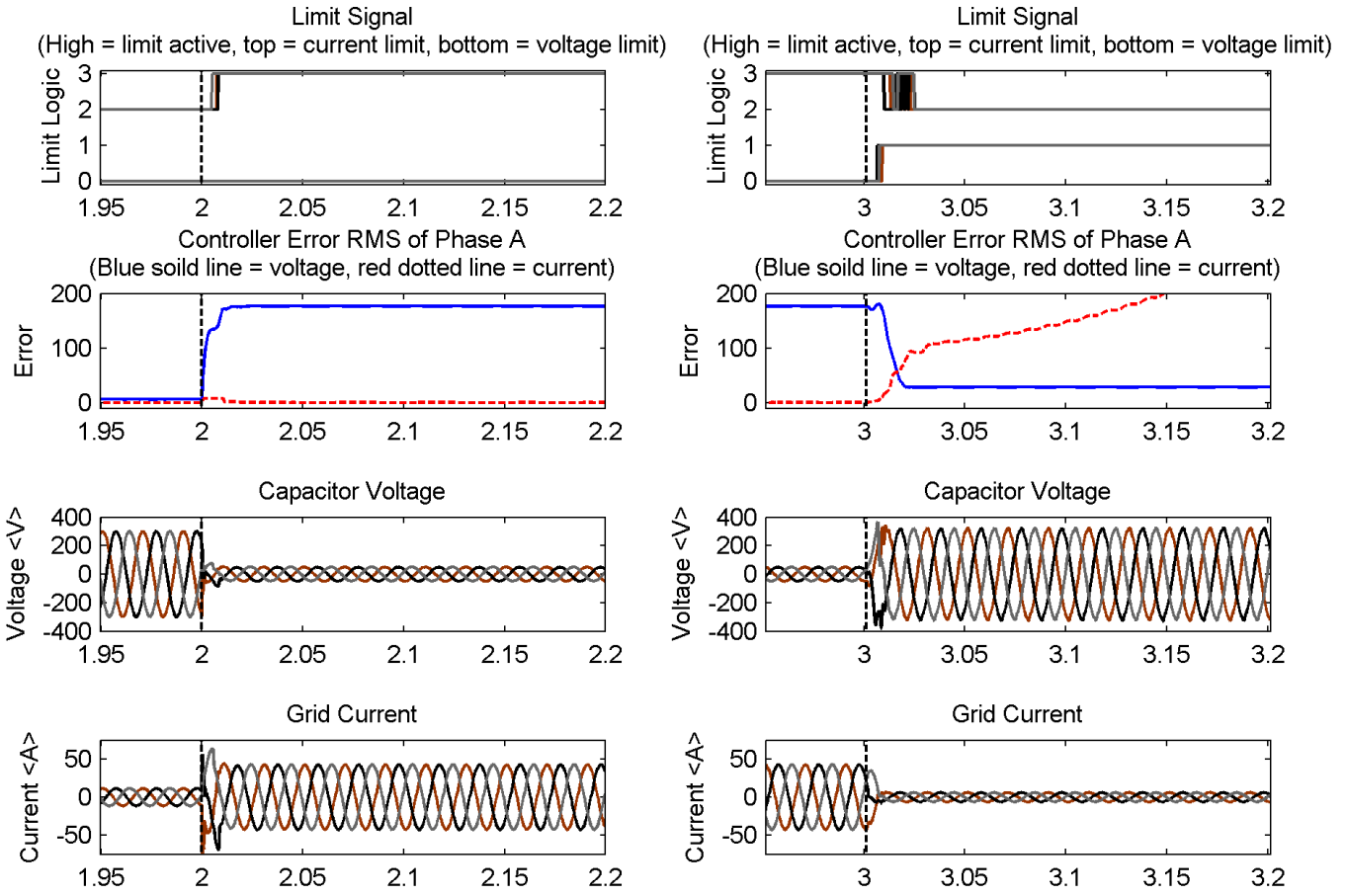

Fig. 16. Case 3c: Current-trip, voltage-reset current limit and voltage-trip, voltage-reset voltage limit. The fault timings are shown by the vertical black dotted line.

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