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Comparison of LER Induced Mismatch in NWFET and NSFET for 5-nm CMOS

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ABSTRACT Nanosheet field-effect transistors (NSFETs) have emerged as a novel device replacement for sub-7nm CMOS technology nodes. However, due to smaller fin thickness (Tfin = 5nm), NSFETs are more vulnerable to the process-induced variations. Among various types of process-induced variations, Line edge roughness (LER) is becoming a significant concern for multi-gate field-effect transistors (MugFETs) with smaller feature sizes. In this article, we have reported and compared the impact of LER on the electrical characteristics of NSFETs and nanowire field-effect transistors (NWFETs) for the sub-7nm technology node. We have generated a 3-D LER profile using 2-D Auto Covariance Function (ACVF) that considers two degrees of freedom for a realistic roughness analysis at advanced CMOS technology nodes. For a complete study of 3-D LER effect in NSFET, we have considered roughness along the nanosheet's sidewalls as well as top and bottom surfaces. We have shown using 3D TCAD simulations that the sidewall roughness in NSFETs contributes to a negligible mismatch in threshold voltage and ON current. The mismatch performance of NSFET is compared with that of the NWFET for sub-7nm technology node. NSFET appears to be more immune to mismatch in ON current than NWFETs considered in this work. On the other hand, as compared with NSFET, owing to its superior gate all-around control, the NWFET achieves lower mismatch in drain induced barrier lowering (DIBL) and subthreshold slope (SS) in presence of LER. In addition to this, FETs with different channel doping modes such as inversion (IM) and Junction less (JL) mode have been compared for their matching performance against 3-D LER. It can be concluded from the results that IM FETs are more immune to 3-D LER as compared to JL FETs.

INDEX TERMS Line edge roughness, mismatch, nanosheet (NS), auto-covariance function, CMOS scaling.

I. INTRODUCTION

Nanosheet field-effect transistors (NSFETs) have gained significant attention in recent days owing to its higher drive current and superior frequency response compared to FinFET and nanowire field-effect transistors(NWFETs) [1]–[5]. Resilience against short channel effects and better gate electrostatic control over channel due to GAA structure makes NSFETs and NWFETs suitable for sub-7nm technology nodes centric design [6]–[7]. However, progressive scaling of CMOS devices aggravates process-induced variation in these devices, and as a result, device performance deteriorates [8]–[16].

Process induced variations, such as random dopant fluctuations, work function variations, and line edge roughness (LER), can significantly affect circuit performance [17]–[32]. Among these, LER, due to lithography and etching process, is a major source of mismatch, and it is not easy to reduce [23]–[27]. Espiñeira *et al.* reported a variability study on FinFET and NWFET for LER, metal grain granularity (MGG), RDF, and gate

edge roughness (GER) [23]. LER has been prevalent as a dominant source of variability among all other sources of process variation in FinFET and NWFETs [23]. LER can induce variation in sheet thickness (T_{fin}), fin width (D_{fin}) of NSFET, and as well as in diameter (D_{nw}) of NWFET, which may result in a higher mismatch in threshold voltage (Vth), and drive current (Ion) in these devices [25]–[28]. Matching performance of FinFET and NWFET with different channel doping modes, such as inversion (IM) and junctionless (JL) mode, have also been reported earlier [30]–[31]. JL FET devices are preferred design architecture for smaller channel length devices due to the absence of source/drain junctions, simple fabrication process, and higher drive current [30]. However, higher doping requirements and shorter channel length design of the JL FET device make it more prone to LER induced mismatch [31]. Thus, it is essential to perform extensive and correct LER analysis on NSFET for future advanced CMOS design. Many papers reported analysis of LER induced mismatch on FinFET and NWFET based on 3-D LER models [20], [25]. For conventional planar FETs, l-D Auto Covariance Function (ACVF) based 2-D LER model was used for LER analysis [21]. Conventional model provided LER only along the line, however for non-planar FETs, roughness is required along the entire surface [17]. Therefore 3-D LER models based on 2-D ACVF function are being used for non-planar FETs and other advanced technology node devices [20], [24].

A significant amount of work on LER in NWFETs and FinFETs has been reported earlier [27]–[29]. Indalecio *et al.* reported the spatial sensitivity of LER in GAA NWFET [28]. It was found that LER induced deformation inside the source and drain region does not cause any change in the performance of NWFET. However, deformation inside the gate region significantly changes device performance [28]. In this work, we have taken a generalized 3-D LER roughness profile in NW and NS-FETs for the worst-case LER scenario [13], [20].

Earlier reports also found that FinFET is more immune to LER as compared to NWFET [17], [24]. Sudarsanan *et al.* reported variability in subthreshold swing and carrier mobility for SOI FinFET due to LER [26]. It is observed that variability in Vth and Ion increases with gate length downscaling. However, very few authors have reported on LER matching performance for NSFETs. Impact of sheet thickness variation (STV) on mismatch in NSFET has been reported earlier by Amita *et al.* [25]. Vardhan *et al.* reported variability analysis on NSFET with modulation of metal thickness variation (MTV) along with the gate [29]. MTV causes variation in work function (WF) and finally results in variability in Vth. Thus, NSFET matching performance needs a detailed investigation. In this work, we report a comparison of NSFET's matching performance with that of NWFETs for the sub-7nm technology node. Matching performance of IM and JL mode NS/NWFETs are also reported in this work. We have performed 3-D TCAD simulations using a 3-D model of LER through a 2-D Auto Covariance Function (ACVF).

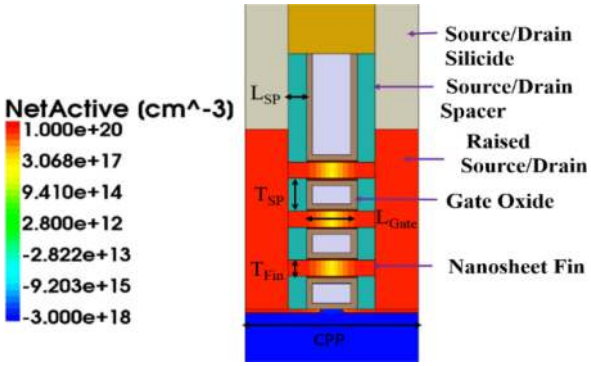

FIGURE 1. 2-D perspective view of vertically stacked NSFET and doping profile along the channel current direction [2].

TABLE 1. Device design parameters for NSFET and NWFET.

Device Parameters	NSFET	NWFET
Gate Length, L_{gate} (nm)	12	12
NS width, D_{fin} (nm)	45	N/A
NS thickness, T_{fin} (nm)	5	N/A
NW diameter, D_{nw} (nm)	N/A	6
Effective Oxide Thickness,EOT (nm)	1	1
Contact Poly Pitch, CPP (nm)	48	48
Spacer Length, L_{SP} (nm)	5	5
Fin to Fin Spacing, T_{SP} (nm)	10	10
Max. Supply Voltage at Drain, V_{DD}(V)	0.7V	0.7V
Silicon Crystal Orientation	<100>	<100>

This article is arranged as follows: 3-D device design and LER generation approach is described in Sections II and III, while the results showing mismatch comparisons for different devices are presented in Sections IV, V, and VI. Conclusion is drawn in Section VII.

II. 3-D DEVICE DESIGN AND SIMULATION

Sentaurus 3-D TCAD tools were utilized for the analysis of LER in NSFETs and its comparison with NW FETs [34], [35]. Vertically stacked NSFETs for 5nm CMOS technology node were designed and simulated as per the parameters listed in Table 1 and as is shown in Fig. 1. We have done benchmarking of our simulation results against published experimental results reported by Loubet *et al.* [2].

It can be seen from Fig. 2 that our simulations correlate to experimental results reasonably well. For device simulations, we have used the hydrodynamic transport model coupled with Poisson's and continuity equations. Density gradient model has been used for quantum confinement effects [34]. For minority carrier recombination, Shockley-Read-Hall and Auger recombination models were used. We have used inversion and accumulation mobility model (IALMOB)

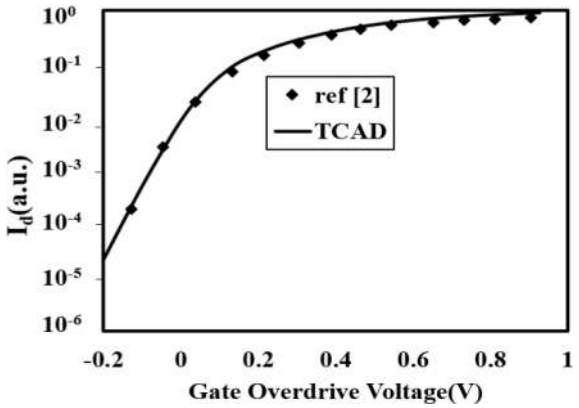

FIGURE 2. Simulated drain current as a function of gate over-drive voltage for NSFETs in the saturation region (V_{DD} = 0.7V), the calibration is against the experimental data reported in [2].

for taking doping and transverse field dependencies and two-dimensional Coulomb scattering.

Calibrated TCAD device model parameter values are listed in Table 2, where 'γ' represents the quantum potential model parameter, 'WF' represents metal gate work function, 'C' represents phonon scattering parameter, 'δ' represents surface roughness scattering parameter, and 'vsat0' represents the high-field saturation parameter.

We have taken the nearly same value of the effective mass of electron in lateral or transport direction [$m_l = 0.9163m_0$] and transverse direction [$m_t = 0.19m_0$] as reported for NSFET [3]. We have already discussed NWFET calibration in our previous work [31]. Quantum confinement cause discretization in bandgap that results in larger bandgap for the thinner semiconductor material. From the band structure analysis, it was found that E_g will be nearly equal for 5nm and 6nm thick NSFET for <100> crystal orientation [3]. Therefore, we have taken the same γ for NSFET (T_{fin} = 5nm) and NWFET (D_{nw} = 6nm). Metal gate WF has been used for matching threshold voltage (V_{th}) and subthreshold slope (SS) of NSFET. C and δ are mobility parameters, which mainly model degradation due to the transverse field as a result of the applied gate bias voltage. Degradation due to the lateral field at larger drain bias voltage is modeled using 'vsat0'.

III. LER GENERATION METHODOLOGY

Surface roughness in 3-D along the sidewalls, top, and bottom surfaces are generated using a 2-D ACVF that considers two degrees of freedom to generate surface roughness instead of line roughness [17], [20]. Hence, it provides a better roughness estimation in small-scale non-planar devices. A Gaussian type LER profile is generated for r.m.s. surface roughness, Δ = 0.5nm to 0.8nm and correlation length, $\Lambda x = \Lambda y$ = 20nm [17]. Here, Δ is the amplitude of the LER, Λx and Λy are defined as the average distance between the two points of uncorrelated amplitude along x and y-directions of the surface respectively. Fig. 3(a) and (b) show the structure with fin sidewall roughness and top-bottom surface roughness respectively, while NWFET structure roughness is shown in Fig. 3 (c).

TABLE 2. TCAD parameter for NSFET and NWFET calibration.

Device		NWFET	NSFET
Parameter	Default	Optimized	Optimized
γ (a.u)	3.60	7.00	7.00
WF (eV)	N/A	4.55	4.51
C(cm5/3/V2/3/s)	4.40e+3	3.40e+3	3.40e+3
δ ($cm^2\ V^{-1}s^{-1}$)	3.97e+13	3.97e+15	1.97e+15
vsat0 (cm/s)	1.07e+7	0.80e+7	0.73e+7

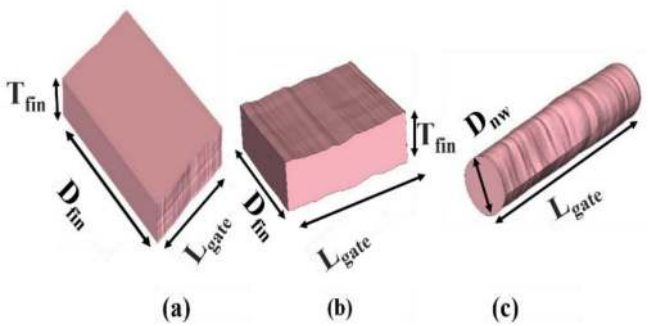

FIGURE 3. 3-D Rough surface along with the (a) sidewall (b) top-bottom surface in NSFET and, (c) cylindrical NWFET.

From fabrication perspective, different surfaces of the NSFET see different process conditions. For instance, the sidewalls of the NSFET stack are exposed to an RIE step during sheet patterning, which can induce some roughness. NS tops and bottoms, however, do not see this RIE but instead are exposed to the sheet release step [2]. In that scenario, the sacrificial SiGe layers are removed, in turn exposing the remaining sheet regions to the SiGe etch process. Although this etch is selective to SiGe over Si, the Si regions may still etch at some finite rate, especially if any Ge from the SiGe layers has diffused into the Si layers during any preceding thermal processing. Our intent in treating all sheet surfaces as having roughness is meant to convey the worst possible case of induced surface roughness in an NS structure. Therefore, we have taken the same amount of roughness along NSFET surfaces for the worst-case scenario.

A detailed discussion on LER generation in GAA NWFET is presented in our previous work [31]. It was also reported that vertically stacked nanowire devices achieve lower mismatch when compared to devices with a single nanowire due to the averaging effect of LER over the number of stacked wires [17]. In this work, we have performed TCAD simulations of devices with a single nanosheet or nanowire, which could mimic the worst-case scenario. Also, owing to the complexity involved in generating the roughness along sidewalls, top, and bottom surfaces together, we have considered

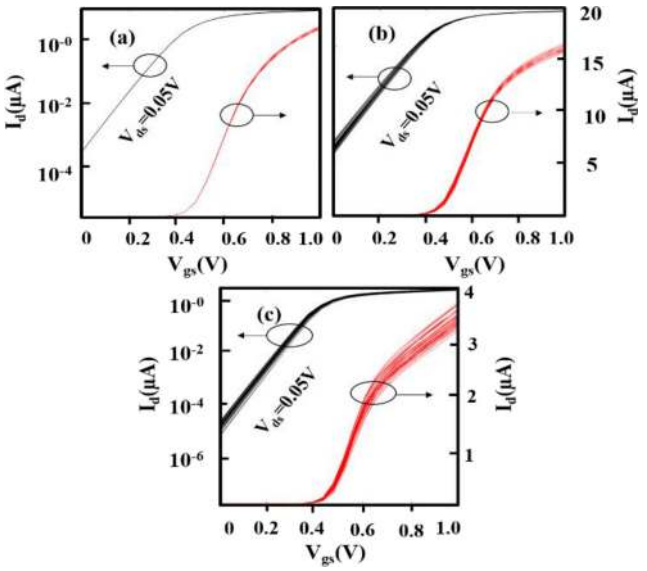

FIGURE 4. $I_d - V_{gs}$ curves with LER in (a) sidewall (b) top-bottom surface in NSFET, and (c) cylindrical NWFET using LER Parameters $\Delta = 0.5$nm, $\Lambda_x = \Lambda_y = 20$nm, simulation ensemble size = 500.

uncorrelated roughness along each of the surfaces of the NSFET individually.

IV. MISMATCH IN NSFET AND NWFETS

Drain current vs. gate voltage ($I_d - V_{gs}$) curves of 5nm technology node NSFET and NWFETs are shown in Fig. 4 for an ensemble size of 500 simulations.

The threshold voltages (V_{thlin}) for these devices are kept identical by adjusting the metal gate work function (WF). It can be seen from Fig. 4 that NSFETs with sidewall roughness offer least amount of variation in linear region drain current (I_{dlin}) and V_{thlin} when compared to both the NSFET with top-bottom surface roughness as well as NWFETs with 3-D roughness. Therefore, the effect of sidewall LER on electrical parameters of NSFET could be neglected. Smaller diameter (Dnw = 6nm) or fin thickness (Tfin = 5nm) in NW/NSFETS causes more quantum confinement in the channel as compared to confinement in NSFET with its larger fin width (Dfin = 45nm) [20], [32]. Due to this, NSFET with sidewall roughness becomes less vulnerable to LER and finally results in superior matching performance.

Histograms plot for mismatch in ΔV_{thlin} and percentage change in overdrive current (β) are shown in Fig. 5 for 5nm node NW and NSFETs. The percentage change in the overdrive current is represented by β. The overdrive current (I_{odlin}) is defined as the current at a gate voltage ($V_{gs} = V_{od} + V_{thlin}$), where V_{od} is the overdrive voltage and V_{thlin} is threshold voltage for the device in the linear region. β is written as [31]:

$$\beta = 100 \times \frac{\Delta I_{odlin}}{\text{Mean}(I_{odlin})} \tag{1}$$

It can be observed from Fig. 5 that both the ΔV_{thlin} and β distributions are broader for NWFETs as compared to

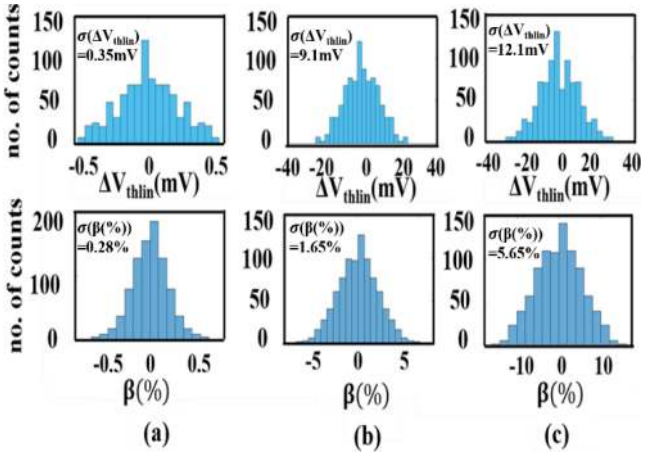

FIGURE 5. Histograms of ΔV_{thlin} and β for roughness in (a) sidewall (b) top-bottom surface in NSFET and (c) cylindrical NWFET using LER Parameters $\Delta = 0.5$nm, $\Lambda_x = \Lambda_y = 20$nm, ensemble size = 500 simulations.

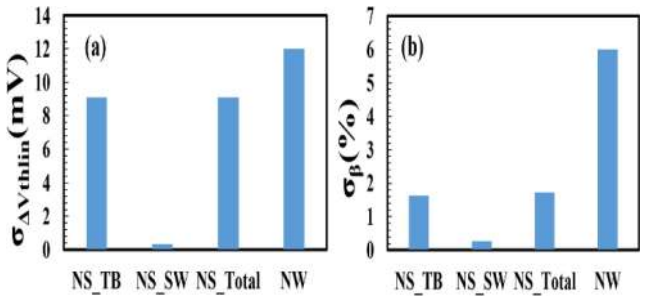

FIGURE 6. Bar plot of 5 nm technology node devices for (a) $\sigma[\Delta V_{thlin}]$ (b) σ_β (%), using LER Parameters $\Delta = 0.5$nm, $\Lambda_x = \Lambda_y = 20$nm, ensemble size = 500 simulations.

NSFETs. From the distributions shown in Fig. 5, σ [β (%)] is found to be 5.65 % for NWFETs, whereas it is 1.65% and 0.28% for NSFETs with top-bottom and sidewall roughness. Superior roughness performance of NSFETs can be attributed to the fact that in the NSFETs, surface roughness has occurred on a much wider surface. As against this, in the NWFETs, surface roughness is simulated across its smaller cylindrical surface. In Fig. 6, mismatch in ΔV_{thlin} and β for NSFET and NWFET are shown as bar plots. *NS_Total* is the total mismatch contribution of sidewall and top-bottom surface roughness in NSFET. *NS_Total* for uncorrelated LER is given by the following equation [13], [16]:

$$\text{NS\_Total} = \sqrt{\left(NS_{SW}^2 + NS_{TB}^2\right)} \tag{2}$$

where *NS_SW* and *NS_TB* are the mismatch components due to the sidewall and top-bottom roughness respectively in nanosheet. NW refers to the mismatch in the nanowire. It is observed from Fig. 6 that total mismatch in NSFET is approximately equal to mismatch due to top-bottom roughness. Therefore, the mismatch component of sidewall roughness can be neglected. For uniformity and due to the lack of experimental data on NSFET, we have considered

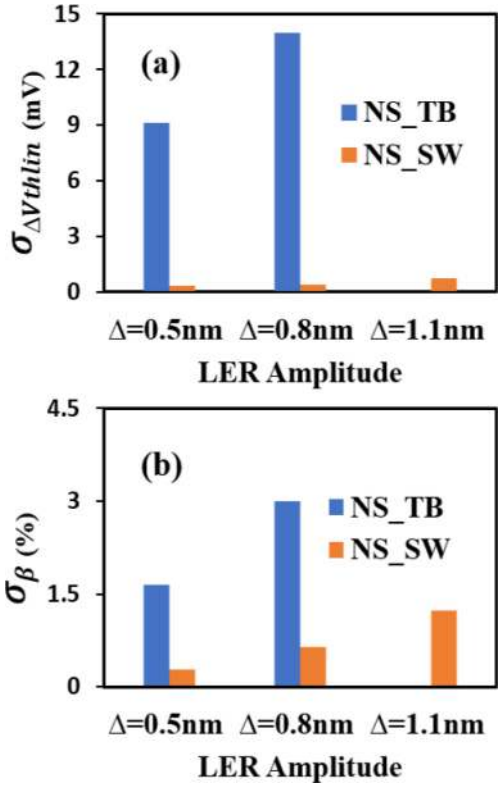

FIGURE 7. Bar plot of 5 nm technology node devices for (a) $\sigma[\Delta V_{thlin}]$ (b) σ_{β} (%), using LER Parameters $\Delta = 0.5$nm to 1.1nm, $\Lambda_x = \Lambda_y = 20$nm, ensemble size = 500 simulations.

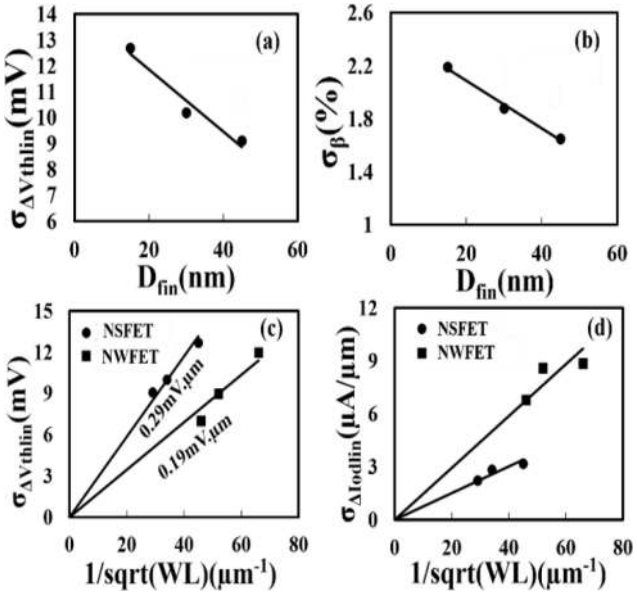

FIGURE 8. Plot of 5nm technology node NSFETs for (a) $\sigma[\Delta V_{thlin}]$ and (b) σ_{β} (%) with varying fin width. Also, Pelgrom plots of NSFET and NWFETs are shown for (c) $\sigma[\Delta V_{thlin}]$ (d) $\sigma[\Delta I_{odlin}]$, using LER Parameters $\Delta = 0.5$nm, $\Lambda_x = \Lambda_y = 20$nm, ensemble size = 500 simulations.

the same roughness along the sidewall as well as the top-bottom surface. However, we have taken a much higher LER amplitude value ($\Delta = 1.1$nm) along NSFET sidewall roughness and compared its matching performances to NSFET with top-bottom roughness for $\Delta = 0.5$nm to 0.8nm, in Fig. 7. Fig. 7 shows that mismatch is found to be lower in σ [ΔV_{thlin}] and σ [β (%)] for NSFET with significantly larger sidewall roughness ($\Delta = 1.1$nm) as compared to mismatch due to top-bottom roughness for $\Delta = 0.5$nm to 0.8nm. Higher mismatch in NSFET with top-bottom roughness can be attributed to smaller fin thickness (Tfin=5nm) [21].

Fin width (D_{fin}) is one of the main design parameters for NSFETs. Fig. 8 (a) and (b) show σ (ΔV_{thlin}) and σ [β (%)] worsen with the reduction of D_{fin}. The reason behind this increase in a mismatch is smaller channel area [16], [21]. We have also carried out a comparison of NSFET and NWFET for different gate channel surface area through Pelgrom plot.

Different device dimensions, such as $D_{fin} = 15$ to 45nm and $L_{gate} = 12$nm for NSFETs were simulated. For NWFETs, we have simulated $D_{nw} = 6$nm and $L_{gate} = 12$ to 25nm. These comparisons are shown in Fig. 8 (c) and (d). From the slope of Pelgrom plot, we can observe that for a given channel surface area, threshold voltage mismatch is higher in NSFET, while the I_{odlin} mismatch is worse for NWFETs. The effective gate length (L) and device width (W) of NS and NW FETs are written as:

$$L = L_{NS} = L_{NW} \tag{3}$$

$$W_{NS} = 2 * (D_{fin} + T_{fin}) \tag{4}$$

$$W_{NW} = \pi * D_{NW} \tag{5}$$

where NS and NW correspond to nanosheet and nanowire respectively. In Pelgrom plot, the origin (x = 0, y = 0) is the point where the device channel area is infinite and mismatch becomes zero [31].

Pelgrom plot slope shows the mismatch in NS/NWFETs with scaling of its channel layout area (Leff*Weff = Aeff) in Fig. 8. Our results in Fig. 6 show that the total mismatch in threshold voltage [$\sigma(\Delta V_{thlin})$] for NSFET ($L_{NS}*W_{NS}$ = 12nm*100nm) is comparable to the $\sigma(\Delta V_{thlin})$ in NWFET($L_{NW}*W_{NW}$ = 12nm*18.84nm). In contrast, mismatch in percentage change in overdrive current σ [β (%)] is significantly higher in NWFET as compared to NSFET. "Aeff" of NSFET is approximately 6X larger as compared to NWFETs for sub-7nm technology node. Pelgrom plot slope exhibits mismatch in NSFET and NWFET for the same "Aeff" and with progressive scaling respectively. Hence, for the same "Aeff " of NW and NSFETs, NSFETS exhibit a higher σ (ΔV_{thlin}) and ultimately leads to a higher slope in Fig. 8 (c). However, mismatch in Iodlin for NSFET is already very low for the sub-7nm node as compared to NWFET, and as a result, for the same "Aeff", NSFET exhibits better matching in Iodlin and finally leads to a lower slope in Fig. 8 (d). From the results, it can be concluded that σ (ΔV_{thlin}) is more dependent on variation in fin thickness (Tfin = 5nm) /diameter (Dnw = 6nm)

TABLE 3. Comparison of mismatch in electrical properties of NWFET (Dnw = 6nm) and NSFET (Dfin = 45nm) for different LER amplitudes.

Device	NSFET/NWFET	NSFET/NWFET
Electrical Parameters	Amplitude of LER	
	Δ=0.5nm	Δ=0.8nm
$\sigma(\Delta V_{thlin})$ in mV	9.10/11.92	14.32/16.33
$\sigma(\Delta V_{thsat})$in mV	14.00/15.30	22.20/20.60
$\sigma(\Delta I_{dlin})$ in µA/µm	2.24/9.60	3.94/13.96
$\sigma(\Delta I_{dlin}/\overline{I_{dlin}})$ in %	1.70/6.81	3.03/10.36
σ (ΔIon) in µA/µm	22.75/ 35.83	35.19/48.0
$\sigma(\Delta I_{on}/\overline{I_{on}})$ in %	5.53/9.13	8.84/12.88
$\sigma\{\Delta \log_{10}(I_{off})\}$ in pA/µm	0.22/0.26	0.33/0.34
$\sigma\{\Delta \log_{10}(I_{off})/\overline{\log_{10}(I_{off})}\}$ in %	5.86/10.16	9.00/13.52
σ (ΔDIBL) in mV	5.11/3.41	8.12/4.41
σ (ΔSS) in mV/dec	1.59/0.93	2.89/1.29

of NS/NWFET, while σ (ΔI_{odlin}) depends more on fin width [20], [21], [32].

V. 3-D LER EFFECTS ON GATE CONTROL AND MOBILITY

Gate control and mobility are the other important aspects that are also affected by LER induced mismatch. Gate control can be investigated by the mismatch in drain induced barrier lowering [σ(ΔDIBL)] and subthreshold slope [σ(ΔSS)], while mismatch in mobility can be analyzed by a mismatch in drain current in linear σ (ΔI_{dlin}) and saturation region [σ (ΔI_{on})]. Here DIBL is defined as the difference between threshold voltage in saturation and linear region, while I_{on} is the current extracted at $V_{DD} = 0.7V$.

It is important to evaluate mismatch in electrical parameters of NSFET and NWFETs for the different amplitude of LER value (Δ) [17], [31]. From Fig. 9 (a) and (b), it is found that σ (ΔDIBL) and σ (ΔSS) is lower in NWFET in comparison to NSFET due to the cylindrical nature of NWFET, which provides better gate control on the channel, while in NSFET, larger Fin width and rectangular channel cross-section cause degradation in its subthreshold slope and gate control [4]. In earlier work, it was reported that mismatch in DIBL and SS are lower in NWFET compared to rectangular FinFET structure [20]. Smaller T_{fin} (5nm) in NSFET may result in more confinement in the channel compared to D_{nw} (6nm) of NWFET. As a result, mismatch in DIBL and threshold voltage are worsened in the saturation region. From the analysis, it is also found that LER induced mismatch on threshold voltage and current will be dominant at larger drain bias voltage. At higher drain bias voltage, short channel effects become dominant due to lower gate control over the channel. It aggravates the mismatch in ON current and threshold voltage at higher drain bias and at the higher amplitude of roughness [14].

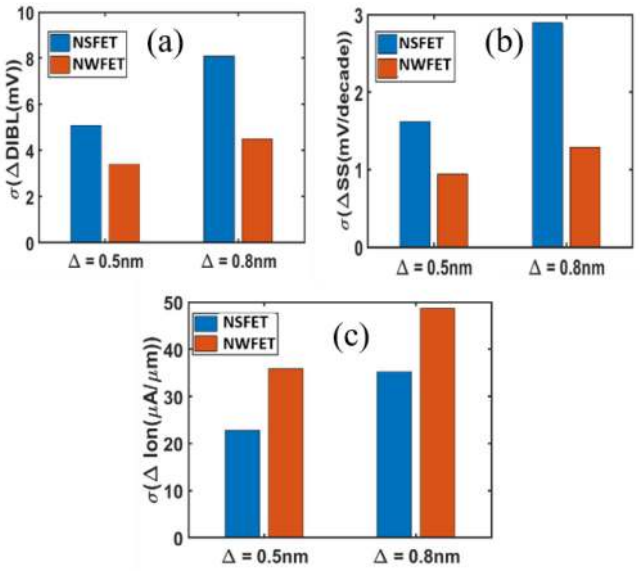

FIGURE 9. Bar Plot of 5nm technology node devices for (a) σ[Δ*DIBL*], (b) σ[Δ*SS*] and (c) σ[Δ*Ion*], using LER Parameters Δ = 0.5nm and 0.8nm, $\Lambda_x = \Lambda_y$Λ20nm, ensemble size = 500 simulations.

Fig. 9 (c) exhibits mismatch in current in the saturation region. Mismatch in current is found to be lower in NSFET as compared to NWFET, which may imply that LER induced mismatch in mobility is less in NSFET as compared to NWFET due to the large surface and rectangular channel cross-section of NSFET. Matching performance of NSFET with roughness along all the four faces of the channel is extracted and compared with NWFET for LER amplitudes of 0.5nm and 0.8nm in Table 3. From the results, it is observed that mismatch in NSFET and NWFET electrical characteristics are degraded more at higher surface roughness amplitude. Mismatch in threshold voltage at saturation degrades more in NSFET due to larger σ(ΔDIBL) at higher drain bias voltage with a large amplitude of surface roughness. It is found that as compared to NWFET, σ(ΔDIBL) in NSFET is 1.5X and 1.84X larger for $\Delta = 0.5$nm and $\Delta = 0.8$nm respectively. Similarly, Matching performance of σ (ΔSS) at $\Delta = 0.8$nm ($\Delta = 0.5$nm) in NWFET is found to be 2.24X (1.69X) better than that of NSFET. Similar observations were also made in previous reports in the context of a comparison of mismatch in NWFET and Fin FET [20].

VI. IM/JL FETS MATCHING PERFORMANCE

LER induced mismatch is also affected by channel doping concentration [29]–[30]. NS/NW-FETs are designed and compared for different channel doping concentrations, such as inversion (IM) and junctionless (JL) doping in this article [18], [30]. For nanoscale FET design, JL devices are a potential replacement for conventional and IM FETs [30], [31]. JL devices have many advantages over IM FETs, such as simple fabrication process, larger drive current, and feasibility of doing short channel length design [30].

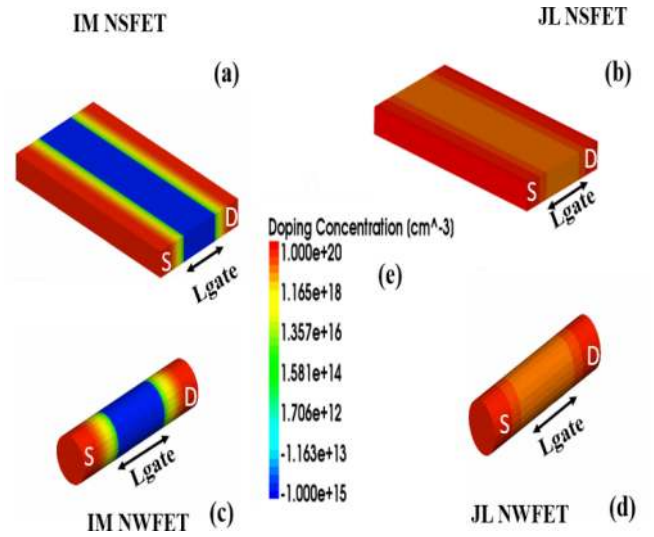

FIGURE 10. 3-D cross-section of FET devices (a) IM NSFET, (b) JL NWFET with Lgate = 12nm, Dfin = 45nm, and Tfin = 5nm, (c) IM NWFET, (d) JL NWFET with Lgate = 12nm, and Dnw = 6nm, and (e) doping profile along channel current direction.

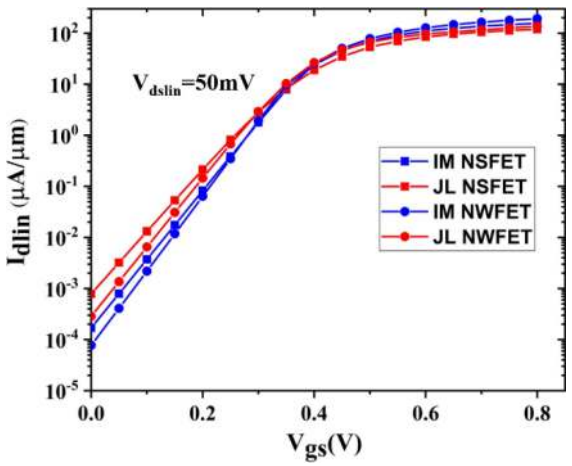

FIGURE 11. Id vs Vgs simulated curve in linear region for IM/JL NSFET (Lgate = 12nm, Dfin = 45nm, and Tfin = 5nm) and IM/JL NWFET (Lgate = 12nm, Dnw = 6nm).

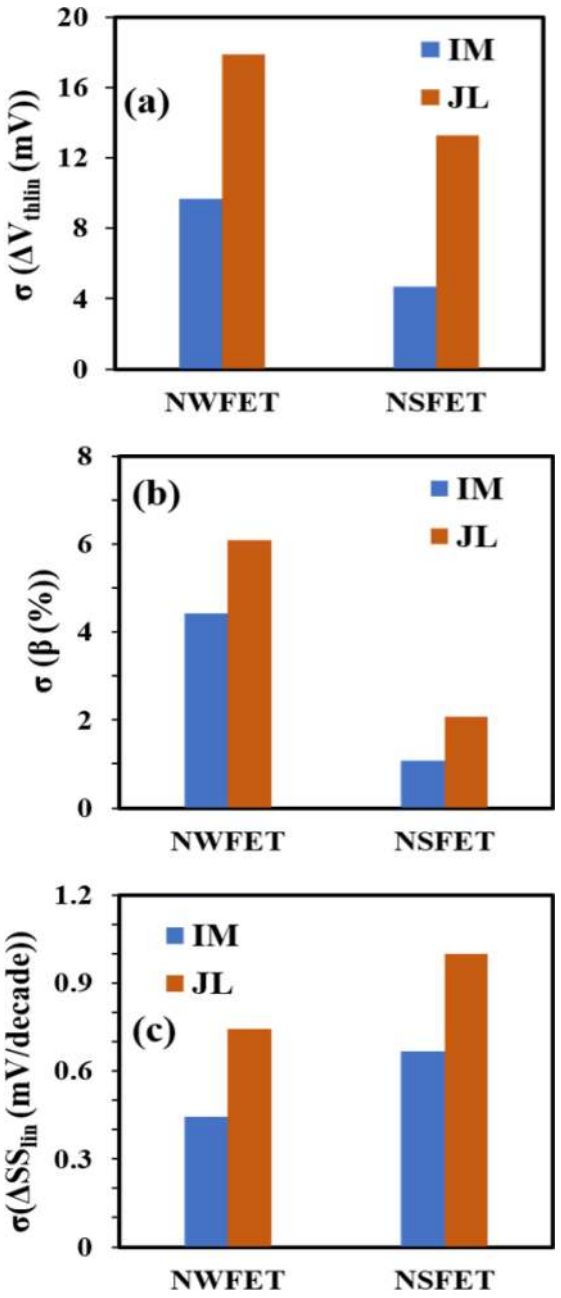

FIGURE 12. Bar plot of 5 nm technology node devices for (a) σ [ΔV_{thlin}] (b) σ_β (%), and (c) σ[ΔSS_{lin}] using LER Parameters Δ = 0.5nm, $\Lambda_x = \Lambda_y$ = 20nm, ensemble size = 500 simulations.

However, shorter channel length design and higher doping in JL devices make it more susceptible to process-induced variation [31]. Mismatch in Vth and Ion due to LER can lead to more change in delay and switching frequency of circuits comprising millions of transistors [18]. Thus, it is important to perform extensive and correct LER analysis on IM/JL NSFET for state-of-the-art CMOS design.

3-D cross-section of IM/JL MuG-FETs and corresponding doping profiles along channel current direction are shown in Fig. 10.

For a fair comparison, the threshold voltage in the linear region of all devices is matched by tuning metal gate work function as reported in [31]. It is observed from Fig. 11 that the subthreshold slope (SS) is better for NWFET due to its cylindrical gate all around structure, compared to NSFET with larger rectangular FinWidth (D_{fin}). As a result, NWFET exhibits better gate control compared to NSFET. SS is also found to be lower in IM devices compared to JL devices as reported earlier in [30]. LER induced mismatch of IM/JL MuG-FETs is compared for r.m.s. surface roughness, Δ = 0.5nm and correlation length, $\Lambda_x = \Lambda_y$ = 20nm [17], [31]. It can be seen from Fig. 12 (a) and (b) that σ (ΔV_{thlin}) and σ [β (%)] exhibits a higher mismatch in JL NS/NW-FET compared to its IM devices. It is observed that as compared to JL NS/NW-FETs, IM NS/NW-FETs exhibit nearly 2X better σ (ΔV_{thlin}) matching performance.

Similarly, matching the σ (β (%)) in IM NS/NW-FETs, it is found to be 1.5X better than its equivalent JL mode design. The main reason behind the higher mismatch in σ (ΔV_{thlin}) is the threshold voltage (Vth) sensitivity dependence on channel doping [30]. Threshold voltage sensitivity increases with higher doping concentration in the channel as reported earlier, therefore larger mismatch occur in JL devices compared to IM devices [31]. Leung and Chui also stated that conducting layer formation along the channel in JL FETs also accelerates mismatch in electrical characteristics due to LER [30], [31].

Since, larger potential barrier is found in IM FETs due to source /drain channel junction compared to JL FETs, potential barrier in IM FETs is not affected as much as in JL FET by body thickness variations induced due to LER. Thus, as a result, IM FETs exhibit lower mismatch compared to JL FET devices. Fig. 11 (c) also shows that LER induced mismatch in subthreshold slope ($\sigma(\Delta$SSlin)) of IM MuG-FETs is 1.51X lower than JL mode devices. Lower $\sigma(\Delta$SS) in IM devices is attributed to better gate control compared to JL devices. Moreover, JL/IM NWFET depicted a lower mismatch in $\sigma(\Delta$SSlin) due to its GAA structure in comparison to larger Fin and rectangular structure in JL/IM NSFET as explained earlier [6], [22].

VII. CONCLUSION

We have compared the impact of LER on contemporary FET architectures for sub-7nm CMOS nodes using a 3-D roughness model. In this analysis, it is observed that with only sidewall roughness component, NSFET shows minimal or negligible mismatch in current and threshold voltage when compared to NWFET. We attribute this superior matching performance of NSFET to its favourably small ratio of rough sidewall width to the total channel width. Even when roughness is considered along all the sides of NS FET channel, the current mismatch is found to be lower in NSFET as compared to NWFET. The drain current matching performance of NSFET in the linear region is found approximately 4X better, while at saturation drain bias, it shows 1.65X improvement over NWFET. As compared to NWFET, the superior drain current matching performance of NSFET could be due to occurance of roughness on much larger channel surface area of the nanosheet, which is consistent with Pelgrom's law. However, as compared to NSFET, the NWFET exerts stronger gate control over the channel. Hence, NW FET exhibits 1.5X better matching performance for short channel effect related parameters, such as DIBL and SS. IM FETs show better matching performance compared to JL FETs, owing to larger potential barrier between source/drain and channel junction. As a result, IM FETs exhibit more immunity against 3-D LER induced thickness variation. It is observed that JL NS/NW-FETs show nearly 2X more mismatch in threshold voltage and drain current in linear region against 3-D LER compared to IM NS/NW-FETs.

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