Comparison of Opamp-Based and Comparator-Based Delta-Sigma Modulation

Massoud Momeni Petru Bogdan Bacinschi Manfred Glesner

Technische Universität Darmstadt
Department of Electrical Engineering and Information Technology
Institute of Microelectronic Systems
Karlstraße 15, D-64283 Darmstadt, Germany
{momeni,bacinschi,glesner}@mes.tu-darmstadt.de

Abstract

Comparator-based switched capacitor (CBSC) circuits present an alternative approach to designing sampled data systems based on the principle of detecting a virtual ground condition with a comparator rather than actively enforcing it with a high-gain operational amplifier (opamp) in feedback. This work demonstrates a 2^{nd}-order $\Delta\Sigma$ converter designed using the CBSC technique. The same modulator topology was also implemented using two conventional design methods for a two-stage Miller-compensated amplifier and a single-stage folded cascode amplifier, such that all three blocks can be used as 'drop-in replacements' in the top-level circuit. The designs are done in a 0.13 μm UMC technology. The SNDR performance and power consumption of all three approaches were simulated with a sampling frequency of 5.12 MHz and an oversampling ratio of 64. It can be concluded that the CBSC method provides a great simplification of design effort and significant power savings compared to the traditional OTA-based methods.

1. Introduction

Technology scaling is driven by the incentive of digital signal processing, enabling ever faster processors and ever greater digital functionality per mm^2 of die area. For the past few decades, technology has scaled in accordance to Moore's Law, roughly doubling the number of transistors per chip area every 18 months and the qualitative nature of the observation still holds. Also, the supply voltage decreases with decreasing feature size [6]. These trends are mainly being driven by the enormous speed and power improvements possible in digital circuits and the enormous demand for high speed, low power applications such as handheld wireless communication and multi-media devices.

However, the indispensable analog interface to the real world becomes the bottleneck in system performance, thus driving up the demands from it. Also, since the area occupied by analog circuits scales much less readily than that occupied by digital circuits, they also limit area savings as technology scales further down. In analog circuits whose performance is limited by thermal noise, the scaling of supply voltage reduces the voltage range, thus increasing capacitor sizes for the same dynamic range. In order to keep the speed of the circuits unchanged, in turn, the circuits need to consume more current - either due to increased transconductance or increased slew rate needed to drive the higher capacitances [8]. Low power, low voltage technologies require multi-stage amplifiers in order to maintain the voltage gain while keeping the speed constant under reduced available swing.

Analog switched capacitor circuits invariably use OTAs connected in negative feedback. Their performance calls for a high voltage gain. This introduces the issue of stability into the design. Compensation, a technique used to overcome this problem, is a major design effort against stability and invariably also entails an increase in power consumed.

In [7], a methodology was reported that completely eliminates in a switched capacitor circuit and employ comparators, which can be designed with high speed and high gain, using multiple stages without worrying about stability. The virtue of comparator-based switched capacitor (CBSC) circuits lies therein that they use a comparator to detect the virtual ground in a feedback configuration and then correct for the loss of virtual ground using constant current sources charging or discharging the load. This process occurs only once per cycle and hence the virtual ground condition is not actively enforced as in the case of an OTA-based switched capacitor circuit. In doing this, we take advantage of the fact that in a sampled-data analog system the value of the voltages at the output of each stage has to be accurate only at the sampling instant, and the means of reaching that value

978-3-9810801-3-1/DATE08 © 2008 EDAA

play no role. Since we only detect the virtual ground once, we may also save considerable power by simply switching off the CBSC unit during the remainder of the cycle.

This work proposes the application of the CBSC technique to design a differential second-order delta-sigma modulator, and compare its performance with similar modulators designed using conventional OTAs. All three architectural approaches—CBSC methodology, two-stage Miller-compensated OTA and single-stage folded cascode OTA—are compared in terms of signal-to-noise-and-distortion ratio (SNDR) and power consumption.

2. Comparator-based Switched Capacitor Circuits

2.1. Single-ended CBSC Configuration

The CBSC gain stage [7] shown in Fig. 1 consists of a comparator which senses the loss of virtual ground at the input, followed by a logic unit which generates control signals E1, E2, S, and P. These are applied to two current sources, I_1 and I_2. The operation of the circuit during the sampling phase is identical to that of an OTA-based SC gain stage. During the charge transfer phase, a small preset pulse is applied to the output, connecting it to the lowest voltage in the circuit. This is followed by a coarse charge transfer phase E1 and a fine transfer phase E2.

Due to the preset, the virtual ground node, V_x, starts below the common-mode voltage, V_{cm}, tripping the comparator. The logic unit generates E1, and current source I_1 charges up the output until the virtual ground equals the common-mode voltage. At this time, the comparator trips again, while the output charges up higher than required due to the finite comparator delay. The logic then generates the signal E2, and current source I_2 discharges the output correctively, until the virtual ground node crosses common mode again, this time in the opposite direction. At that point, sampling switch S opens, and the correct value is sampled on the load capacitor (which is the sampling capacitor of the next stage). Following this, the signal E2 and current source I_2 may return to zero slowly, since the sampling has already been done. The output is slightly below the ideal value due to the comparator delay. This produces a constant signal-independent undershoot each cycle.

Thus, we take advantage of the fact that we need to reach the correct output value only at the sampling instant, regardless of how it reaches there. This enables us to detect the virtual ground thereby eliminating the OTA and feedback amplifiers for which we would have to deal with issues of speed, linearity, gain, and stability. The price to be paid is the final undershoot, which, however, does not pose a serious problem if kept within small limits. This effectively places a speed requirement on the CBSC comparator, but

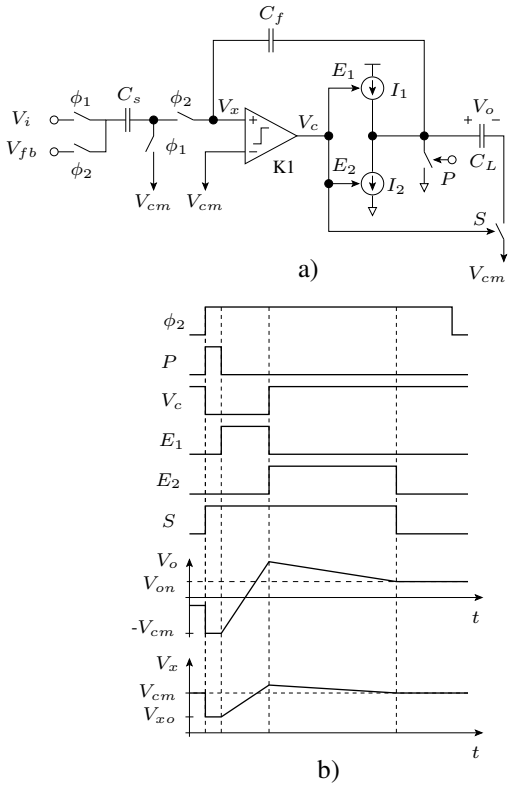

Figure 1. Simplified single-ended CBSC gain stage (CBSC logic unit not shown). a) Charge transfer circuit and b) timing diagram.

we can design a comparator with lower current consumption which can be switched off for a large part of the cycle thereby saving power when compared to the OTA.

2.2. Differential CBSC Gain Stage

Differential circuitry has several important advantages over single-ended circuitry, such as higher immunity to noise sources, an increase in maximum achievable signal swings, higher linearity, and lower distortion. For these reasons, we have developed a differential version of the single-ended CBSC gain stage in Fig. 1, which is shown in Fig. 2.

Two current sources are used, each for I_1 and I_2 in order to achieve a differential output voltage. The currents charge their unit of the load capacitor in opposite directions, such that both input nodes of the comparator meet 'halfway' at the common-mode point. It is essential to match the two I_1 and the two I_2 current sources to ensure equal rate of charging and thus control this common-mode point.

The logic block of the CBSC unit takes the clock, preset, and comparator as inputs and generates the signals E1, E2, and S, which control the coarse charging, fine charging, and sampling operation of the charge transfer phase, respec-

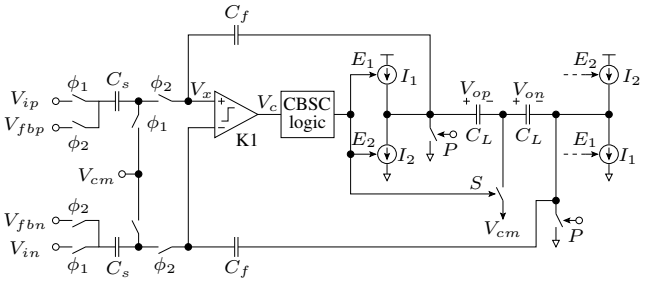

Figure 2. Differential CBSC gain stage.

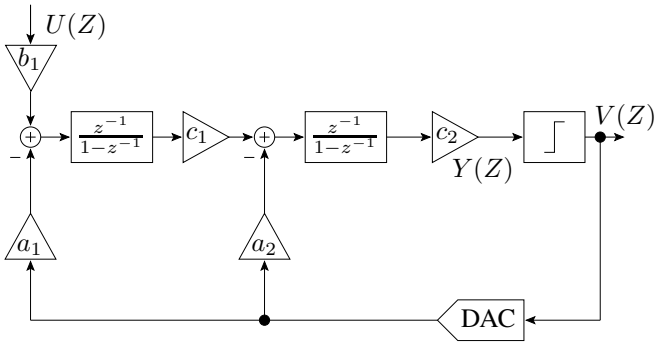

Figure 3. Linearized block diagram of the Boser-Wooley Modulator.

tively. These signals are generated from an asynchronous state machine. Such a state machine is essential in order to generate the signals only once even though the comparator may trip more than once. Also, the sequence of their generation is important, as is the fact that E1 and E2 should be non-overlapping for a clean operation.

In the following, the differential CBSC unit gain stage in Fig. 2 is used in a 2^{nd}-order $\Delta\Sigma$ modulator.

3. System and Circuit Design

3.1. Modulator Topology

The modulator chosen to compare the three architectural approaches has a second order single-bit single-loop architecture containing two delaying integrators, known widely as the Boser-Wooley Modulator [1] and shown as a block diagram in Fig. 3.

Delaying integrators enable us to use a clocking scheme which allows each integrator to settle independently of the other in half a clock cycle [3]. The clocking scheme is chosen such that the delaying integrators pipeline correctly. The coefficients a_1, a_2, b_1, c_1, and c_2 are computed by Schreier's Delta-Sigma Toolbox [4]. After proper scaling and denormalization of the signals, the block diagram is then translated into a practical circuit for the $\Delta\Sigma$ modulator.

3.2. Circuit Implementation

For reasons already indicated in Section 2.2, a fully-differential architecture was chosen for the implementation of the modulator. Important advantages in doing so are the cancellation of all even-order distortion terms (harmonic and intermodulation), regardless of the cause of the distortion, reduced clock feedthrough and charge injection due to switching, higher linearity, and increased dynamic range. The modified version of the 2^{nd}-order modulator using differential CBSC gain stages is shown in Fig. 4.

On the first phase of the clock, the input is sampled onto capacitor C_{s1}, while the amplifier holds the previous state on the feedback capacitor. In the charge transfer phase, the difference between the input and reference is integrated onto feedback capacitor C_{f1}. Since the coefficients are equal for the signal and the feedback path, their sampling capacitance C_s can be shared. The clocking scheme is chosen such that the input switch opens slightly later than the common-mode switch. Thus, the particular issue of signal-dependent charge injection is alleviated.

The D/A operation through the capacitors is inherently linear. The first DAC and the first integrator in the modulator are critical since their distortion and noise appear directly at the output of the modulator without attenuation. The OTA in the integrator must provide a high gain to avoid shifting of the poles and transfer function (integrator leakage) and must be sufficiently linear. The two-stage Miller architecture provides a high gain and high swing at the cost of higher power consumption. The folded cascode architecture provides a high gain at moderate power consumption, but has limited swing. To maintain the same dynamic range, the capacitance size needs to be increased (due to thermal noise considerations), thus increasing the bandwidth and slew requirements. Effectively, we end up increasing power consumption again.

Miller amplifier: The two-stage OTA, as shown in Fig. 5, consists of a fully-differential first stage with high common-mode rejection and a Class A second stage. This architecture provides a high DC gain with a large output swing. However, the presence of a significant non-dominant pole creates stability issues, requiring a large Miller compensation capacitance. The Miller compensation produces pole-splitting, pushing the pole due to the load capacitance to a higher frequency, and introducing a low frequency pole from the compensation capacitance.

Finite DC gain of the OTA results in a shift of the poles of the integrator, resulting in a change of the noise transfer function (NTF) and a degraded attenuation of quantization noise in the signal band. A gain equal to the oversampling ratio (OSR) should normally be sufficient to ade-

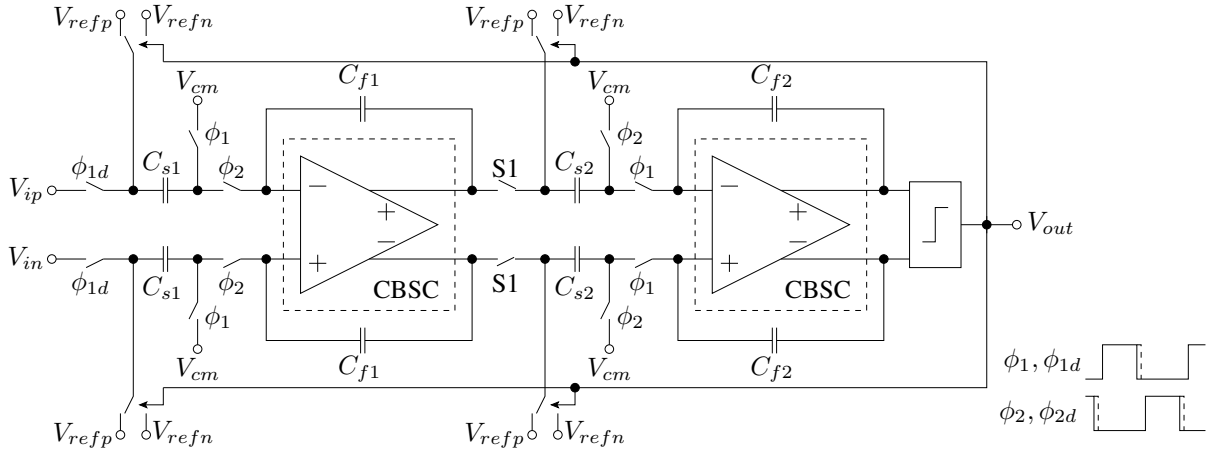

Figure 4. Switched-capacitor implementation of the second-order CBSC $\Delta\Sigma$ modulator (simplified illustration) and clocking scheme.

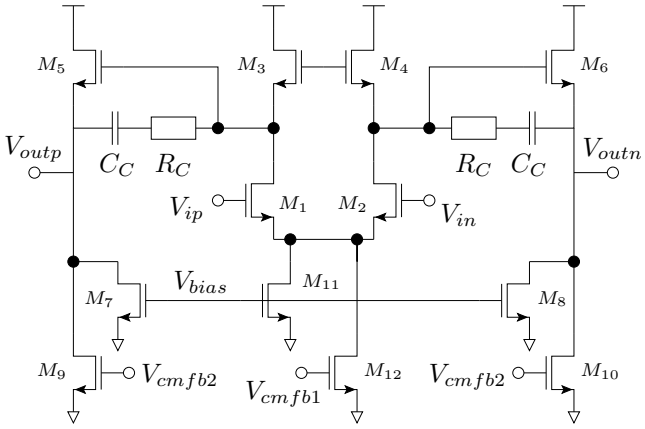

Figure 5. Two-stage Miller OTA (common-mode feedback and bias circuit not shown).

quately suppress this problem, under the assumption of linearity. However, the gain of the OTA is nonlinear due to the voltage-dependent nature of the device operating points, producing distortion in the integrator output [5]. The mechanism of nonlinear gain is complicated, making it difficult to model accurately. Nonetheless, its adverse impact can be limited by designing an OTA wih a high DC gain [2, 5]. The two-stage Miller OTA uses long channel lengths for the transistors, achieving a large output resistance and a DC gain that is high enough to ensure a finite but very small gain error, which is fairly signal-independent.

The settling behaviour of the OTA in capacitive feedback may be divided into two distinct regions: slewing and linear settling. Assuming that the input differential pair is able to provide an output current as large as needed by feedback, the output will rise exponentially towards its final stable value. Nevertheless, in the presence of large input step-changes, the tail current limits the output current capability of the OTA, and it can only charge the output through the compensation capacitor as a constant current source. When the output has charged sufficiently, the input voltage becomes small enough for the tail current to accommodate the g_m-defined output current and the OTA begins to settle exponentially (linear behaviour). The tail current should be designed such that the OTA has a large portion of the half-clock cycle in order to settle linearly, while limiting the effect of nonlinear slewing on the final output.

Folded-cascode amplifier: The two-stage Miller compensated OTA solves the gain problem by using two stages of amplification. This introduces a stability issue, which is solved by means of Miller compensation. But, this is expensive in terms of power consumption. Another high gain alternative is a cascode topology. However, the telescopic cascode is immediately ruled out in a very low voltage design. Here, we use a folded cascode architecture, which is a compromise between the low swing, low power telescopic cascode, and the high swing, high power two-stage design. The folded cascode circuit shown in Fig. 6 is a single-stage design with a load-compensated frequency response and an output swing reduced by two overdrive voltages compared to the two-stage design. However, it has a larger swing compared to a telescopic cascode. The DC gain, linearity and settling requirements are similar to those for the Miller OTA.

CBSC comparator: The CBSC comparator, shown in Fig. 7, uses an architecture with three low gain, high bandwidth fully-differential stages using PMOS resistor loads, followed by class A output stages. By using this configuration, we take advantage of a multi-stage architecture,

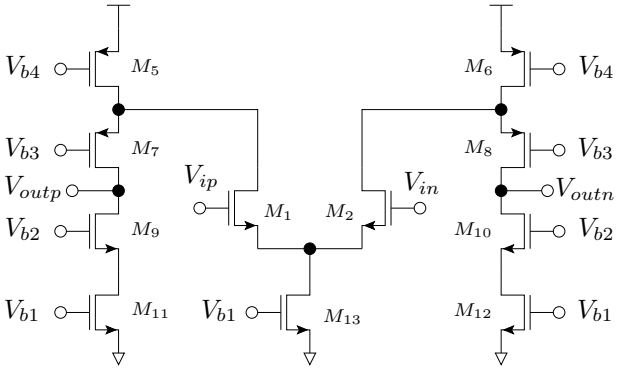

Figure 6. Folded cascode OTA (common-mode feedback circuit not shown).

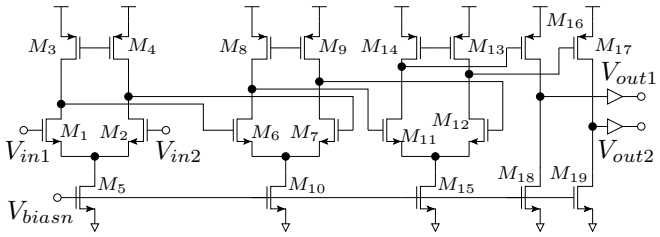

Figure 7. Comparator used in the CBSC stage (bias circuit not shown).

eliminate the stability problems associated with multi-stage OTAs, and can thus increase the gain to a large enough value. The speed of the comparator has been maximized by keeping all parasitic capacitances loading the signal path as small as possible and thus reduce the undershoot of the CBSC stage output voltage. The final state shifts the comparator to nearly rail-to-rail values, and the digital buffers at the output provide logic voltage levels.

Summary: It is a tremendous challenge to design an amplifier with a large enough and relatively stable gain, which is fast enough to settle within the required resolution in the given time and consumes a small current. On the other hand, the CBSC methodology enjoys several advantages. The linearity and DC gain requirements are rolled up into just one signal-independent parameter: the output offset at the end of settling. This shows up as a DC value at the output of the modulator which is easily taken care of. Since the exact nature of settling is not important in our case as long as the final value at the sampling instant is correct, we are not constrained by maintaining linearity constraints.

The comparator gain can be made extremely high by using multiple stages of amplification since we are not limited by stability problems. The transconductance and slew rate of the OTA have to be large enough to supply the necessary current under the given settling constraints. In the case of CBSC circuits, we only need to ensure that the comparator delay is within a limit imposed by the amount of tolerable undershoot. This delay can be made very small. Also, since the CBSC comparator is active for only a fraction of a cycle, we can also save power during the inactive phase. This is not possible in an OTA, which requires some slewing time as well as all of the remaining half clock phase for settling. The CBSC methodology thus demonstrates a significant reduction in design effort as well as power savings.

4. Results and Discussion

All three modulators designed here were simulated with a sampling frequency $f_s = 5.12$ MHz, an OSR = 64, and an input frequency of $f_{in} = 32$ kHz. The Nyquist rate is 40 kHz, which means that the simulation was performed at a relatively high frequency. Figs. 8, 9, and 10 show the power spectral density (PSD) of the three architectures, as well as the expected plot computed by the Delta-Sigma MATLAB Toolbox [4]. The input amplitude in these cases is -6 dBFS.

In order to compute the power spectral density of the modulators, their output was processed with a Hann window to minimize noise leakage and, for the FFT, the number of samples was chosen as 4096 based on accuracy and repeatibiliy specifications in estimating a signal-to-noise-ratio and observing a sufficiently reliable, spurious-free dynamic range (SFDR) [5]. Also, to avoid spectral signal leakage, the input has been placed exactly at a frequency bin.

It can be seen that all three simulation approaches yield results very close to the theory.

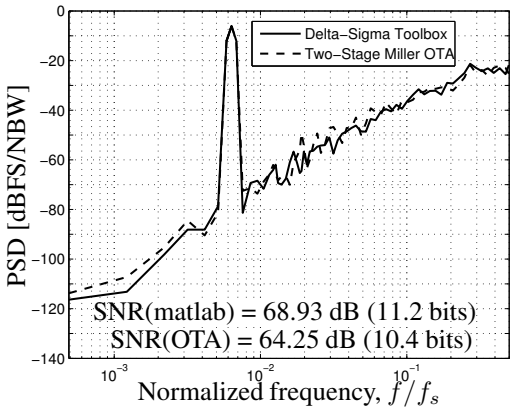

Figure 8. $\Delta\Sigma$M PSD with Miller OTA.

The current consumptions of the three modulators from a 1.2 V supply are shown in the Fig. 11. As can be seen, the CBSC approach provides a great saving in power, as can be seen from the fact that both the total power as well as the integrator-share of the total power decrease dramatically.

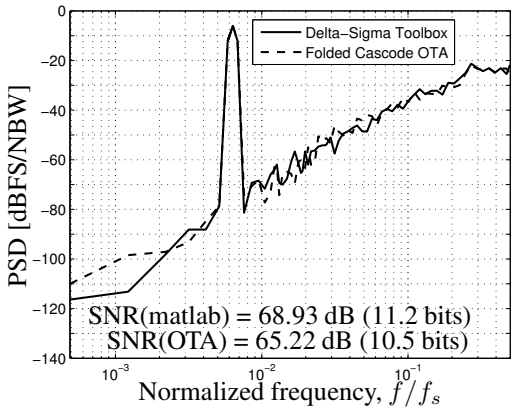

Figure 9. $\Delta\Sigma$M PSD with folded cascode OTA.

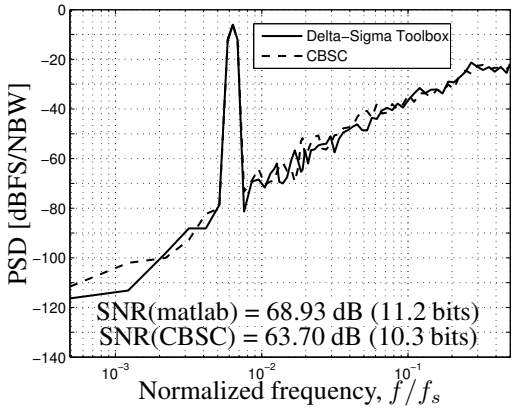

Figure 10. $\Delta\Sigma$M PSD with CBSC gain stages.

The power optimization bottleneck thus shifts significantly away from the integrators, without a loss of performance as can be seen from the SNDR values in Figs. 8, 9, and 10.

5. Conclusion

This work proposes a differential second-order delta-sigma modulator based on the CBSC technique. The output of the CBSC stage contains an input-independent DC undershoot. In case of a delta-sigma converter, the DC undershoot from the first integrator appears directly at the output of the modulator. The value of this undershoot is predictable a priori since we know the values of the current sources, the load capacitor and the comparator delay, at least to a reliable accuracy. Jitter and offset voltages are additional factors that affect the accuracy of the output. However, offset voltages due to device mismatches and jitter due to the statistical uncertainty of threshold detection both lead to errors that are signal independent. While the former can be

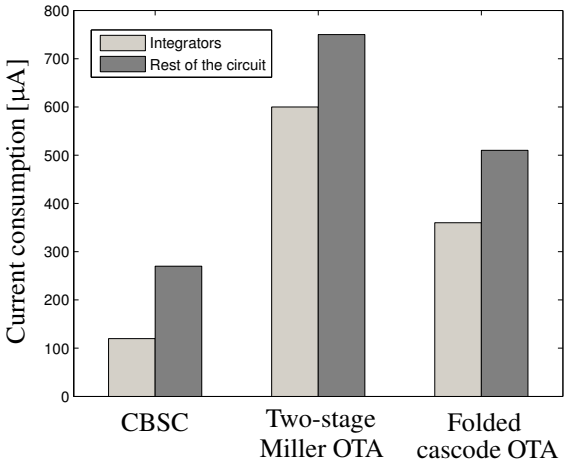

Figure 11. Current consumption comparison.

corrected, the latter is a fundamental limit of accuracy.

Due to the transient nature of a CBSC circuit, thermal noise analysis is not as straightforward as in the case of amplifiers. Further investigation needs to be done in the areas of distortion and effects of pattern noise due to DC components.

In summary, the CBSC approach promises a great power, area and design effort advantage over conventional switched capacitor implementations of delta-sigma modulators as shown by this work.

References

[1] B. Boser and B. Wooley. The design of sigma-delta modulation analog-to-digital converters. *IEEE Journal of Solid-State Circuits*, 23(6):1298–1308, Dec 1988.

[2] B. Brandt, P. F. Ferguson, and M. Rebeschini. *Analog circuit design for $\Delta\Sigma$ ADCs*, chapter 11, pages 333–379. Wiley-IEEE Press, Hoboken, NJ, 1997.

[3] R. Gregorian and G. C. Temes. *Analog MOS Integrated Circuits for Signal Processing*. Wiley-Interscience, 1986.

[4] R. Schreier. $\Delta\Sigma$ Toolbox. MATLAB Central File Exchange.

[5] R. Schreier and G. C. Temes. *Understanding Delta-Sigma Data Converters*. Wiley-IEEE Press, Hoboken, NJ, 2005.

[6] Semiconductor Industry Association. *The International Technology Roadmap for Semiconductors*. 2006.

[7] T. Sepke, J. K. Fiorenza, C. G. Sodini, P. Holloway, and H.-S. Lee. Comparator-based switched-capacitor circuits for scaled CMOS technologies. In *Proc. IEEE International Conference Solid-State Circuits*, volume 49, pages 220–221, Feb 2006.

[8] M. Waltari. *Circuit Techniques For Low-Voltage And High-Speed A/D Converters*. PhD thesis, Helsinki University of Technology, Department of Electrical and Communications Engineering, Electronic Circuit Design Laboratory, Helsinki, Finland, 2002.