Comparison of Raised and Schottky Source/Drain MOSFETs Using a Novel Tunneling Contact Model

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Abstract

We present, for the first time, a physical contact tunneling model that is critical for studying the increasingly important contact behavior in future scaled CMOS. The tunneling processes are self-consistently treated with all current transport in the semiconductor. With this new model, we compared the performance of raised S/D and Schottky S/D MOSFETs. Both raised S/D and Schottky S/D MOSFETs can be designed to give good short-channel characteristics. Our analyses show that despite the lower sheet resistance of the Schottky S/D MOSFETs, contact resistance could be large due to finite Schottky barrier height. A lower barrier height contact material should be used to minimize the contact resistance.

Introduction

Raised source drain MOSFETs [1] and Schottky source drain MOSFETs [2] (see Fig.1) are two candidates for high performance CMOS that can be scaled down to 25 nm with low series resistance.

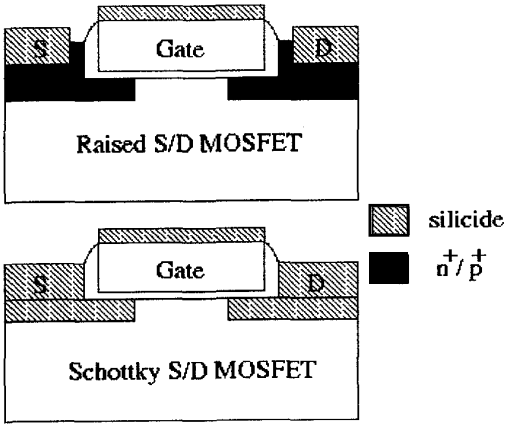

Figure 1: Raised S/D and Schotky S/D MOSFET.

The contact between silicide and silicon is an important component of these small MOSFETs, because the contact resistance constitutes a significant fraction of the total resistance in the path of the drain current [3]. It has been demonstrated that the contact resistance can be very sensitive to the silicide thickness due to the difference in interface doping [3] (also see Fig. 2).

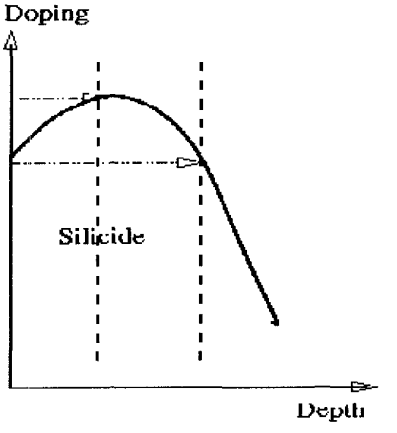

Figure 2: Effect of silicide thickness on interface doping. The contact resistance can be severely impacted by low interface doping.

A realistic, physical tunneling contact model in a CAD based device simulator is crucial for accurately assessing the effects of technology parameters on the performance of these small MOSFETs. Since tunneling occurs only within about 20 nm of the silicide/silicon interface, the contact is often modeled by an equivalent (lumped or distributed) resistor, by the velocity-limited boundary conditions[4], or by using the current boundary conditions with current calculated by summing all tunneling current over the entire energy spectrum [5]. However, for MOSFETs less than 50 nm, this assumption is clearly unacceptable because the tunneling distance is comparable to the channel length. The electrons and holes in the channle region

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can be directly exchanged with the Silicide through tunneling. In this paper, we report, a novel tunneling contact model where all tunneling processes are self-consistently treated with all current transport in the semiconductor. We apply the model to compare raised S/D and Schottky S/D MOSFETs.

Model

The key feature of the model is that tunneling current through the barrier is converted into a local generation or recombination process where the local rate, $G_{Tun}(r)$, depends on the local Fermi-level, ϕ_n and the potential profile along the tunneling path. This is possible because the tunneling integral over distance and energy can be transformed into a double integral over distance alone (see Fig.3).

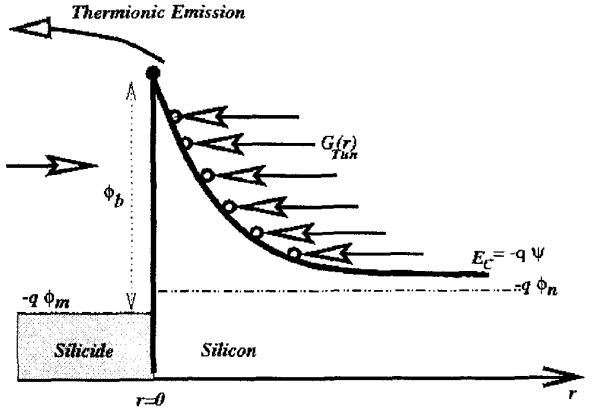

Figure 3: Nodal equivalent generation rate due to tunneling at the contact.

For each contact node, a tunneling path is extracted from the 2D/3D spatial domain using a carefully constructed mesh (see Fig. 4). The local generation rate associated with the tunneling can be related to the local tunneling current, J_{Tun}, as

$$\begin{aligned} G_{Tun}(r) &= \frac{1}{q}\nabla \cdot J_{Tun} \\ &= \frac{1}{q}\frac{dJ_{Tun}}{d\psi}\cdot\nabla\psi \\ &= \frac{dJ_{Tun}}{d\varepsilon}\cdot\vec{E}, \end{aligned} \tag{1}$$

where $\psi, \varepsilon = -q\,\psi$, and $\vec{E} = -\nabla\psi$ are the electrostatic potential, the energy level, and the electric field, respectively. The total tunneling current from Silicon to Silicide

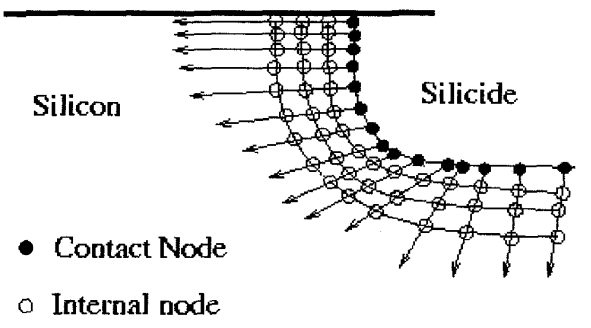

Figure 4: Two-dimensional mesh and tunneling paths. Electrons and holes in the vincinity of the contacts can be tunnelled in and out.

can be expressed as,

$$J_{Tun,S-M} = A^*T^2 \int_{\varepsilon}^{\infty} \Gamma(r) \quad \ln\left[\frac{1}{1+\exp((\varepsilon'-E_{Fn})/k_BT)}\right] d\varepsilon', \tag{2}$$

and the total tunneling current from Silicide to Silicon can be expressed as,

$$J_{Tun,M-S} = A^*T^2 \int_{\varepsilon}^{\infty} \Gamma(r) \quad \ln\left[\frac{1}{1+\exp((\varepsilon'-E_{Fm})/k_BT)}\right] d\varepsilon', \tag{3}$$

where A^* is the Richardson constant, T is the temperature, $E_{Fm} = -q\phi_m$ is the Fermi-level for the metal (silicide), $E_{Fn} = -q\phi_n$ is the electron Quasi Fermi-level in the Silicon, and $\Gamma(r)$ is the tunneling probability. The total tunneling current includes tunneling from both directions,

$$J_{Tun} = J_{Tun,S-M} - J_{Tun,M-S}. \tag{4}$$

The local tunneling generation rate can therefore be formulated as,

$$G_{Tun}(r) = \frac{A^*T}{k_B}\,\vec{E}\,\Gamma(r) \ln\left[\frac{1+\exp(-q(\psi-\phi_n)/k_BT)}{1+\exp(-q(\psi-\phi_m)/k_BT)}\right], \tag{5}$$

The WKB approximation for the tunneling probability can be written as,

$$\Gamma(r) = exp\left[-\frac{2}{\hbar}\int_0^r \sqrt{2m(\phi_b/q+\phi_m-\psi(x))}dx\right]. \tag{6}$$

The above integral is evaluated through numerical integration. The thermionic emission current is also included

at each contact node (filled-circle in Fig. 4), in addition to the tunneling current.

To ensured zero-current at thermal equilibrium, the Fermi-levels and built-in voltages of the contacts are evaluated at the beginning of the simulation. This advanced model is fully integrated into our new version of 2D/3D moment-based device simulator, Fieldday-III [6]. To test the capability of the model, the dependence of silicided contact I-V characteristics on the silicide/silicon interface doping and on the temperature and barrier height are shown in Figs. 5-6.

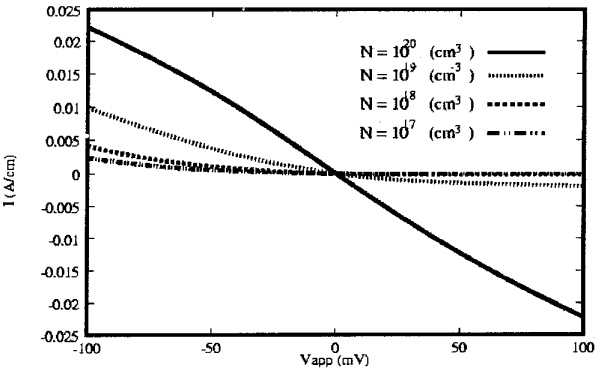

Figure 5: I-V characteristics of a $0.4\mu m$ $n^+ - n - n^+$ diode with silicide/silicon contact and different n^+ doping.

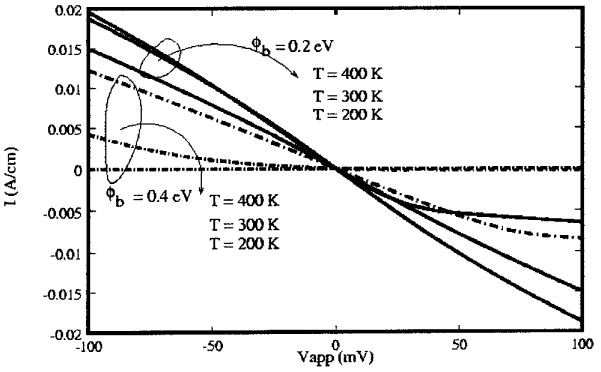

Figure 6: I-V characteristics of a silicide/silicon contact for I-V characteristics of a $0.4\mu m$ $n^+ - n - n^+$ diode with silicide/silicon contact and different different temperatures and barrier heights.

The model can cover the entire range of contact behavior. The contact exhibits Schottky characteristic when the doping is low and exhibits Ohmic characteristics when the doping is high. The current increases at elevated temperature due to the increases of thermionic and thermionic-field emission. It is interesting to note from Fig.6 that the contact characteristic switches from Ohmic-like to Schottky-like when the temperature is reduced.

Simulation Results

The model can reproduce experimental data of a $2\mu m$ Schottky S/D PMOS from Snyder and Helms [7] as shown in Fig.7. The thermal emission, field emission, and the

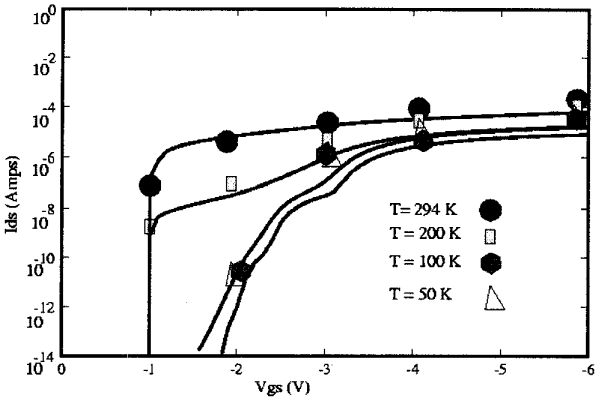

Figure 7: I-V characteristics of a Schottky S/D PFET at different temperatures. ($V_d = 2.0$ volts, $L = W = 2\mu m, t_{ox} = 143A$, undoped substrate; $\phi_{bn} = 0.9V$ (or $\phi_{bp} = 0.2V$)). Lines are simulations using the new tunneling contact model, symbols are experimental data from [7]. The changes from field emission (tunneling) to thermal emission and to channel resistance regime can be modeled.

channel resistance regime can clearly be seen in Fig.7. This device has too large a leakage current at room temperature for practical use. The leakage problem can, however, be alleviated by increasing the substrate doping. We next study the feasibility of scaling the Schottky S/D MOSFET for room temperature operation and compare its performance with the raised S/D MOSFET. The Vt-rolloff behavior is indeed comparable for Schottky S/D and raised S/D FET as can be seen in Fig.8.

However, the series resistance of a Schottky S/D MOSFET can be very large for small supply voltage. Considering a technology with a supply voltage of 1.5V or below, we found that the drive-current can be severely degraded by the contact resistance associated with the Schottky barrier (see Fig.9).

In Fig.10, we compare the conduction band along the channel of $1\mu m$ Schottky S/D and raised S/D NMOS. Even with relatively long channel, a significant voltage drop at the source side of the Schottky S/D FET clearly

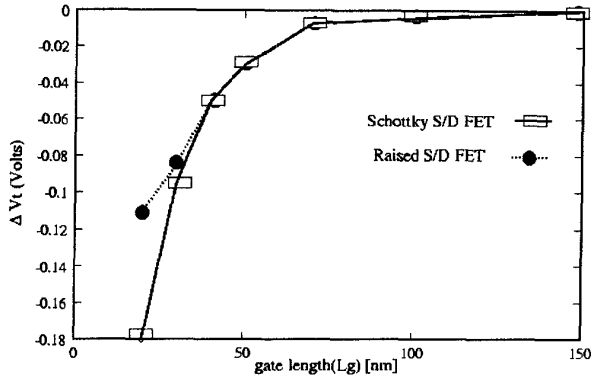

Figure 8: Linear Vt roll-off curves for Raised S/D and Schottky S/D NFET ($t_{ox} = 16A, N_{sub} = 5 \times 10^{17} cm^{-3}, X_j = 200A, V_{ds} = 50mV$ in both devices).

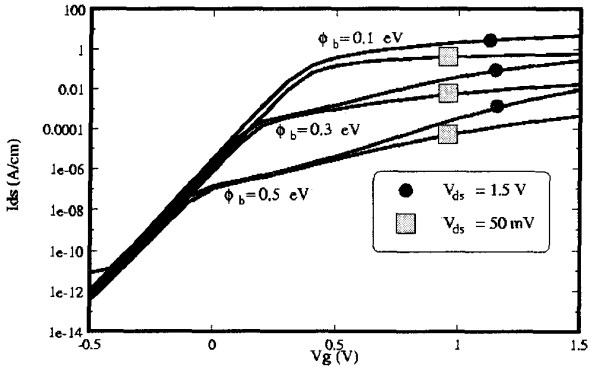

Figure 9: I-V characteristic of a Schottky S/D NFET for different Schottky barrier heights. The kink at low gate overdrive indicates large gate-voltage-dependent contact resistance, especially for high barrier contact materials.

indicates insufficient field-emission current to support the traditional drift current from the channel. The voltage drop is expected to be more severe for shorter channel length.

Discussion

In summary, we have presented, for the first time, a physical contact tunneling model that is critical for studying the increasingly important contact behavior in future scaled CMOS. With this new model, we compared the performance of raised S/D and Schottky S/D MOSFETs. Both raised S/D and Schottky S/D MOSFETs can be designed to give good short-channel characteristics. Because of the total elimination of S/D diffusion, the Schottky S/D FETs have the advantage of lower sheet resistance and potentially higher density. However, the contact resistance associated with the finite Schottky barrier can be large. A lower barrier height contact material should be used to minimize the contact resistance. It is worth mentioning that the equivalent channel-resistance was underestimated because the channel carrier transport was modeled by the drift-diffusion equation. The complete current path for drain current consists of the channel- and the contact-component. Therefore, the component associated with the tunneling contact should be even more important when velocity over-shoot is included.

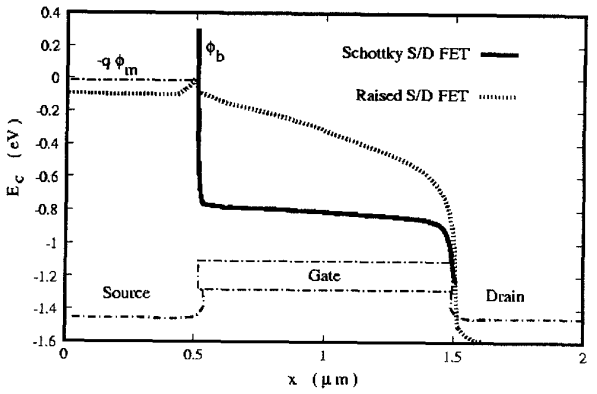

Figure 10: Comparison of conduction band, Ec, along the channel of Schottky and Raised S/D MOSFET. ($V_{gs} = V_{ds} = 1.5V$, and $\phi_b = 0.3V$.)

Acknowledgment

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