Comparison of Three Single-Phase PLL Algorithms for UPS Applications

Rubens M. Santos Filho, Paulo F. Seixas, Porfírio C. Cortizo, Leonardo A. B. Torres, and André F. Souza

***Abstract*—In this paper, the performance assessment of three software single-phase phase-locked loop (PLL) algorithms is carried out by means of dynamic analysis and experimental results. Several line disturbances such as phase-angle jump, voltage sag, frequency step, and harmonics are generated by a DSP together with a D/A converter and applied to each PLL. The actual minus the estimated phase-angle values are displayed, providing a refined method for performance evaluation and comparison. Guidelines for parameters adjustments are also presented. In addition, practical implementation issues such as computational delay effects, ride-through, and computational load are addressed. The developed models proved to accurately represent the PLLs under real test conditions.**

***Index Terms*—Mathematical modeling, phase-locked loops (PLLs), uninterruptible power systems (UPSs).**

I. Introduction

THE CORRECT line phase-angle is a very important information in uninterruptible power systems (UPSs) and in other grid-connected equipment such as controlled rectifiers, active filters, dynamic voltage restorers, and also in emerging distributed generation systems such as eolic and photovoltaic power plants. In UPS systems, in order to achieve bumpless operation when the bypass switch is turned on, it is necessary to guarantee prior good synchronization between the inverter output voltage and the primary source voltage. The same is true when the transfer switch is engaged in offline or line-interactive UPSs. In parallel redundant UPS arrangements, a very precise synchronization is also required prior to each UPS connection to the protected bus in order to avoid catastrophic transients. To estimate the phase-angle, open-loop and closed-loop methods are available [8], [10]. The closed-loop methods are commonly known as phase-locked loops (PLLs).

Generally, the line frequency varies within a limited range even in isolated systems, and its rate of change is limited by generators mechanical inertia. However, when grid faults occur, equipment become exposed to phase-angle jumps and voltage sags [15]. Furthermore, harmonics, notches, spikes, and other kinds of undesirable perturbations are common in industry line voltages. These disturbances and their effects on industrial power equipment are currently subjects of research [12]–[15].

The picture sketched above shows that the development of robust synchronizing algorithms is needed in order to meet the growing performance requirements of modern UPSs and other grid-connected equipment. The figures of merit of a PLL are the steady state phase-angle error, speed of response to phase, frequency and voltage amplitude disturbances, harmonic rejection and line unbalance rejection in case of three-phase systems.

In recent years, several PLL algorithms with different characteristics have been developed and presented in the literature [1]–[11]. However, it is often difficult to recognize their exact behavior and to compare their performances because the results are not presented in a quite satisfactory way, i.e., usually in the form of sawtooth or sine waves that represent the real and estimated phase angles.

The main objectives of this paper are to evaluate and to compare three selected single-phase PLL algorithms for UPS applications under diverse controlled line disturbances by means of dynamic analysis and experimental phase-angle error data. Approximate linear models are presented, and parameter adjustment guidelines are also proposed.

The selected structures have simple digital implementation and, therefore, low computational burden. The first PLL algorithm is based on fictitious electrical power [power-based PLL (pPLL)], which is a single-phase version of [1]. The second is based on the inverse Park transformation (parkPLL) [5], [6], and the later is based on an adaptive phase detection scheme, originally called enhanced PLL (EPLL) [8], [9].

II. Single-Phase PLL Structures for UPS Applications

Despite their differences, all PLL algorithms are derived from a standard structure which can be divided into three main sections: phase detector (PD), filter, and voltage controlled oscillator (VCO), as shown in Fig. 1. The differences from one PLL to another are concentrated in the PD section, which is nonlinear in general. The implementation of the filter and VCO sections is common to all structures covered in this paper. The linear model shown in Fig. 2 will be used to model the PLLs throughout this paper. The PD section dynamics are represented by $F(s)$, the compensator $C(s)$ is a proportional plus integral controller (PI) needed to meet closed-loop performance specifications, and, finally, the VCO function is represented as an integrator.

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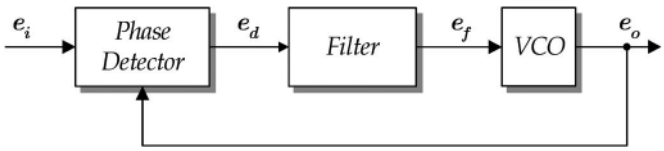

Fig. 1. Classical PLL structure.

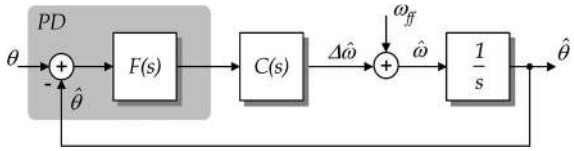

Fig. 2. PLL linear model.

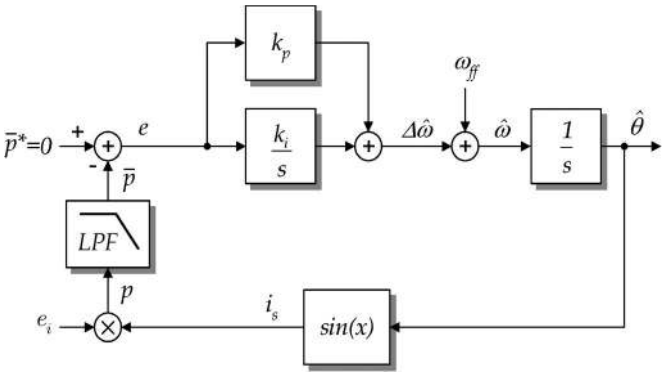

Fig. 3. Single-phase power PLL.

The input and output of this structure are the line voltage angle θ and the estimated angle $\hat{\theta}$, respectively. The integration in the compensator renders the system type II, so it will present zero steady state error for a step both in input angle and in input frequency. The feedforward term $\omega_{\rm ff}$ defines the central frequency around which the PLL will lock to.

A. pPLL

Fig. 3 displays the block diagram of the single-phase pPLL, which is a classical structure. Since its PD section is based on a single multiplier, the analogy with electric power can be used in order to understand its behavior more intuitively. If the fictitious power mean $\overline{p}$ is zero, then the fictitious current $i_{\rm s}$ will be in quadrature with the fundamental of the input voltage $e_{\rm i}$. Assuming a purely sinusoidal input voltage $e_{\rm i}$ in the form $V\cos\theta$, in that situation $\hat{\theta}$ equals θ.

The expression of the signal $p(\theta,\hat{\theta})$ in Fig. 3 is

$$p = V\cos\theta\sin\hat{\theta} \tag{1}$$

or

$$p = \frac{V}{2}\sin(\hat{\theta}-\theta) + \frac{V}{2}\sin(\hat{\theta}+\theta). \tag{2}$$

The low-pass filter extracts the mean power $\overline{p}$, which is given by the first term of (2). Considering $\theta = \omega t + \phi$, $\hat{\theta} = \hat{\omega}t + \hat{\phi}$ and allowing $\hat{\omega} \cong \omega$, for small phase differences $\phi - \hat{\phi}$, $\overline{p}$ can be approximated by

$$\overline{p} \cong \frac{V}{2}(\hat{\phi} - \phi) \tag{3}$$

which exhibits the small-signal static PD gain. The PD dynamics will rely entirely on the filter structure. As pointed out by (2), there is a strong drawback to this structure: The product of input voltage and fictitious current $i_{\rm s}$ yields a second harmonic component which has to be filtered out. Thus, at first sight, the low-pass filter should have a low cutoff frequency, which degrades system speed response.

Nevertheless, this drawback can be minimized if the filter order is increased simultaneously to its cutoff frequency, while maintaining adequate attenuation at the second harmonic and small phase lag at the desired open-loop crossover frequency. Thus, the careful design of the low-pass filter and compensator must be performed in order to provide good dynamic response and disturbance rejection. It is worth noticing that either a dc or a second harmonic component in input signal would produce a fundamental frequency component in PD output signal which must also be filtered out. Indeed, according to (2), each harmonic component of order h and amplitude $V_{\rm h}$ will produce two components of orders $h \pm 1$ and amplitude $V_{\rm h}/2$ in PD output. Moreover, subharmonic components in very low-frequency range (1–2 Hz) will produce components around fundamental frequency in PD output. Hence, it is desirable to have some attenuation at fundamental frequency so that large oscillations in the estimated frequency and phase are avoided. The parameter design guidelines are based on the frequency response method since the filter order may be high. An iterative design procedure, based on a trial-and-error approach can be outlined as follows.

1) Choose the open-loop crossover frequency $\omega_{\rm c}$ less than the fundamental frequency. There is a tradeoff between speed of response and rejection of DC, subharmonics and second harmonic in input voltage.
2) Choose filter attenuation at $2\cdot\omega_{\rm i}$ based on corresponding ripple $\mathbf{\Delta}\hat{\theta}$ allowable in estimated angle $\hat{\theta}$, where $\omega_{\rm i}$ is the line input frequency. This will be a first try since the PI gains are not known yet.
3) Choose filter type and order that meet desired attenuation with minimum phase delay at $\omega = \omega_{\rm c}$.
4) Check filter attenuation at fundamental frequency. If attenuation is not high enough to cope with expected dc and second harmonic levels in input voltage, change filter order or cutoff frequency and return to second step.
5) Based on the frequency response $M\angle\phi_G$ of cascaded PD, filter and integrator $G_{\rm PFI}(s) = s^{-1}F(s)V/2$ at $\omega = \omega_{\rm c}$, where $F(s)$ is the filter transfer function, determine the PI gains $k_{\rm p}$ and $k_{\rm i}$ that result in required phase margin $\phi_{\rm m}$ and crossover frequency $\omega_{\rm c}$

$$k_{\rm p} = M^{-1}\cos\phi_{\rm c} \tag{4}$$

$$k_{\rm i} = -k_{\rm p}\omega_{\rm c}\tan\phi_{\rm c} \tag{5}$$

where $\phi_{\rm m}$ is the desired phase margin $(\phi_{\rm m} < \phi_G + 180)$ and $\phi_{\rm c} = \phi_{\rm m} - \phi_G - 180^\circ$.
6) Having the gains $k_{\rm p}$ and $k_{\rm i}$, check if attenuations of $G_{\rm PFI}(s)$ at $\omega_{\rm i}$ and at $2\cdot\omega_{\rm i}$ are high enough and return to the second step if necessary.

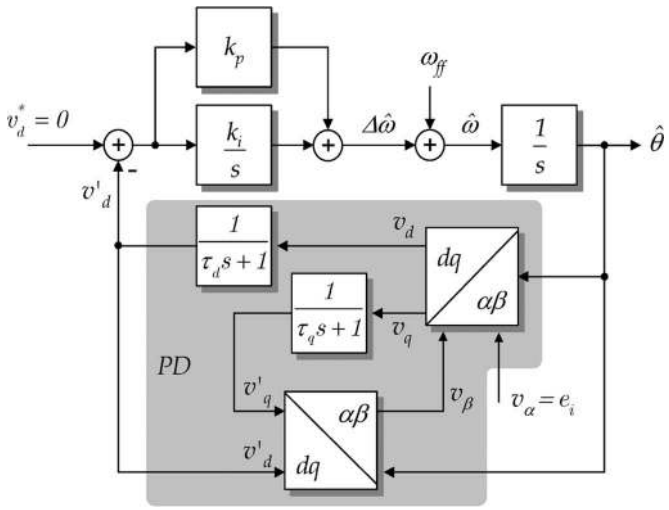

Fig. 4. Single-phase inverse Park PLL.

7) Using the diagram of Fig. 2 check dynamic response. Modify $\phi_{\rm m}$ and $\omega_{\rm c}$ as needed.

In this paper, we have chosen $\omega_{\rm c} = 10$ Hz, $\boldsymbol{\Delta}\hat{\theta} < 10^{-3}$ rad at 120 Hz and $\phi_{\rm m} > 30^\circ$ for 0.8 per unit input voltage amplitude, what demanded a fourth-order Butterworth-type filter, yielding: $\phi_{\rm m} = 34^\circ$, $k_{\rm p} = 160$, $k_{\rm i} = 3600$, $|G_{\rm PFI}(s)| = -28$ dB at 60 Hz, -58 dB at 120 Hz.

B. parkPLL

Fig. 4 displays the block diagram of the parkPLL [5], [6], which is a single-phase version of the three-phase SRF PLL [1]. The component v_β of the stationary frame is obtained by inverse Park transforming the filtered synchronous components v'_d and v'_q. Thus, a balanced three-phase system is emulated. The time constants τ_q and τ_d of the two first-order filters determine the PD dynamic behavior. The static gain of the PD section will be found as follows. The expressions of the transformations are

$$\begin{bmatrix} v_d \\ v_q \end{bmatrix} = \begin{bmatrix} \sin\hat{\theta} & \cos\hat{\theta} \\ \cos\hat{\theta} & -\sin\hat{\theta} \end{bmatrix} \begin{bmatrix} v_\alpha \\ v_\beta \end{bmatrix} \tag{6}$$

$$\begin{bmatrix} v'_\alpha \\ v_\beta \end{bmatrix} = \begin{bmatrix} \sin\hat{\theta} & \cos\hat{\theta} \\ \cos\hat{\theta} & -\sin\hat{\theta} \end{bmatrix} \begin{bmatrix} v'_d \\ v'_q \end{bmatrix}. \tag{7}$$

The filtered components v'_d and v'_q are given in frequency domain by

$$v'_d(s) = \frac{v_d(s)}{\tau_d s + 1} \tag{8}$$

$$v'_q(s) = \frac{v_q(s)}{\tau_q s + 1}. \tag{9}$$

Manipulating (6)–(9), one obtains (10), which describes the PD large signal behavior in the rotating reference frame. This expression represents a linear time-varying system because the state matrix and gain vector are functions of $\hat{\theta}(t)$

$$\frac{d}{dt}\begin{bmatrix} v'_d \\ v'_q \end{bmatrix} = \begin{bmatrix} -\frac{\sin^2\hat{\theta}}{\tau_d} & -\frac{\sin\hat{\theta}\cos\hat{\theta}}{\tau_d} \\ -\frac{\sin\hat{\theta}\cos\hat{\theta}}{\tau_q} & -\frac{\cos^2\hat{\theta}}{\tau_q} \end{bmatrix} \begin{bmatrix} v'_d \\ v'_q \end{bmatrix} + \begin{bmatrix} \frac{\sin\hat{\theta}}{\tau_d} \\ \frac{\cos\hat{\theta}}{\tau_q} \end{bmatrix} v_\alpha. \tag{10}$$

Considering $\hat{\theta} = \hat{\omega}t + \hat{\phi}$, $v_\alpha = V\cos(\omega t + \phi)$, and allowing $\hat{\omega} \cong \omega$, i.e., estimated frequency equal to the input frequency, the equilibrium point for the system can be found by zeroing the derivative terms in (10) and solving for v'_d and v'_q, leading to

$$\overline{V}'_d = V\sin\phi_e \tag{11}$$

$$\overline{V}'_q = V\cos\phi_e \tag{12}$$

where $\phi_e = \hat{\phi} - \phi$, $\overline{V}'_d$ and $\overline{V}'_q$ are the steady state values of the PD outputs.

Expression (11) reveals the rationale behind the structural approach found in this PLL: If the component v'_d is regulated to zero, ϕ_e will also be zero. Moreover, (12) shows that, in this situation, $\overline{V}'_q$ is equal to the input voltage amplitude. Writing the differential equations for the stationary frame variables v'_α and v'_β yields

$$\frac{d}{dt}\begin{bmatrix} v'_\alpha \\ v'_\beta \end{bmatrix} = \begin{bmatrix} -1/\tau & d\hat{\theta}/dt \\ -d\hat{\theta}/dt & 0 \end{bmatrix} \begin{bmatrix} v'_\alpha \\ v'_\beta \end{bmatrix} + \begin{bmatrix} 1/\tau \\ 0 \end{bmatrix} v_\alpha \tag{13}$$

where the time constants τ_d and τ_q were made equal to τ. Recognizing $d\hat{\theta}/dt$ as the estimated frequency $\hat{\omega}$ and allowing $\hat{\omega} \cong \omega$ and constant, (13) becomes a SISO linear time invariant system with sinusoidal excitation, whose characteristic equation is $\det(\lambda I - A) = 0$ or

$$\lambda^2 + \lambda/\tau + \hat{\omega}^2 = 0. \tag{14}$$

The eigenvalues will depend on τ and $\hat{\omega}$ according to

$$\lambda_{1,2} = -\frac{1}{2\tau} \pm \frac{1}{2}\sqrt{\frac{1}{\tau^2} - 4\hat{\omega}^2} \tag{15}$$

which shows that this PD is always asymptotically stable around the equilibrium condition $\hat{\omega} \cong \omega$. If $\tau^{-1} \gg 2\hat{\omega}$, i.e., if τ is made too small, a pair of real poles will take place. One of these poles will be $\lambda_1 \approx \tau^{-1}$ which is fast, but λ_2 will approximate zero, and it will dominate the dynamics with slow time constant. Otherwise, if $\tau^{-1} \ll 2\hat{\omega}$, a pair of complex conjugate poles with small real part will occur, which are also slow and oscillatory. Hence, if fast dynamics are required, the filter cutoff frequency should be set to $1/\tau \approx 2\omega$, i.e., the filter cutoff frequency should be equal to about two times line frequency.

After applying the Park transformation so that $v'_d = v'_\alpha\sin\hat{\theta} + v'_\beta\cos\hat{\theta}$, and by considering that the oscillating terms due to sinusoidal excitation will decay to zero according to the real part in (15), the transfer function of the PD output v'_d from an abrupt phase change can be approximated by

$$F(s) = \frac{v'_d(s)}{\phi_e(s)} \cong \frac{\overline{V}'_d}{2\tau s + 1}. \tag{16}$$

Hence, for small phase differences $\hat{\phi} - \phi$ the closed-loop transfer function of the system in Fig. 4 can be approximated by

$$\frac{\hat{\phi}(s)}{\phi(s)} \cong k_{\rm v}\frac{sk_{\rm p} + k_{\rm i}}{2\tau s^3 + s^2 + sk_{\rm v}k_{\rm p} + k_{\rm v}k_{\rm i}} \tag{17}$$

where $k_{\rm v}$ is the static PD gain $= V$.

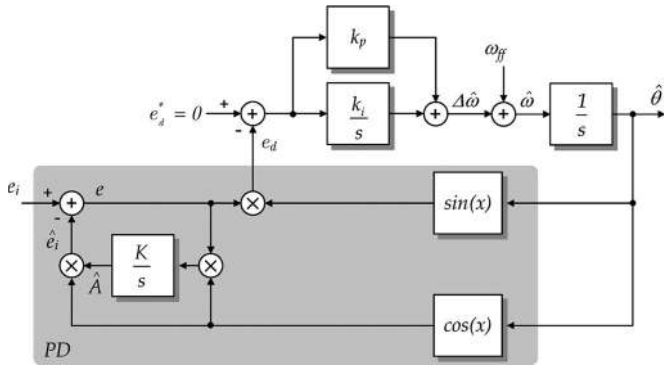

Fig. 5. Single-phase EPLL.

Based on (17), the compensator gains can be set up in order to meet dynamic and disturbance rejection specifications. It is important to notice that each harmonic component of order h and amplitude $V_{\rm h}$ in input voltage will produce two components of orders $h \pm 1$ in the PD output signal, whose amplitudes $V_{\rm h1}$ and $V_{\rm h2}$ can be found by writing the steady state equation of the PD output v'_d for $\omega = h\hat{\omega}$, yielding

$$v'_d(t) = \frac{V_{\rm h}V_1}{2}(h+1)\sin\left[(h-1)\omega t + \phi_e - \phi_1\right] - \frac{V_{\rm h}V_1}{2}(h-1)\sin\left[(h+1)\omega t - \phi_e - \phi_1\right] \quad (18)$$

where ω is the input voltage fundamental frequency; $V_{\rm h}$ is the input harmonic amplitude; and V_1 and ϕ_1 are the gain and phase of $v'_\alpha(s)$ for $s = j\omega$ in (13).

By inspection of (18), one concludes that

$$V_{\rm h1} = \frac{V_{\rm h}V_1}{2}(h+1) \quad (19)$$

$$V_{\rm h2} = \frac{V_{\rm h}V_1}{2}(h-1). \quad (20)$$

Therefore, there is a tradeoff between speed of response and rejection of harmonic components. Furthermore, a dc level in input voltage will lead to a fundamental frequency oscillation in the dq components. If harmonics are a concern, the response of $G_{\rm OL}(s) = s^{-1}F(s)C(s)$ at the harmonic frequencies of interest may be used as a target parameter for adjusting $k_{\rm p}$, $k_{\rm i}$, and τ.

In this paper, the cutoff frequencies of the d and q filters were set to 120 Hz, yielding critical damping for the PD. The PI controller gains were set to $k_{\rm p} = 200$ and $k_{\rm i} = 20\,000$ for $V = 0.8$ per unit, yielding 50-ms settling time and amplitude attenuation of 20 dB at 120 Hz.

C. EPLL

Fig. 5 displays the block diagram of the EPLL [8], [9]. This PLL is based on adaptive filter theory. Basically, it reconstructs in real time the fundamental component of the input signal by estimating its amplitude, phase, and frequency through the steepest descent algorithm. The gain K controls the convergence speed of $\hat{A}$, i.e., the estimated line voltage amplitude. Assuming a purely sinusoidal input voltage $e_{\rm i}$ in the form $V\cos\theta$, the PD static gain can be found by writing the expression of its output e_d as a function of θ, $\hat{\theta}$ and V, yielding

$$e_d = \frac{V}{2}\sin(\hat{\theta} - \theta) + \frac{V}{2}\sin(\theta + \hat{\theta}) - \frac{\hat{A}}{2}\sin 2\hat{\theta}. \quad (21)$$

Considering $\hat{\theta} = \hat{\omega}t + \hat{\phi}$, $\theta = \omega t + \phi$ and allowing $\hat{\omega} \cong \omega$, (21) can be approximated by (22) if $\hat{A} \approx V$

$$e_d \cong \frac{V}{2}(\hat{\phi} - \phi). \quad (22)$$

Notice that the phase difference $\hat{\phi} - \phi$ is readily available at PD output without any time delay. Oscillatory terms whose frequency is about twice input frequency as can be deduced from (21) will exist only during transient conditions, once they will fade out as $\hat{A}$ converges to V and $\hat{\phi} - \phi$ goes to zero in steady state. Hence, neglecting the PD dynamics and taking phase ϕ as input, for small phase differences $\hat{\phi} - \phi$, the EPLL closed-loop transfer function can be approximated by

$$\frac{\hat{\phi}(s)}{\phi(s)} \cong k_{\rm v}\frac{sk_{\rm p} + k_{\rm i}}{s^2 + sk_{\rm v}k_{\rm p} + k_{\rm v}k_{\rm i}} \quad (23)$$

where $k_{\rm v} = V/2$ is the static PD gain.

The compensator gains can be set up based on (23) in order to meet closed-loop dynamic and disturbance rejection specifications. As in the parkPLL, each harmonic component of order h and amplitude $V_{\rm h}$ in input voltage will generate two components of orders $h \pm 1$ in the PD output signal. Therefore, there is a tradeoff between speed of response and rejection of harmonic components. In addition, a dc level in input voltage will lead to a fundamental frequency oscillation in PD output. If harmonics are a concern, the closed-loop frequency response at the harmonic frequencies of interest may be used as a target parameter for adjusting $k_{\rm p}$ and $k_{\rm i}$.

In the experiments reported in this paper, the amplitude convergence gain K was set to 200. This gain can be varied in a wide range with low influence on overall results. The gains of the PI controller for $V = 0.8$ per unit were set to $k_{\rm p} = 400$ and $k_{\rm i} = 40\,000$, yielding closed-loop damping $\zeta \approx 0.63$, 40-ms settling time and amplitude attenuation of 13.4 dB at 120 Hz.

III. Experimental Results

A. General Setup and Practical Issues

Real time experiments based on a digital signal processor (DSP)—DSP platform were conducted for all three PLL structures in order to validate the former analysis under several line input disturbances. The block diagram of the experimental setup is depicted in Fig. 6. A fixed-point DSP from Texas Instruments (TMS320F2812) was used to perform both the PLL algorithms and the generation of their input signal through a two channel, 10-b D/A converter. In order to present the results more clearly, the known phase-angle θ and the

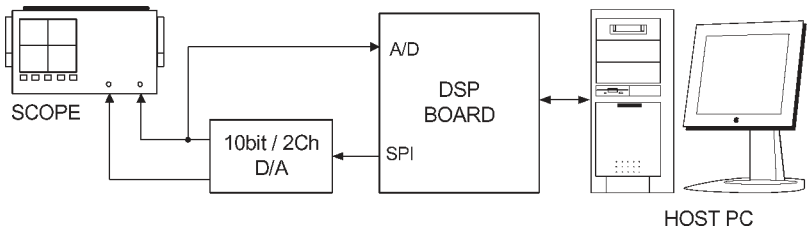

Fig. 6. Experimental setup overview.

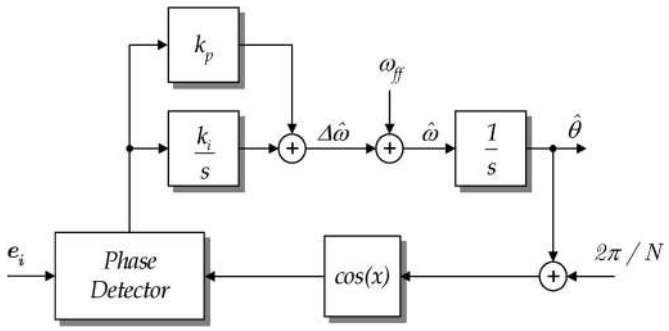

Fig. 7. Correction of the steady-state error in $\hat{\theta}$ due to computational delay.

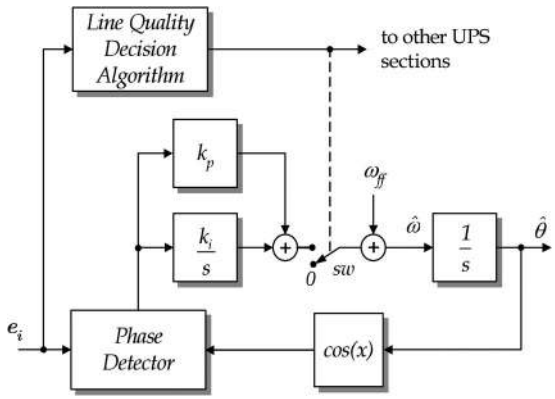

Fig. 8. Switch is needed to assure correct free-running in abnormal line conditions.

estimated phase-angle $\hat{\theta}$ were subtracted to allow comparison, performance evaluation, and model validation based on the phase-angle error. The host PC was used to select and to issue preprogrammed line disturbances. Moreover, the PC was also used to select the output signal to come from one of the D/A converter channels, while the other channel was kept dedicated to the emulated line signal.

A sampling frequency of 30 720 Hz was used. This apparently high value is a consequence of the bandwidth requirements of the UPS output voltage control loop rather than the PLL bandwidth requirements. The system A/D conversion time and D/A update time are negligible when compared to sample time. The discretization process has minor effects in the above modeling provided that sampling frequency is more than ten times the PLL bandwidth. Nevertheless, the implementation of low cutoff frequency filters at high sampling rates leads to numeric representation problems, even when using 32-b word length. The fourth-order Butterworth filter for the pPLL has been implemented with the help of the Texas Instruments 32-b filter library, which performs the filtering through cascaded second-order sections, reducing numeric problems. In addition, it is written in assembly language optimized to take full advantage of DSP architecture. The Q20 fixed point base was employed for overall calculations, while the Q30 base was used for filter calculations. The trapezoidal method was used to implement the integrations because it yields exact phase equivalence when discretizing continuous systems.

A computational delay of one sampling time occurs in the control loop. This delay has negligible effect on stability, since the closed-loop poles are at low frequency, very far from Nyquist frequency. However, a steady state error of $2\pi/N$ radians in estimated angle (where N is the number of samples per fundamental period) occurs due to this one sample time delay. In the performed experiments N was equal to 512 at the nominal frequency of 60 Hz, resulting in 0.7° steady state error. Such quite small error value could only be confirmed with the help of Lissajous (XY) scope plots. This error could be compensated by adding the value $2\pi/N$ to $\hat{\theta}$ before feeding it back, as shown in Fig. 7. This correction term would need to vary according to the input frequency. Nevertheless, it yields satisfactory correction for a range in input frequency variation of $\pm 15\%$.

Another important and essential PLL feature for UPS applications is the ride-through capability, i.e., the PLL output signal must remain running in the case of unacceptable line conditions or even in the case of line outage, because this signal is usually the reference for the UPS inverter control section. The usual implementation of PLL algorithms found in the literature does not inherently provide the ride-through feature since the PI controller will try to follow the reference even when the line voltage is in an undefined, abnormal condition, or when it is out of PLL lock range. A line quality algorithm that continuously inspects the line voltage shall turn a switch in abnormal line situations, so that the PLL output remains on its nominal condition, as depicted in Fig. 8. This algorithm must have adequate hysteresis margins and timings in order to avoid unstable behavior near established quality thresholds. In this paper, the adopted quality criterion was the range $(-20\%, +15\%)$ for the input rms line voltage. Further discussion of line quality criteria is beyond the scope of this paper.

B. Experimental Results for the pPLL

Figs. 9 and 10 show the phase-angle error $\theta - \hat{\theta}$ and estimated frequency $\hat{\omega}$ responses to a 40° phase-angle jump and to a frequency step of +5 Hz in input voltage, respectively. It can be seen the good agreement between predicted and actual results. The oscillations in the variables are not predicted by the

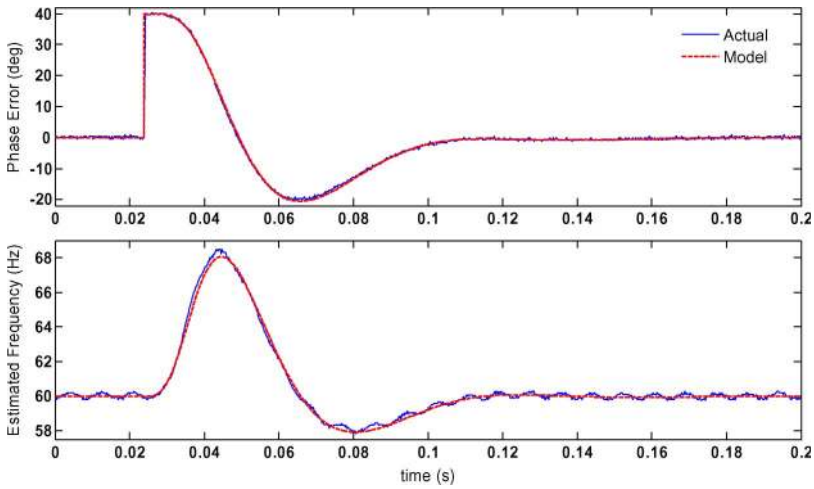

Fig. 9. pPLL response to a phase-angle jump of 40°. Top: phase-angle error. Bottom: estimated frequency.

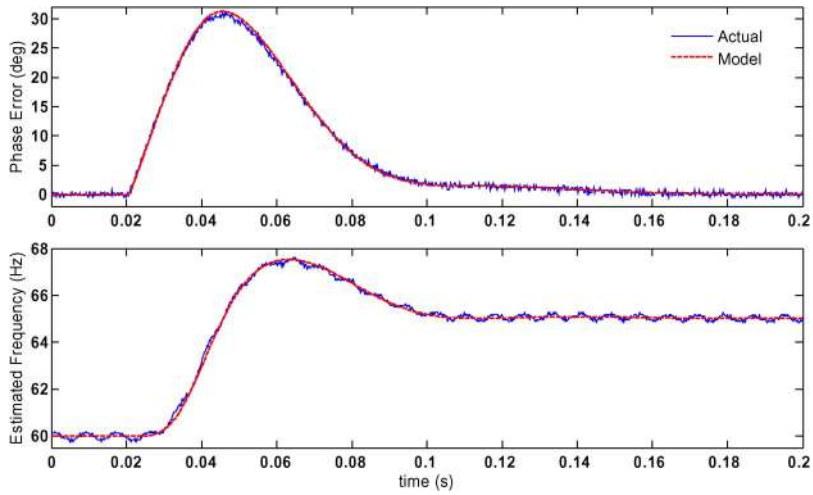

Fig. 10. pPLL response to a frequency step from 60 to 65 Hz. Top: phase-angle error. Bottom: estimated frequency.

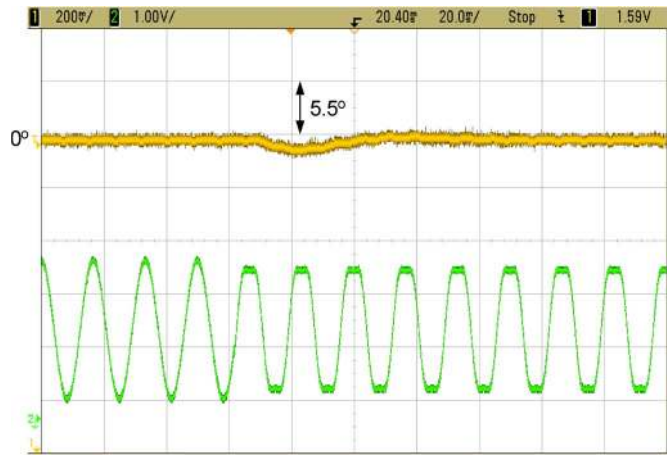

Fig. 11. pPLL response to 15% third harmonic injection in input voltage. Top: phase-angle error. Bottom: input signal to the PLL (0.3 per unit/div).

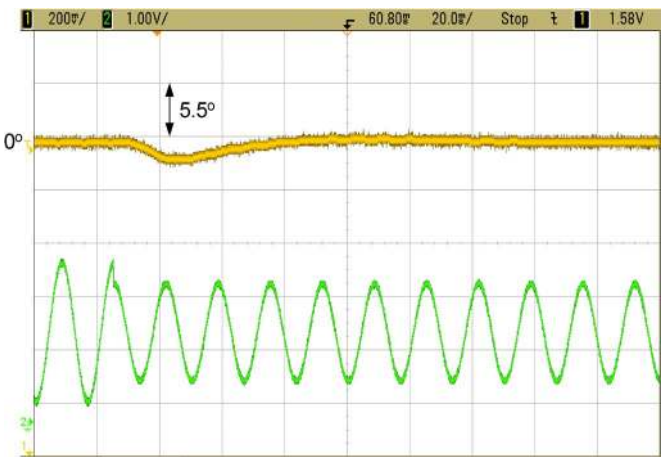

Fig. 12. pPLL response to a voltage sag of 30% in input voltage. Top: phase-angle error. Bottom: input signal to the PLL (0.3 per unit/div).

model since it is an approximation that describes the relation between estimated angle and input phase difference. The pPLL locks to the new condition with zero steady-state error within about seven cycles (120 ms) in both tests.

Fig. 11 shows the response to 15% third harmonic injection. As shown, the pPLL is almost insensitive to harmonics. Fig. 12 shows the voltage sag test response, where it can be seen the pPLL low sensitivity to input signal amplitude variations.

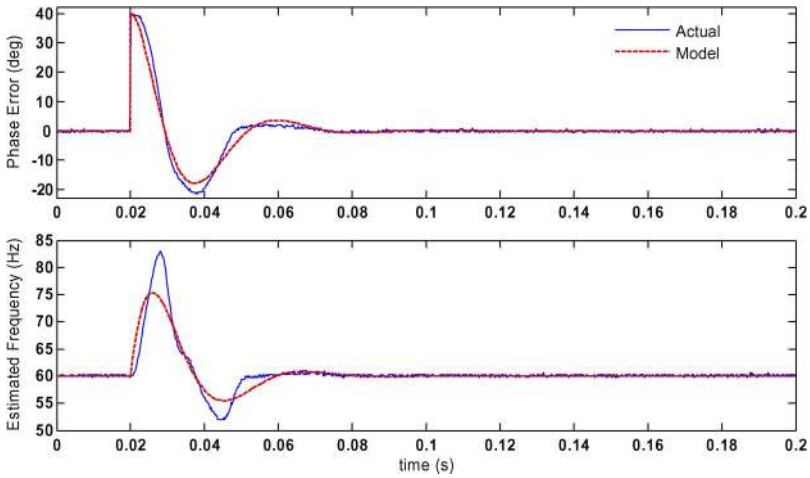

Fig. 13. parkPLL response to a phase-angle jump of 40°. Top: phase-angle error. Bottom: estimated frequency.

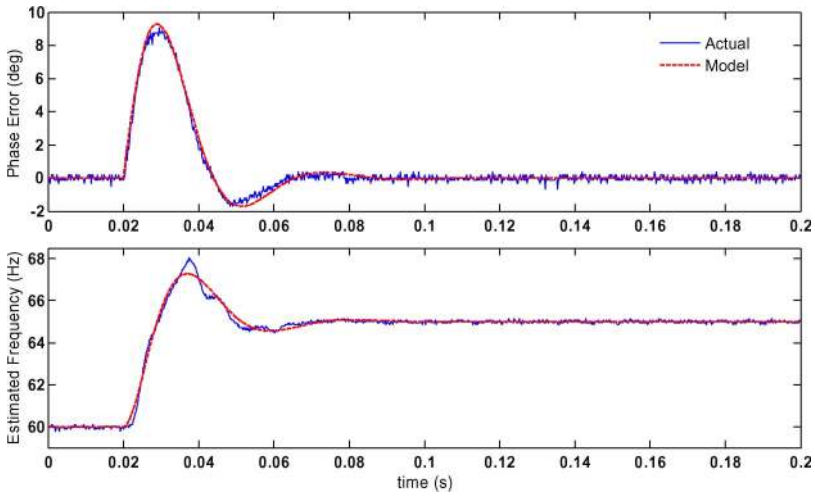

Fig. 14. parkPLL response to a frequency step from 60 to 65 Hz. Top: phase-angle error. Bottom: estimated frequency.

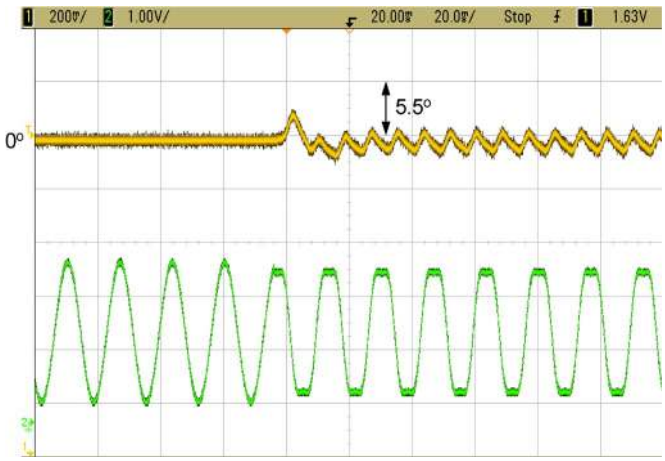

Fig. 15. parkPLL response to 15% third harmonic injection in input voltage. Top: phase-angle error. Bottom: input signal to the PLL (0.3 per unit/div).

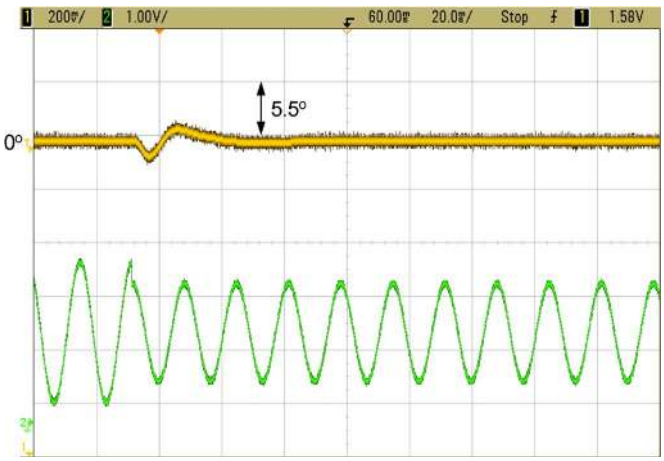

Fig. 16. parkPLL response to a voltage sag of 30% in input voltage. Top: phase-angle error. Bottom: input signal to the PLL (0.3 per unit/div).

C. Experimental Results for the parkPLL

Fig. 13 shows the parkPLL response to a 40° phase-angle jump. The settling time is about three cycles (50 ms) in both tests. It can be seen the good agreement of predicted and actual results.

In Fig. 14, the parkPLL locks to the new frequency quickly with zero steady-state error after a frequency step of +5 Hz

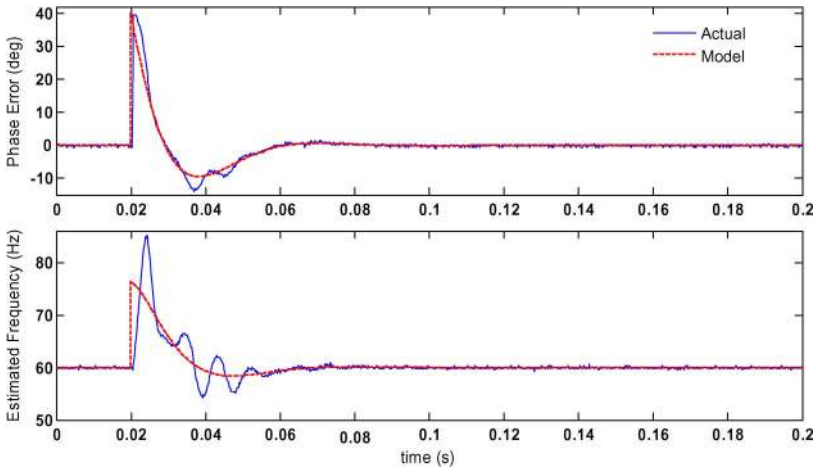

Fig. 17. EPLL response to a phase-angle jump of 40°. Top: phase-angle error. Bottom: estimated frequency.

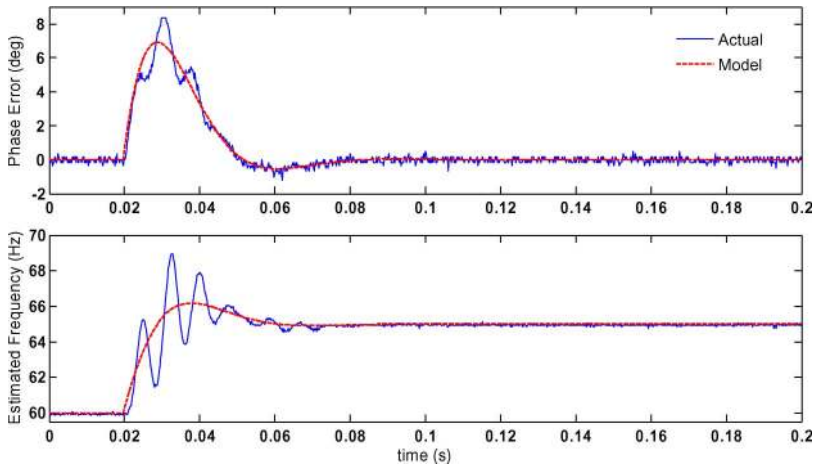

Fig. 18. EPLL response to a frequency step from 60 to 65 Hz. Top: phase-angle error. Bottom: estimated frequency.

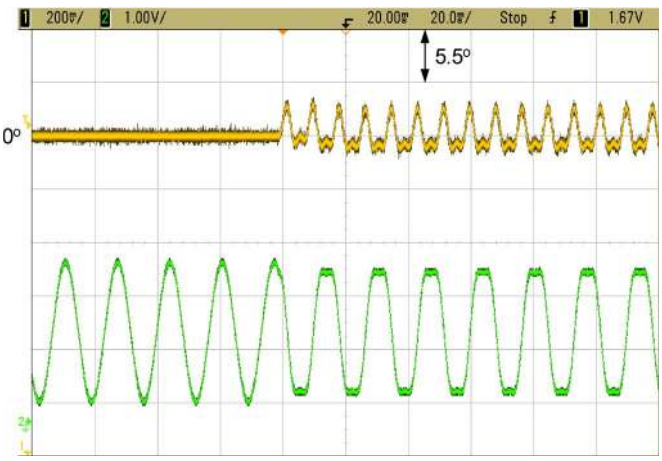

Fig. 19. EPLL response to 15% third harmonic injection in input voltage. Top: phase-angle error. Bottom: input signal to the PLL (0.3 per unit/div).

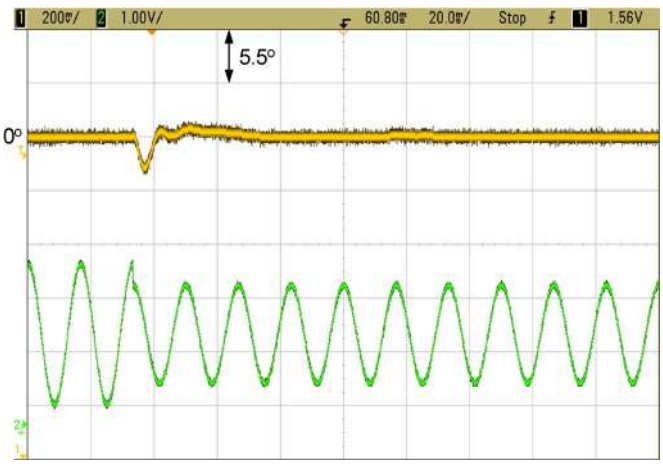

Fig. 20. EPLL response to a voltage sag of 30% in input voltage. Top: phase-angle error. Bottom: input signal to the PLL (0.3 per unit/div).

in input voltage. Fig. 15 shows the response to 15% third harmonic injection, where an oscillation of about 3° peak-to-peak in steady state is noticeable. Fig. 16 shows the response to 30% voltage sag. The phase-angle error is still small, although it is higher than the pPLL error to the same test.

D. Experimental Results for the EPLL

Fig. 17 shows the response to a 40° phase-angle jump in input voltage. The settling time is about three cycles (40 ms) for both tests. Fig. 18 shows the response to a frequency

TABLE I
EXPERIMENTAL RESULTS SUMMARY

	pPLL	parkPLL	EPLL
+5Hz Frequency step			
Settling time	7 cycles	3 cycles	2.5 cycles
Peak Error	30°	9°	9°
+40° Phase-angle jump			
Settling time	7 cycles	3 cycles	2.5 cycles
Overshoot	23°	14°	15°
30% Voltage sag			
Settling time	5 cycles	2 cycles	2.5 cycles
Peak Error	2°	4°	3°
15% 3rd harmonic injection			
Peak-to-Peak phase error	≈0°	3°	5°
Computational Load	68%	100%	80%
	2.58μs	3.80μs	3.04μs

step of +5 Hz. The PLL locks to the new frequency quickly with zero steady state error. The third harmonic injection led to about 5° peak-to-peak error in steady state, as shown in Fig. 19. The response to 30% voltage sag is shown in Fig. 20. This result has been confirmed by floating point simulation in MATLAB.

E. Results Summary

Table I presents a summary of the main time response parameters and other characteristics found in the experimental results for the PLLs.

IV. CONCLUDING REMARKS

Three simple different single-phase PLL structures have been analyzed and their experimental results have been objectively presented by true phase-angle error data. Schemes for avoiding unpredictable PLL behavior under abnormal line conditions and also to compensate for computational delay effect on steady state phase-angle error have been proposed.

The developed models led to results with good agreement with experimental data. The modeling error for the parkPLL PD decreases as the filter time constant τ increases. The models could only predict the averaged evolution of the estimated frequencies of the parkPLL and EPLL. The difference between predicted and actual phase-angle error also decreases when closed-loop bandwidths of these PLLs are reduced.

The dynamic analysis showed that the EPLL has the fastest PD, but its output signal highly oscillates at second harmonic during transient conditions, therefore some filtering may be required at this frequency depending on the application. The parkPLL PD has an inherent filtering, but its output also oscillates at second harmonic during transient conditions. The speed of response of these two PLLs to input angle disturbances can be increased at the cost of lower harmonic rejection. On the other hand, the pPLL bandwidth can be extended at the cost of higher filter order. It is worth to notice that the static PD gain in all three structures depends on input signal amplitude V.

The proposed method for designing the pPLL filter allowed the extension of its bandwidth when compared to usual low-order filtering, while maintaining good attenuation of second and higher harmonic orders. This shows that the pPLL, when appropriately tuned, can become almost insensitive to harmonics in the input voltage and to voltage sags. This robustness is achieved at the cost of only augmenting settling time by a factor of two when compared to the others structures. Moreover, this PLL had the lowest computational load, and showed to be suitable to run under severe line conditions as it is the case of UPS systems.

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