# Comparisons Between Serpentine and Flat Spiral Delay Lines on Transient Reflection/Transmission Waveforms and Eye Diagrams

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***Abstract*—In contrast to the commonly employed single-ended delay lines, the employment of differential signaling may alleviate the occurrence of crosstalk and improve the signal integrity. This paper qualitatively investigates the time-domain reflection (TDR) and time-domain transmission (TDT) waveforms for the single-ended and differential delay lines with the serpentine and flat spiral routing schemes. A numerical formula is then proposed to quantitatively predict the voltage levels of the saturated near-end and far-end propagating crosstalk noises among the sections of differential delay lines. Signal waveforms and eye diagrams of the four basic routing schemes are obtained by HSPICE simulations, demonstrating that the combination of differential signaling and flat spiral layouts can exhibit the best delay-line performance. Furthermore, both the TDR and TDT measurements for differential delay lines are performed to validate the exactitude of proposed analyses.**

***Index Terms*—Crosstalk, differential delay line, eye diagram, flat spiral, laddering wave, serpentine, signal integrity, time-domain reflection (TDR), time-domain transmission (TDT).**

## I. Introduction

As THE cycle time of computer systems falls into the subnanosecond regime, the fraction of cycle time to accommodate the clock skew for the synchronization of clock signal among the logic gates has risen. While several approaches have been proposed to minimize the clock skew, the delay lines are usually employed in the critical nets of a printed circuit board (PCB), for example, the serpentine or flat spiral routing schemes, as depicted in Fig. 1. Intuitively, the total time delay should be proportional to the total length of the delay line. However, the crosstalk noise induced by those closely packed transmission-line sections may cause a drastic deterioration in the total time delay and even result in the false switching of logic gates, especially for the serpentine delay line [1], [2].

Being dependent on the difference in the signal level on the paired lines, the differential circuits are relatively insensitive to noises such as the ground bounce that may exist on the power and/or ground plane and to the common-mode signals that may appear equally on each line. Moreover, the differential signals are somewhat immune from the electromagnetic interference (EMI) and crosstalk noise. Therefore, the differential signaling gradually becomes a common routing scheme in the PCB layout design rather than the single-ended signaling. Until now, it has been widely applied in high-speed digital systems, such as for the serial ATA and USB 2.0, and a typical example is PCI Express interconnect.

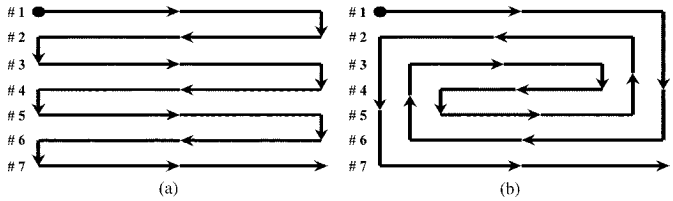


Fig. 1. Two typical routing schemes for the delay line. (a) Serpentine routing scheme. (b) Flat spiral routing scheme.

The signaling characterization of differential delay lines in both the serpentine and flat spiral schemes is investigated in this paper [3]. By using a simple trace model and extending the mechanism to the differential form, the responded time-domain reflection/time-domain transmission (TDR/TDT) waveforms of delay lines are qualitatively explained in Section II. A numerical formula derived by the concept of the pair-to-pair coupling is used to quantitatively predict the level of crosstalk noise on the differential delay lines. Sections III and IV thereof present the simulated TDR/TDT waveforms and eye diagrams of four delay lines, which have the cross sections as depicted in Fig. 2. The magnitudes of crosstalk noise under the single-ended and differential signaling conditions are compared as well. The routing scheme, the number of sections, the spacing $S$ between two sections, the loss of material, and the bit period of signals are also identified to comprehend the major parameters affecting the eye diagrams. The measurement results and their comparisons are presented in Section V to validate the accuracy of proposed analyses. Finally, the conclusions are drawn in Section VI.

## II. Crosstalk-Induced Noises at TDT and TDR for Delay Lines

First, consider that the single-ended delay lines shown in Fig. 1 are matched at both ends and a ramp pulse of rise time $t_r$ is launched at the sending end of the delay lines. It is known that the near-end crosstalk among the sections of a single-ended serpentine delay line accumulates in phase and

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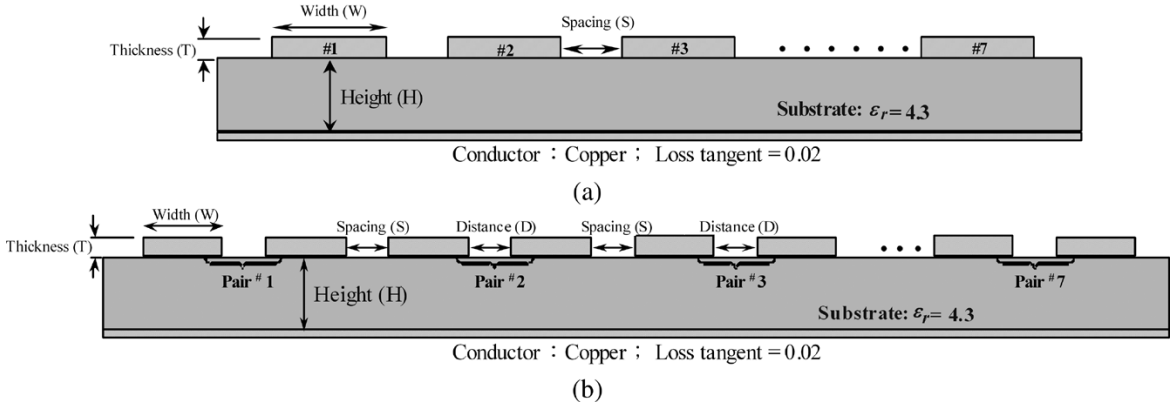


Fig. 2. Cross-sectional view of the delay lines in reference to Fig. 1. (a) Configuration of the single-ended lines. (b) Configuration of the differential-pair lines.

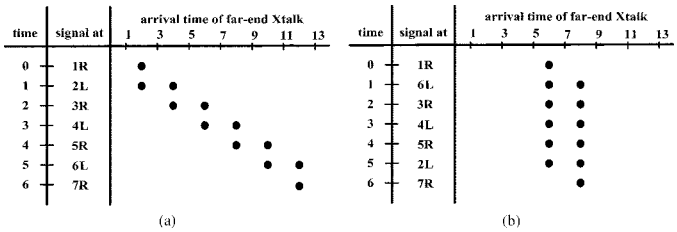


Fig. 3. Time diagrams of TDR far-end crosstalk noise (Xtalk) due to the adjacent coupling in both delay lines as depicted in Fig. 1. (a) Serpentine. (b) Flat spiral.

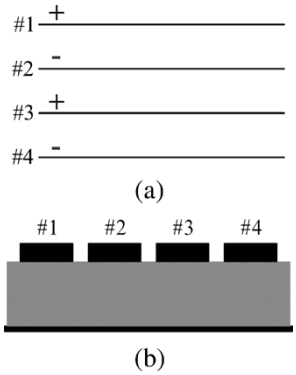


Fig. 4. Top and side views of the two-pair differential coupled lines. (a) Top view. (b) Side view.

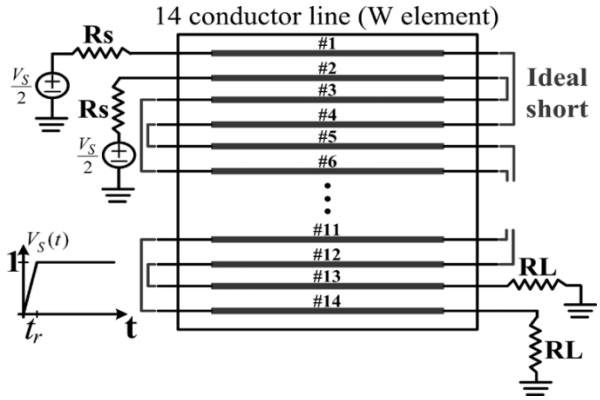


Fig. 5. Graphical configuration of simulation method used in HSPICE.

TABLE I
CROSSTALK NOISE LEVELS OF THE SEVEN-PAIR DIFFERENTIAL SERPENTINE DELAY LINES

| Analysis Methodology | First Voltage Drop on TDR | The Highest Ladder on TDT |
|---|---|---|
| Formula Calculation | 21.97 mV | 22.86 mV |
| HSPICE Simulation | 21.95 mV | 22.41 mV |

appears as a laddering wave on the TDT time diagram [1]. The employment of single-ended flat spiral layout patterns has the ability to evenly spread the crosstalk noise in time and avoids the crosstalk penalty at the receiving end [2].

If the transmission line lies in an inhomogeneous space, such as a microstrip line, the capacitive and inductive coupling waves do not cancel and the far-end noise is present. This will result in significant noises at the sending end. For example, consider a single-ended serpentine delay line with time delay $t_d$ for each section. The far-end crosstalk at the instant of $t = t_d$ due to the adjacent coupling will be induced at the far-end of section II when the main signal propagates to the right-hand side of section I, as depicted in Fig. 1. It reaches the sending end at $t = 2t_d$, as marked by a dot in the row "1R" of Fig. 3(a). After the main signal travels down to the left-hand side of section II, denoted by "2L", it induces two adjacent crosstalk noises at the near end while $t = 2t_d$: one is at section I, which directly appears at the sending end; the other is at section III, which requires another $2t_d$ to arrive at the sending end and thus appears at $t = 4t_d$. Similarly, the other crosstalk noises will be induced as the main signal travels down all sections to the receiver, but they arrive at the sending end in the different time. Therefore, no matter how many sections are on the delay line, the crosstalk noises are uniformly distributed in time and the magnitude should be equal to $2 \times V_f$, where $V_f$ means the magnitude of far-end crosstalk among the neighboring sections.

On the other hand, for a single-ended flat spiral delay line, the far-end crosstalk induced by the main signal at "1R" must travel five sections to reach the sending end, that is, it will present at the sending end at $t = 6t_d$, as marked by a dot in the row "1R" of Fig. 3(b). Then, the main signal propagates down to the left-hand side of section VI at $t = 2t_d$ and induces two far-end crosstalk pulses at the near-ends of sections V and VII. The two pulses require the additional $4t_d$ and $6t_d$, respectively,

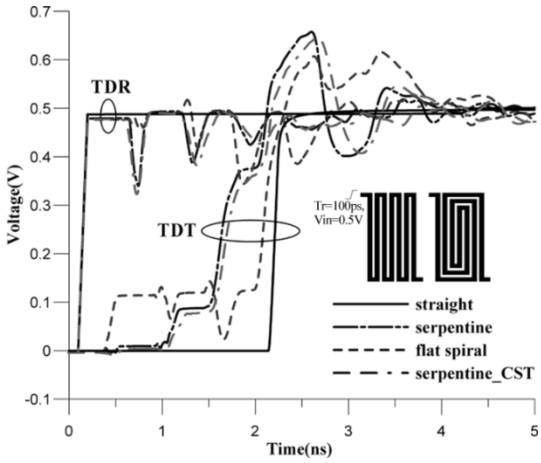


Fig. 6. Simulated TDR/T waveforms of the single-ended delay lines

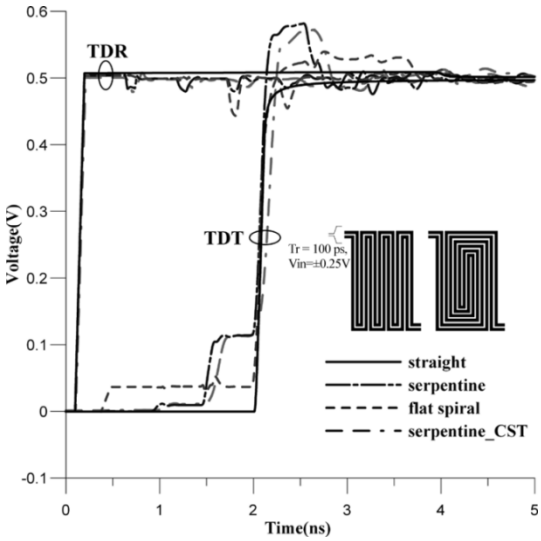


Fig. 7. Simulated TDR/T waveforms of the differential delay lines.

TABLE II
CROSSTALK LEVEL OF THE SERPENTINE DELAY LINES

| Layout Design | First Voltage Drop on TDR | The Highest Ladder on TDT |
|---|---|---|
| Single-Ended | 139 mV | 376 mV |
| Differential | 20 mV | 114 mV |

to reach the sending end. They altogether form a pulse in the TDR time diagram at $t = 6t_d$ and $t = 8t_d$, as distinguished by the dot marks in the row "6L" of Fig. 3(b). This process continues until the main signal finally arrives at the receiving end. Before the arrival, it has induced six pulses due to the adjacent coupling. Although being induced at the different instants, all of them get to the sending end at the same time and accumulate to appear as a large downward pulse of magnitude $6 \times V_f$ on the TDR waveform. The more the number of sections on the delay line, the more significantly the crosstalk distorts the TDR waveform. Consequently, the employment of a flat spiral layout pattern does have the ability to avoid the crosstalk penalty at the receiving end, but its far-end crosstalk will accumulate at the sending end to cause an aggravated crosstalk as observed on the TDR waveform.

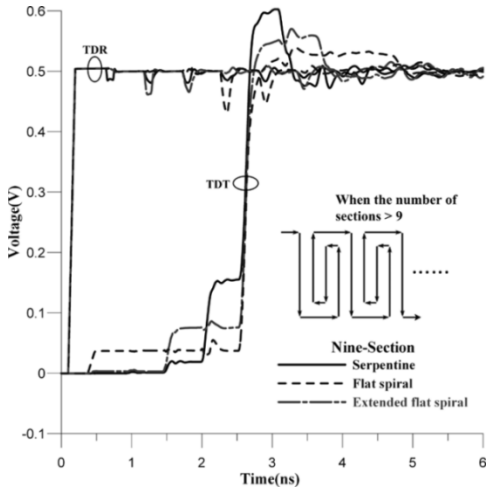


Fig. 8. Comparison of the simulated TDR/T waveforms among the differential serpentine, flat spiral, and extended flat spiral delay lines.

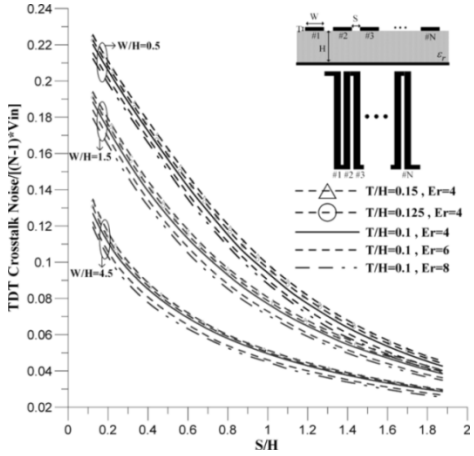


Fig. 9. Design graph of the TDT crosstalk noise versus the physical dimension of single-ended delay lines.

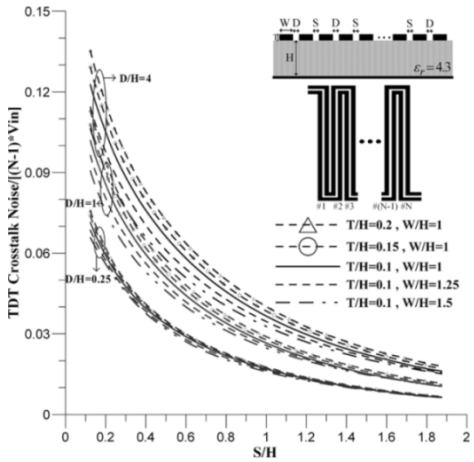


Fig. 10. Design graph of the TDT crosstalk noise versus the physical dimension of differential delay lines.

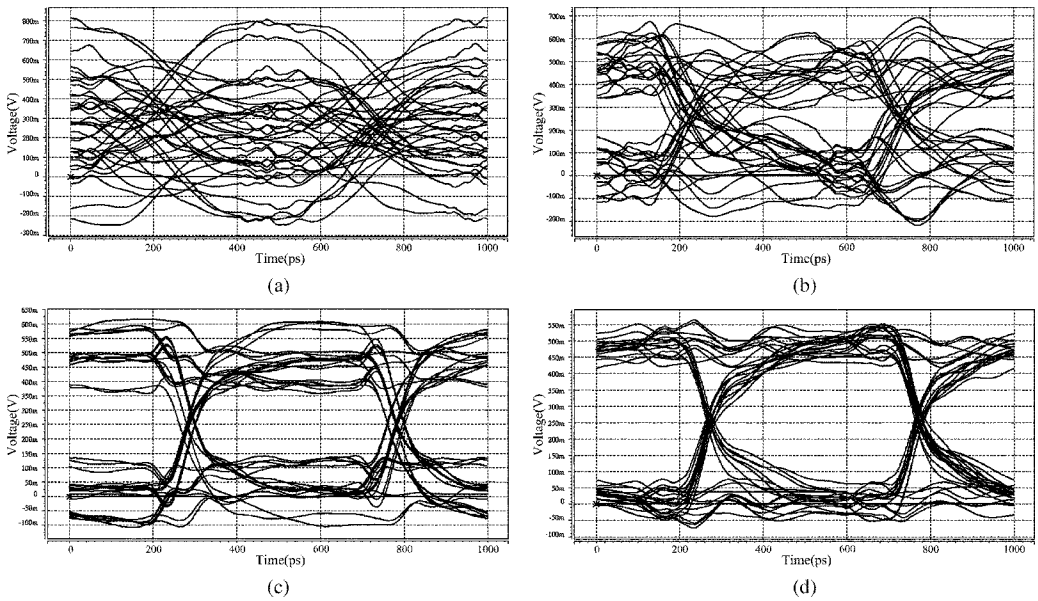


Fig. 11. TDT eye diagrams of the four delay lines. (a) Single-ended serpentine delay line. (b) Single-ended flat spiral delay line. (c) Differential serpentine delay line. (d) Differential flat spiral delay line.

## III. Crosstalk-Induced Mechanism of Differential Delay Lines

As for the differential signaling, the positive and negative signals will finally integrate to form a new signal driving the next stage of a computer system. Hence, by using the concept of pair-to-pair coupling, the crosstalk-induced mechanism of single-ended delay lines can be exactly applied to the differential delay lines. Furthermore, as the propagating signals on differential delay lines are positive-and-negative alternate, the crosstalk noise will be reduced more greatly than that of using a single-ended delay line.

Under the assumption of weak coupling in the coupled transmission lines, the main signal in the active line is rarely influenced by the presence of the crosstalk noise. Then, with respect to the input voltage, $V_{(\text{input})}$, the voltage magnitudes of saturated near-end and far-end crosstalk levels in the quiet line can be respectively formulated as [4]

$$V_{(\text{near end})} = \frac{V_{(\text{input})}}{4}\left(\frac{L_m}{L_S}+\frac{C_m}{C_S}\right)$$
$$V_{(\text{far end})} = -\frac{V_{(\text{input})}\cdot t_d}{2t_r}\left(\frac{L_m}{L_S}-\frac{C_m}{C_S}\right) \qquad (1)$$

where $L_m$ is the mutual inductance, $L_s$ is the self-inductance, $C_m$ is the mutual capacitance, $C_s$ is the self-capacitance, $t_d$ is the line delay, and $t_r$ is the rise time.

For the differential pairs of a four-conductor system with all of the ends (#1, #2, #3, and #4) matched as depicted in Fig. 4, the capacitance matrix equation is given by [5]

$$Q_i = [C_{ij}]\cdot V_j, \qquad i,j = 1,2,3,4. \qquad (2)$$

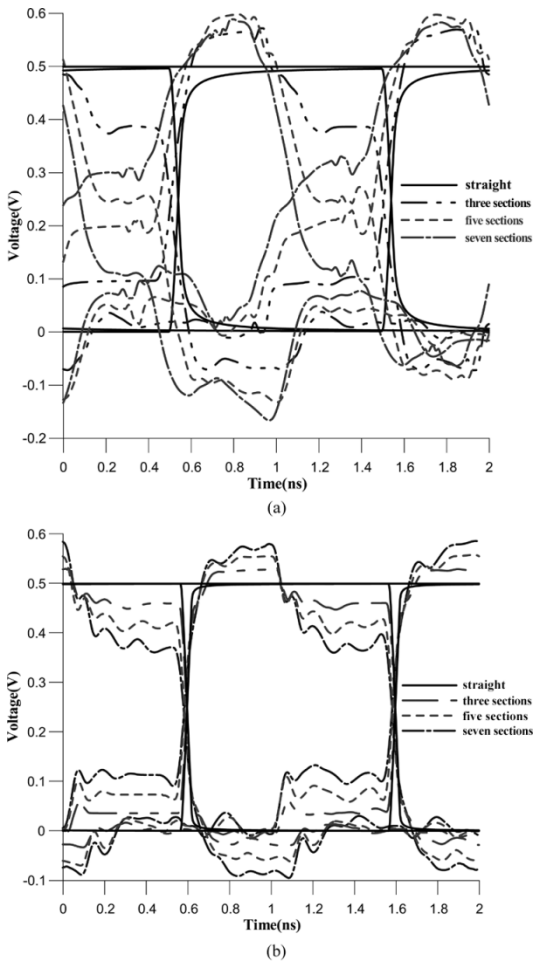


Fig. 12. TDT eye diagrams of delay lines with $S = 0.8$ mm but varying number of sections. (a) Single-ended serpentine delay line. (b) Differential serpentine delay line.

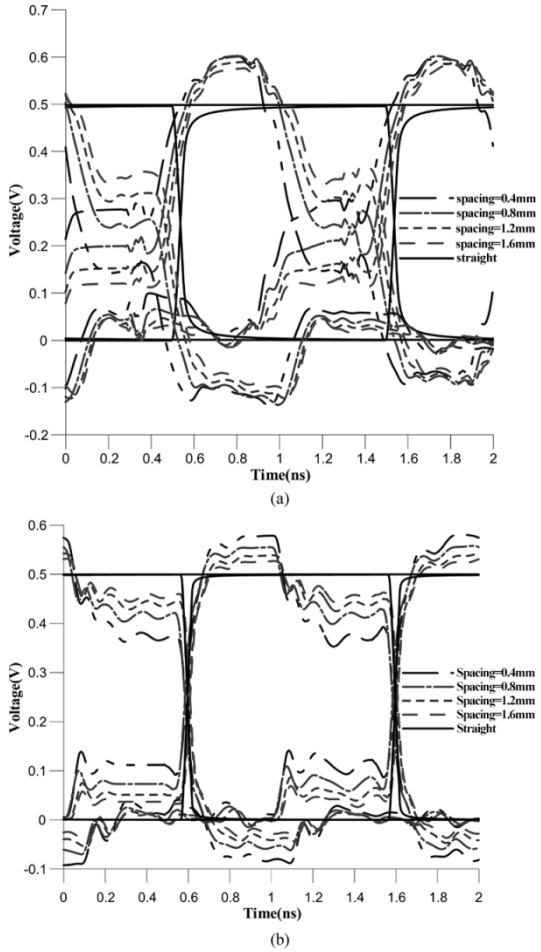


Fig. 13. TDT eye diagrams of delay lines with five sections but varying section spacings. (a) Single-ended serpentine delay line. (b) Differential serpentine delay line.

Consider the conductors #1 and #2 are driven by the differential signaling with $V_2 = -V_1$ and $Q_2 = -Q_1$, while the conductors #3 and #4 form another pair. By a simple calculation, the self-capacitance $C_s = (C_{11} + C_{22} - C_{12} - C_{21})/2$ and the mutual capacitance $C_m = (C_{13} - C_{23} - C_{14} + C_{24})/2$. Similarly, the self-inductance $L_s = (L_{11} + L_{22} - L_{12} - L_{21})/2$ and the mutual inductance $L_m = (L_{13} - L_{23} - L_{14} + L_{24})/2$. Inserting both the self and mutual capacitances and inductances into (1), the amount of crosstalk can be easily calculated.

Considering the seven-pair differential serpentine delay lines as depicted in Fig. 1(a), the cross-sectional view in Fig. 2(b) with $W = 18$ mil, $D = S = 30$ mil, $T = 2.5$ mil, and $H = 10$ mil is applied. The driver and load resistances are chosen $R_S = R_L = 50\ \Omega$ while the rise time of the source $V_S(t)$ is $t_r = 100$ ps. For simplicity, as shown in Fig. 5, the ends of two adjacent sections are connected to each other by an "ideal short" line because its influence on the simulated waveforms is not significant. Moreover, the above quantitative analysis uses the first two differential pairs here to acquire the approximate pair-to-pair capacitance and inductance. The levels of the first voltage drop at the sending end and the highest ladder before the arrival of the main signal at the receiving end can then be derived and listed in Table I, respectively. It is found that the two values agree well with those simulated by HSPICE.

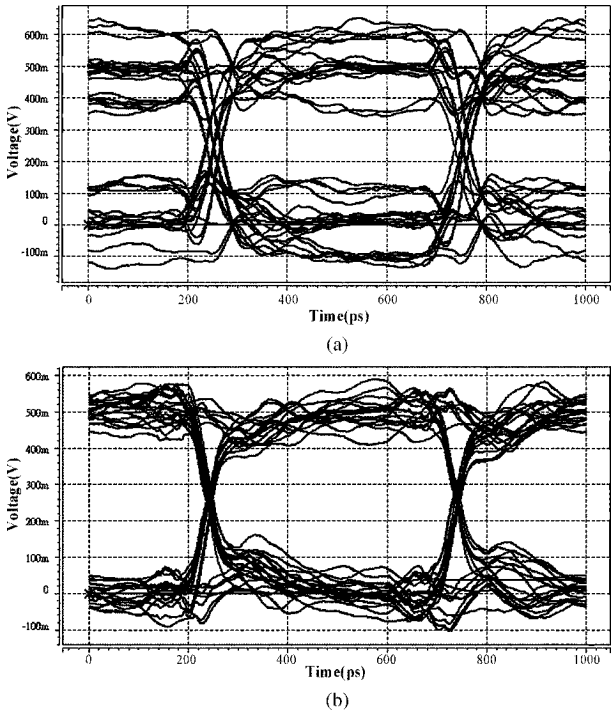


Fig. 14. TDT eye diagrams of the lossless differential delay lines. (a) Differential serpentine delay line. (b) Differential flat spiral delay line.

## IV. Simulated Waveforms and Design Graphs

Consider the single-ended and differential delay lines as depicted in Fig. 1 with the cross sections shown in Fig. 2, respectively. The physical dimensions are chosen as $W = 1.6$ mm, $D = S = 0.8$ mm, $T = 0.05$ mm, and $H = 1.5$ mm while the driving source $V_S(t)$ is a ramp pulse that reaches the steady state of unit voltage after a rise time $t_r = 100$ ps. At both the near and far ends, the simulated TDR and TDT waveforms of the single-ended serpentine and flat spiral delay lines are compared in Fig. 6. The full-wave simulation results based on the finite integration technique is presented in this figure for validity as well [7].

For a single-ended serpentine delay line, the voltage drops on the TDR waveform behaves as explained before, and the laddering wave on the TDT waveform advances the arrival time of the main signal. Despite some time shift incurred from the neglect of the discontinuities at the edges of all coupled transmission lines, the trend of TDR and TDT waveforms between HSPICE and full-wave simulation is similar. The layout design in use of a flat spiral line can reduce the crosstalk penalty on the TDT waveform but will incur much deeper voltage drops on the TDR waveform. Moreover, there is also a little difference in the total time delay, and the substrate loss may lower the level of voltage drops on the TDR waveform.

For the differential delay lines, the transient responses of positive-and-negative alternate signals are summed to form a new graph, as presented in Fig. 7. The waveforms between the single-ended and differential delay lines are alike; nonetheless, the differential delay-line design achieves much better signal integrity than does the single-ended line. In addition, the level of crosstalk noise is greatly reduced so that the time delay of a

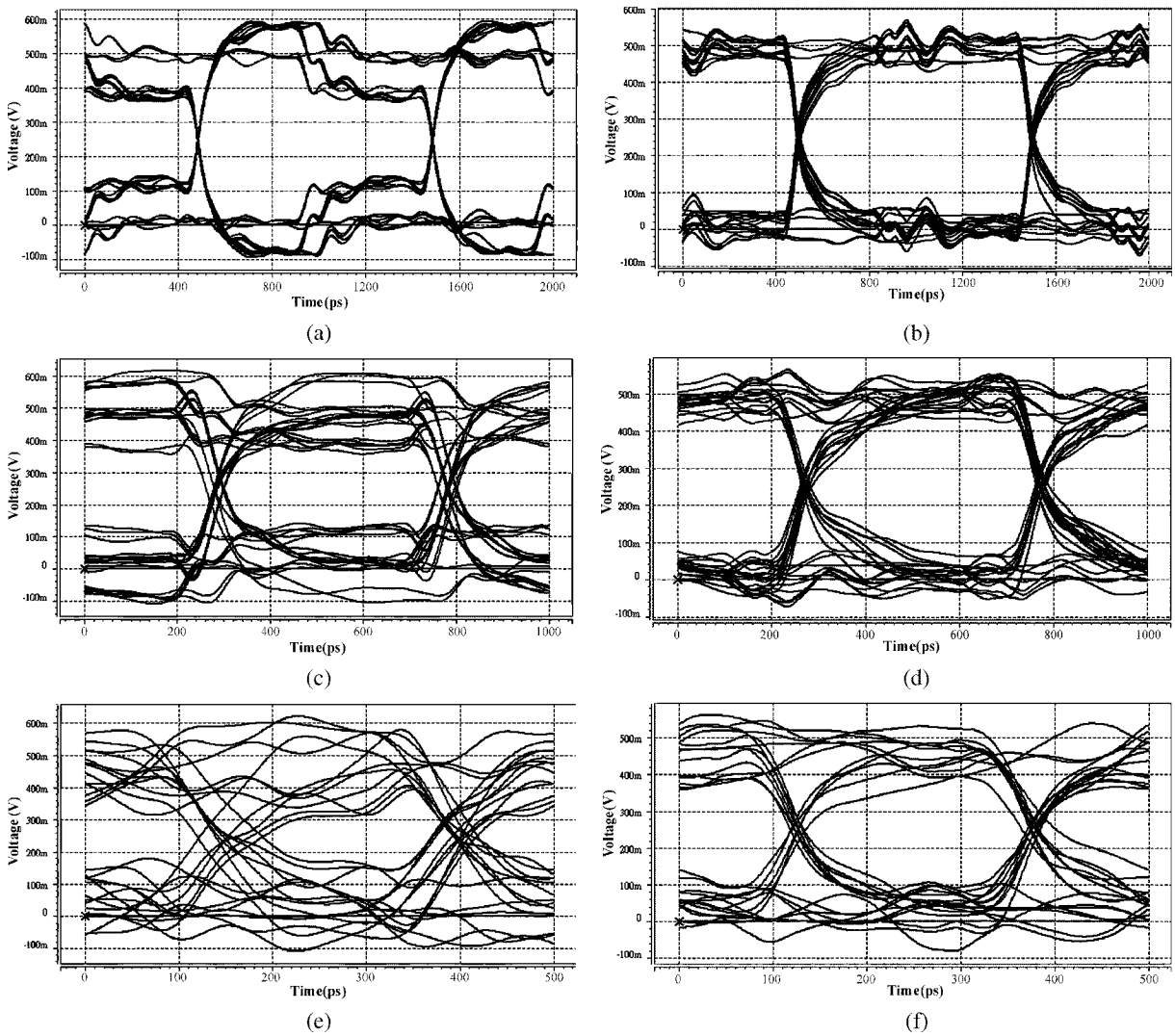


Fig. 15. TDT eye diagrams for the varying bit period with the rise time of 50 ps. (a) Bit period $=$ 1 ns for differential serpentine delay line. (b) Bit period $=$ 1 ns for differential flat spiral delay line. (c) Bit period $=$ 0.5 ns for differential serpentine delay line. (d) Bit period $=$ 0.5 ns for differential flat spiral delay line. (e) Bit period $=$ 0.25 ns for differential serpentine delay line. (f) Bit period $=$ 0.25 ns for differential flat spiral delay line.

main signal is almost the same as that of a straight-line prototype. The observation and comparison of waveforms between the single-ended and differential delay-line designs are listed in Table II accordingly.

However, if the section length of differential pairs is getting shorter and the number of sections is getting larger, the realization of the flat spiral pattern in Fig. 1(b) will become more difficult. A new routing scheme is then proposed to improve this drawback, as exemplified in Fig. 8. After comparing the simulated waveforms, it is demonstrated that the utilization of the extended flat spiral patterns could not only strengthen the feasibility of physical layout but also be a compromise between the serpentine and flat spiral schemes.

Although the quantitative analysis for evaluating the magnitude of TDT crosstalk noise for both the single-ended and differential signaling is presented, it may be time-consuming to repeat the process once the layout of delay lines is redesigned. Therefore, it is useful to give the two design graphs of TDT crosstalk noise versus the dimension for single-ended and differential delay lines. As shown in Figs. 9 and 10, the coupling degree of TDT crosstalk noise is normalized by the number of sections ($N$) and the input signal ($V_{\text{in}}$) for the sake of generality. It can also be found that the crosstalk noise induced by the differential signaling is less sensitive to the change of dimension than that of the single-ended signaling.

## V. Comparison of TDT Eye Diagrams

Owing to the capability in the crosstalk reduction by the differential signaling, there is no significant difference in the time delay of a main signal between both the differential delay lines. Nevertheless, the magnitude of TDT crosstalk noise still influences the noise margin of digital signals. In HSPICE simulation for eye diagrams, the pseudorandom incident signal is specified with rise time 50 ps, bit period 500 ps (2 Gb/s), and voltage swing 0$\sim$1 V. Recalling the four routing schemes as depicted in Fig. 1 with the cross-sectional views in Fig. 2, the simulated

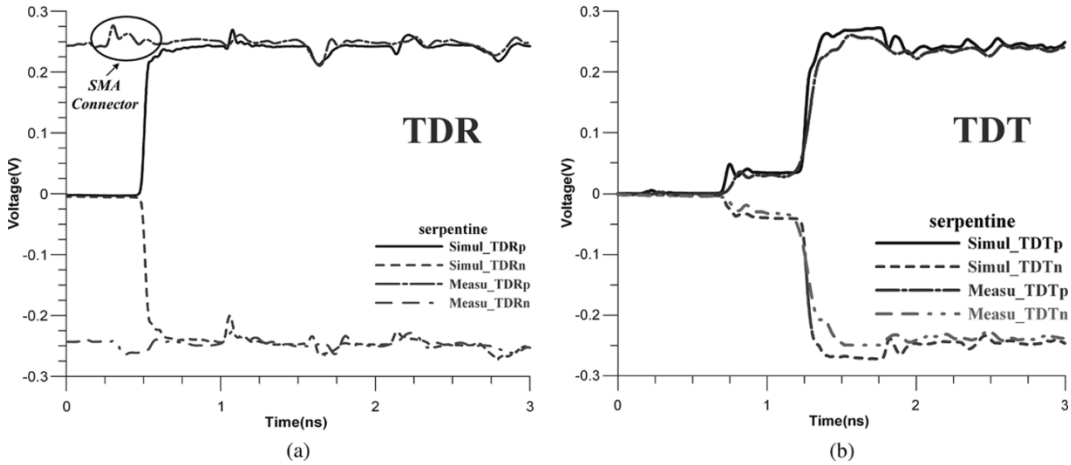


Fig. 16. Comparison between the simulated and measured waveforms of differential serpentine delay lines. (a) TDR waveforms. (b) TDT waveforms.

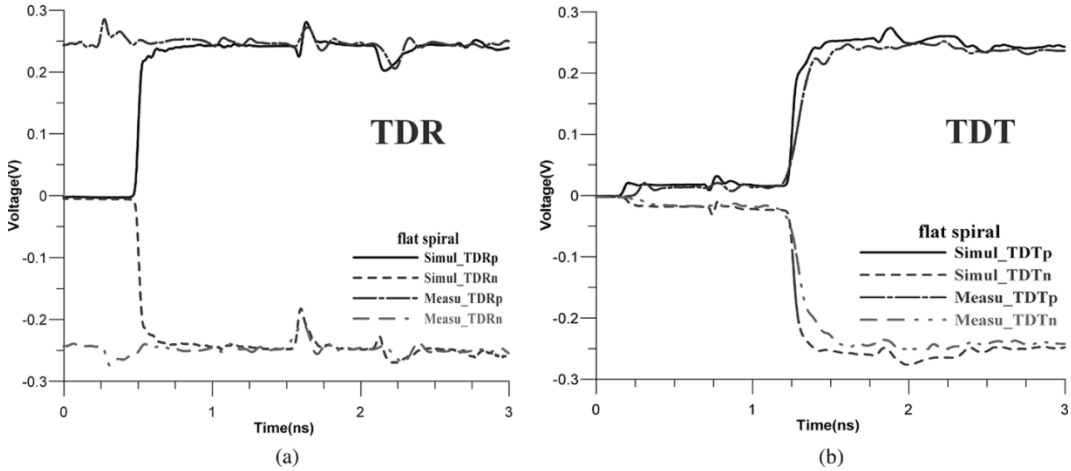


Fig. 17. Comparison between the simulated and measured waveforms of differential flat spiral delay lines. (a) TDR waveforms. (b) TDT waveforms.

results of TDT eye diagrams are shown in Fig. 11. It is apparent that the eye opening and the jitter of Fig. 11(d) is the best due to the great ability of crosstalk reduction in the differential signaling and the spreading effect of crosstalk noise in the flat spiral scheme.

As for the number of sections, which affects the accumulation of crosstalk, the TDT eye diagrams corresponding to the single-ended and differential delay lines are investigated in Fig. 12, respectively. It can be found how significantly the crosstalk deteriorates the eye opening for the single-ended serpentine delay line. The employment of differential signaling can relieve this problem significantly.

Moreover, Fig. 13 presents the TDT eye diagrams with the spacing between adjacent sections as a parameter, which affects the coupling strength. It can be seen that the eye openings are better if the spacing is larger. Furthermore, from the shape of the eye openings, the digital signal propagating on the single-ended serpentine delay line may have a greater probability of causing the error functioning of logic gates.

When the conductor and substrate loss are not taken into consideration, the simulated eye diagrams are shown in Fig. 14. All of the eye openings are similar to those of the lossy cases in reference to Fig. 11(c) and (d). This reveals that the lossy effect of transmission lines is not a key factor in affecting these eye openings.

In contrast, the bit period of a signal plays an important role. As for the varying bit periods with the fixed rise time of 50 ps, the simulated eye diagrams of delay lines are shown in Fig. 15. Note that the smaller the bit period, the worse the eye opening.

## VI. Experimental Verification

The comparison of simulated and measured waveforms for the single-ended delay lines with the serpentine and flat spiral pattern has been demonstrated in [1] and [2]. As for the five-section differential serpentine and flat spiral delay lines having the cross section with $W = 1.8$ mm, $D = S = 0.8$ mm, $T = 0.05$ mm, $H = 1.5$ mm, substrate material of $\varepsilon_r = 3.38$, and loss tangent $= 0.0022$, the experimental verification performed on the time domain reflectometer TEK/CSA8000 is presented. With both the source and load resistances at 50 $\Omega$, the launching voltage source is drawn out of the reflectometer for the HSPICE simulation.

As compared in Figs. 16 and 17, it is evident that the simulated waveforms agree well with the measured ones except at the rising edges of TDT signals. The deviations found in

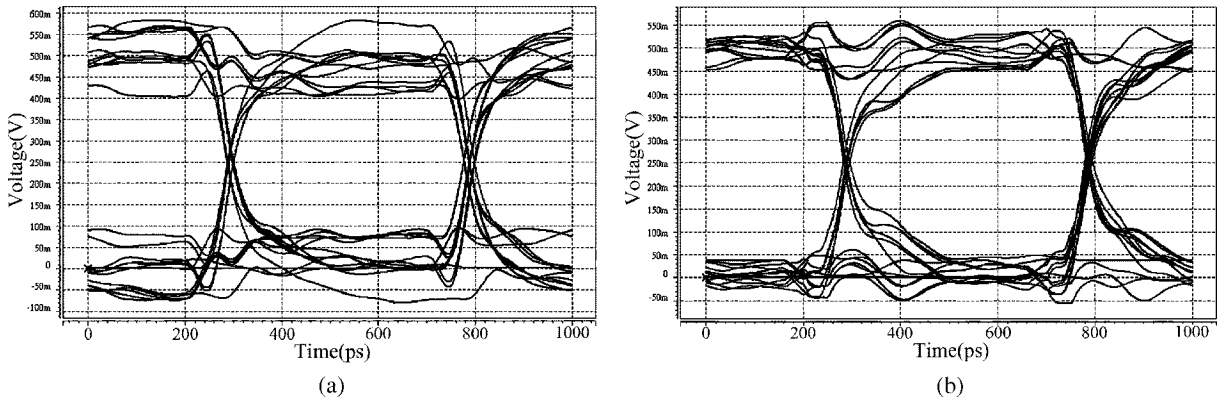


Fig. 18. Simulated eye diagrams of the five-section differential delay lines. (a) Differential serpentine delay line. (b) Differential flat spiral delay line.

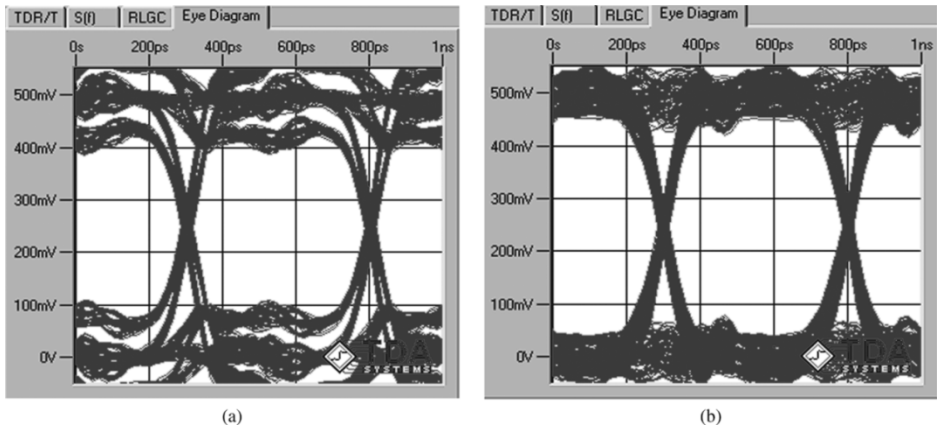


Fig. 19. Measured eye diagrams of the five-section differential delay lines. (a) Differential serpentine delay line. (b) Differential flat spiral delay line.

HSPICE simulations are attributed to the negligence of additional high-frequency loss on the coaxial cable and the skin-effect resistance and equivalent capacitance and inductance near the corners of delay lines.

Furthermore, the measured waveforms are imported into the time-domain simulator IConnect [8] to obtain the individual eye diagrams in comparison with the simulated data by HSPICE. It is found that the consistency is good in reference to Figs. 18 and 19. Although the slight discrepancy exists, the results acquired by the trace model, quantitative analysis, simulation, and measurement have justified the presence of crosstalk noise on the differential delay lines. Accordingly, the investigation in this paper shows that the resultant TDR and TDT waveforms of differential delay lines suffer from the less signal distortion and delay penalty than those of the single-ended delay lines.

## VII. Conclusion

On the single-ended serpentine delay line, the magnitude of the laddering wave may grow up to a significant level before the arrival of the main signal. In use of the single-ended flat spiral routing scheme for delay-line designs, the crosstalk penalty on the TDT waveform can be greatly alleviated but with the deteriorated TDR waveform as a tradeoff. This paper extends the laddering wave analysis to the differential signals and proposes an extended flat spiral pattern to assure the routing feasibility in the layout designs. It is found that the physical mechanism of differential delay lines can be treated as that of single-ended delay lines if the concept of pair-to-pair coupling is introduced. The magnitude of TDR and TDT crosstalk noise can be easily calculated by the derived formula or design graphs furthermore.

As demonstrated on the HSPICE simulations, the differential signaling can significantly reduce the crosstalk noise on both TDR and TDT waveforms against those in use of the single-ended signaling. The combination of the flat spiral routing and differential signaling can further improve the signal integrity to obtain the best eye openings. In addition, the number of sections, the spacing between adjacent sections, and the bit period of a signal are major parameters in determining the signal integrity and should be carefully considered in the design of delay lines.

## References

[1] R. B. Wu and F. L. Chao, "Laddering wave in serpentine delay line," *IEEE Trans. Comp., Pkg., Manuf. Technol., B*, vol. 18, no. 4, pp. 644–650, Nov. 1995.

[2] ——, "Flat spiral delay line design with minimum crosstalk penalty," *IEEE Trans. Comp., Pkg., Manuf. Technol., B*, vol. 19, no. 2, pp. 397–402, May 1996.

[3] W. D. Guo, G. H. Shiue, and R. B. Wu, "Comparison between flat spiral and serpentine differential delay lines on TDR and TDT," in *Proc. IEEE 13th Topical Meeting Elect. Perform. Electro. Packag.*, Oct. 2004, pp. 147–150.

[4] S. H. Hall, G. W. Hall, and J. A. McCall, *High-Speed Digital System Design, A Handbook of Interconnect Theory and Design Practices*. Hoboken, NJ: Wiley, 2000, ch. 3, p. 48.

[5] W. T. Weeks, "Calculation of coefficients of capacitance of multi-conductor transmission lines in the presence of a dielectric interface," *IEEE Trans. Microw. Theory Tech.*, vol. MTT-18, no. 1, pp. 35–43, Jan. 1970.
[6] B. J. Rubin and B. Singh, "Study of meander line delay in circuit boards," *IEEE Trans. Microw. Theory Tech.*, vol. 48, no. 9, pp. 1452–1460, Sep. 2000.
[7] *"CST Microwave Studio Manual"* Computer Simulation Technology, Germany, 2003 [Online]. Available: www.cst.com
[8] IConnect TDA Systems, Inc. [Online]. Available: www.tdasystems.com

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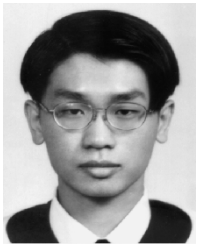

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