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著者 Author(s)	Takiguchi, Naoya / Koba, Shunsuke / Tsuchiya, Hideaki / Ogawa, Matsuto
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Comparisons of Performance Potentials of Si Nanowire and InAs Nanowire MOSFETs under Ballistic Transport

Naoya Takiguchi[1], Shunuske Koba[1], Hideaki Tsuchiya[1,2], *Senior Member*, *IEEE*, and Matsuto Ogawa[1], *Senior Member*, *IEEE*

[1]Department of Electrical and Electronic Engineering, Graduate School of Engineering, Kobe University
1-1, Rokko-dai, Nada-ku, Kobe 657-8501, Japan

[2]Japan Science and Technology Agency, CREST, Chiyoda, Tokyo 102-0075, Japan

In this paper, we study the band structures of Si and InAs nanowires based on a first-principles calculation, and project performance potentials of Si and InAs nanowire field-effect-transistors (NWFETs) by using a semi-classical ballistic transport model. We demonstrate that the device performance of InAs NWFETs strongly depends on its cross sectional dimension and gate oxide thickness. In particular, InAs NWFETs unexpectedly indicate the lower current drivability than Si NWFETs as the gate oxide thickness is extremely scaled down to 0.5 nm, in the ballistic limit. We discuss the mechanism in terms of operation in quantum capacitance limit (QCL). We also demonstrate that the advantage in a lower power operation with InAs NWFETs reduces when the devices operate in the QCL or higher subbands with heavier transport effective mass participate in the transport.

***Index Terms*—nanowire transistors, high mobility semiconductors, first-principles calculation, ballistic transport, quantum capacitance, power-delay-product**

I. Introduction

NANOWIREs are one-dimensional nanostructures with carriers confined in the two directions normal to transport. They exhibit interesting physical properties that are noticeably different from those of the bulk and quantum wells. Of particular importance in technology are semiconductor nanowires that have potential applications in many fields such as optoelectronics, sensors, and especially integrated logic circuits. Several experimental studies have shown that Si nanowire metal-oxide-semiconductor field-effect transistors (MOSFETs) have excellent electrical properties, e.g., small short-channel effects (SCEs), particularly in a gate-all-around (GAA) configuration [1-4]. Therefore, conventional planar MOSFETs could be replaced by Si nanowire MOSFETs (NWFETs) in the future, if their promising performances are concretized. On the other hand, III-V semiconductor nanowires have recently received much attention because of their higher electron mobility and lower effective mass [5]. However, although better electron transport properties are expected with III-V materials, Si has remained the material of choice to fabricate GAA NWFETs due to its well-understood characteristics and compatibility to conventional CMOS technology [4].

In accordance with the progress in fabrication technique, a simulation approach beyond semi-classical models based on an effective mass approximation has become indispensable, because nanoscale devices are characterized by three-dimensional (3D) material properties varying at the atomistic scale. Recently, a 3D atomistic quantum transport simulator based on a nonequilibrium Green's function model has been developed to explore NWFETs [4]. It can provide accurate and detailed device performances of NWFETs in the presence of interface roughness, electron-phonon and impurity scatterings. However, it requires huge computational resources, and thus it seems to be unfit for a systematic investigation of the performance of NWFETs with various operating conditions and different channel materials.

In this paper, we address a performance comparison between Si and InAs *n*-channel NWFETs under the ideal ballistic transport. To this end, we employed a first-principles band structure calculation and a top-of-the-barrier (ToB) ballistic MOSFET model [6], where the ToB model is simple and can readily assess an upper limit performance of atomistic transistors, if once we obtain the band structure numerically or analytically. First, we calculated the band structures of hydrogen-passivated Si and InAs nanowires by using the Vienna *ab initio* simulation package (VASP) [7], within the generalized-gradient approximation (GGA) interactions. We adopted the <110>-crystal orientation as the transport direction because of the superior transport characteristics compared with other crystal orientations [8-10] and the highest immunity to interface roughness scattering reported in Si nanowires [11]. Then, we estimated the electrical characteristics of Si and InAs NWFETs by incorporating their first-principles band structures into the ToB model. We demonstrate strong dependency of the device performance of InAs NWFETs on its cross sectional dimension and gate oxide thickness, and the mechanism is discussed in terms of band structure modulation and quantum capacitance.

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The authors are with the Department of Electrical and Electronic Engineering, Graduate School of Engineering, Kobe University, 1-1, Rokko-dai, Nada-ku, Kobe 657-8501, Japan (e-mail: 101t236t@stu.kobe-u.ac.jp, 108t224t@stu.kobe-u.ac.jp, tsuchiya@eedept.kobe-u.ac.jp, ogawa@eedept.kobe-u.ac.jp). This work was supported by Grant-in-Aid for Scientific Research from the Japan Society for the Promotion of Science (JSPS), and the Japan Science and Technology Agency (JST)/CREST.

II. Bandstructures of Si and InAs Nanowires

We use square-shaped Si and InAs nanowires grown in the <110>-direction as shown in the insets of Fig. 1, where quantum confinement directions are $\langle 001 \rangle$ and $\langle 1\bar{1}0 \rangle$, and their actual dimensions (W) are also indicated in the insets. The integers m and n in parentheses ($m \times n$) denote the number of atoms in the $\langle 001 \rangle$ and $\langle 1\bar{1}0 \rangle$-directions, respectively. We considered two different cross sections of $W \approx 2$ nm and 3 nm both for Si and InAs nanowires. Zinc blende structure was adopted for InAs nanowires [10,12]. All surface dangling bonds are passivated by hydrogen (H) atoms, and their positions were carefully adjusted to obtain the most stable electronic states of the nanowires. For Si nanowires, Si-H distance was set at 1.43 Å, while for InAs nanowires In-H and As-H distances were 1.76 Å and 1.52 Å, respectively. The band structures were computed by using VASP [7] within the GGA exchange-correlation interactions. The cut-off energy was set at 250 eV both for Si and InAs nanowires, and a k-point mesh with $4 \times 4 \times 1$ Monkhorst Pack special points was used. A convergence condition for the self-consistent field was set at 10^{-5} eV, which was successfully accomplished in all simulations. The conduction band structures computed for the Si nanowires and the InAs nanowires are plotted in Fig. 1 (a) and (b), respectively, where in each case the conduction band minimum is set at $E = 0$. The valence band structures are omitted, since we examine n-channel NWFETs in this study. According to previous theoretical calculations, InAs nanowires with cross sections of 4 nm or less have bandgaps of 0.8 eV or more [10,12,13]. Consequently, we can neglect band-to-band tunneling leakage current at an off-state bias, which will not be included in the ToB model, by choosing a drain bias voltage sufficiently small. As seen in Fig. 1 (a), the Si nanowires have conduction band minimum at the Γ point

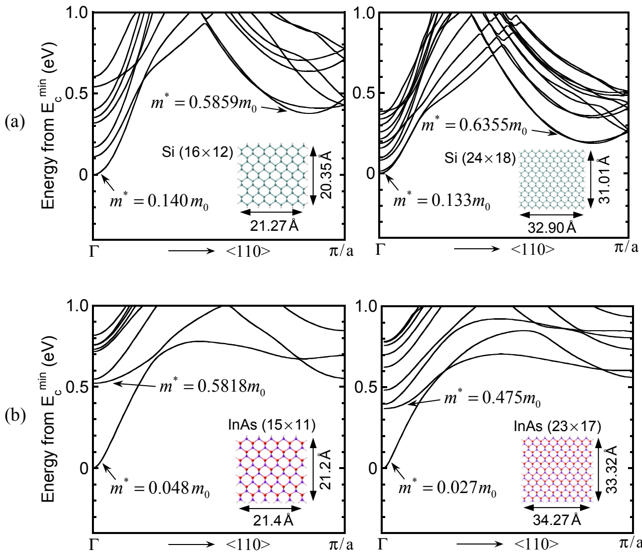

Fig. 1. Conduction band structures computed for (a) Si nanowires and (b) InAs nanowires with two different cross sections of about 2 nm and 3 nm. In each case, the conduction band minimum is set at $E = 0$. The insets show atomic models used in the simulations for Si and InAs nanowires grown in the <110>-direction. Electron effective masses of the lowest subbands and the higher subbands with smaller curvatures are also indicated in each figure.

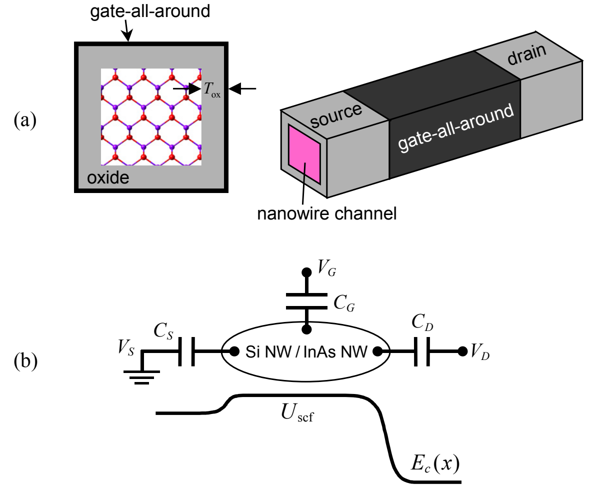

Fig. 2. (a) Schematic diagrams of simulated GAA NWFETs and (b) ToB model used to calculate electrical characteristics. The gate insulator is assumed to be SiO_2 with two different thicknesses of $T_{ox} = 3$ nm and 0.5 nm.

due to the k-space projection of the bulk six ellipsoidal bands onto the two quantization planes [8,9,14]. The electron effective masses of the lowest subbands at the Γ point are also shown in each figure. As previously reported in several literatures [8,9,14], the <110>-oriented Si nanowires have transport mass around 0.13 ~ 0.14 m_0, which is smaller than the bulk transverse mass of $m_t = 0.19$ m_0. On the other hand, the <110>-oriented InAs nanowires have an increasing transport mass with decreasing wire width [10,12,13]. Our effective masses of the InAs nanowires fall within reasonable range compared to that estimated by an eight-band $k \cdot p$ model [13], although the different wire orientation, <100>-orientation, is used in [13].

Furthermore, the effective masses of higher subbands with smaller curvatures are indicated in each figure of Fig. 1. For Si nanowires, they originally result from the 4-fold equivalent valleys located near the X point in bulk Si, and appear around the X point even in the <110>-oriented nanowires [8,9,14], as shown in Fig. 1 (a). On the other hand, for InAs nanowires they appear at the Γ point as shown in Fig. 1 (b). This is because the L valleys in bulk InAs are folded onto the Γ point due to the k-space projection. As seen in Fig. 1, those higher subbands lower to approach the lowest subband with increasing the nanowire cross section. Therefore, if electrons occupy those higher subbands by increasing the gate voltage or increasing the cross section, the electrical performances are influenced by their heavier transport mass. We will also discuss this point in the next section.

For reference, we examined Si and InAs nanowires with a smaller cross section and found that the transport mass of the InAs nanowire increases to 0.129 m_0 for $W \approx 1$ nm, which is almost the same as that of the Si nanowires with $W = 1 \sim 3$ nm. Therefore, Si and InAs NWFETs will exhibit similar device performances at around $W \approx 1$nm, although we do not include further discussion on the devices with $W \approx 1$nm in this paper.

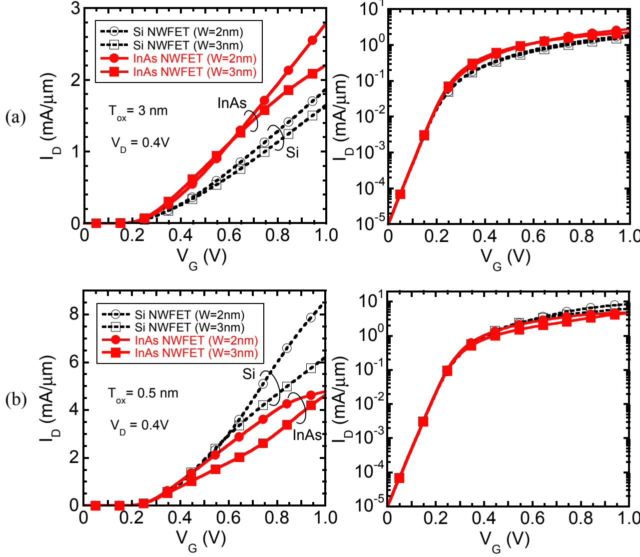

Fig. 3. I_D - V_G characteristics computed for (a) T_{ox} = 3 nm and (b) 0.5 nm, where the left and right figures represent linear plot and logarithm plot of drain current, respectively. Note that the vertical axis denotes drain current density normalized by perimeter of nanowires, to make a comparison under the same gate electrostatics. V_D = 0.4V. I_{OFF} = 0.01 μA/μm.

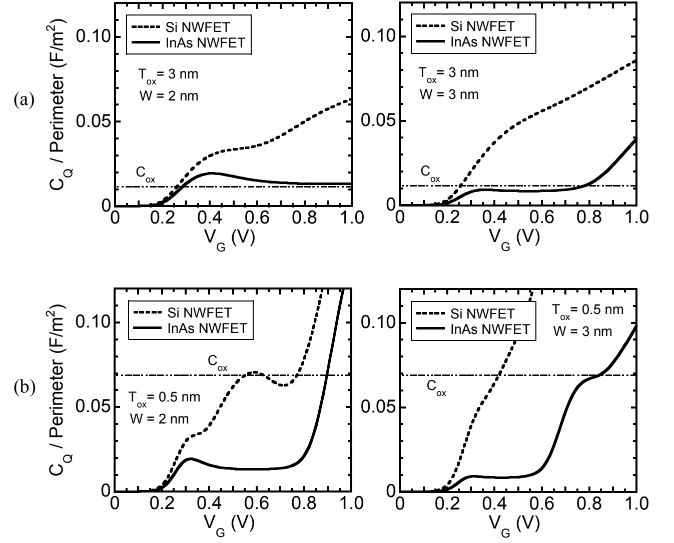

Fig. 4. Computed quantum capacitances as a function of gate voltage corresponding to I_D - V_G characteristics in Fig. 3, where (a) T_{ox} = 3 nm and (b) 0.5 nm. The results for $W \approx$ 2 nm and 3 nm are separately plotted. The vertical axis denotes quantum capacitance normalized by perimeter of nanowires. Since the quantum capacitance is calculated per unit length along channel as described in the text, the normalized quantum capacitance has the unit of [m^2]. The horizontal dashed lines represent oxide capacitances determined by $C_{ox} = \varepsilon_{ox} / T_{ox}$.

III. Comparisons of Performance Potentials of Si and InAs NWFETs

Fig. 2 shows (a) the schematic diagrams of simulated GAA NWFETs and (b) the ToB model used to calculate the electrical characteristics in the ballistic limit. In the present ToB model, any scattering mechanisms including surface roughness scattering at the Si/SiO_2 interface are not considered. Although this assumption seems impractical, the model intends to investigate the performance potentials of NWFETs with ultimately-scaled channel length, by considering atomistic band structures. The Si and InAs nanowires with $W \approx$ 2 nm and 3 nm, which were simulated in the previous section, are employed as the channel materials, and the gate insulator is assumed to be SiO_2 with two different thicknesses of T_{ox} = 3 nm and 0.5 nm. The drain voltage is set at 0.4 V, which is sufficiently small so that the band-to-band tunneling leakage current at the off-state bias can be neglected. The donor density in source and drain is taken as 1.0 × 10^{20} cm^{-3} for Si NWFETs and 2.0 × 10^{19} cm^{-3} for InAs NWFETs, considering the maximum doping concentration limited by the solid solubility of donors [15,16]. We assumed perfect electrostatic gate control over the channel, i.e., $C_D / C_G, C_S / C_G = 0$. However, coupling between channel and source/drain may become more serious in InAs NWFETs, because of the smaller maximum donor concentration as mentioned above. It will be an important subject for a further study.

Fig. 3 shows the I_D - V_G characteristics computed for (a) T_{ox} = 3 nm and (b) 0.5 nm, where the results for four different devices, that is, the Si and InAs NWFETs with the two cross sections, are plotted together in each figure. The vertical axis denotes the drain current density normalized by the perimeter of nanowires, to make a comparison under the same gate electrostatics. The OFF-current density is set at 0.01 μA/μm in the present simulations. As seen in the right figures of Fig. 3, the subthreshold slope is ideal for all devices, and thus they have the same threshold voltage V_t as well. First of all, we note that for T_{ox} = 3 nm the InAs NWFETs exhibit higher drain current than the Si NWFETs, as expected from the smaller transport effective mass of the lowest subband. By closely looking at Fig. 3 (a), the InAs NWFET with $W \approx$ 3 nm exhibits slightly larger drain current than the one with $W \approx$ 2 nm until $V_G \approx$ 0.55 V because of the smaller effective mass, but the situation is opposite beyond $V_G \approx$ 0.7 V. This is due to electron occupation of the higher subband with the heavier transport effective mass in the InAs NWFET with $W \approx$ 3 nm as discussed later. Here, it is particularly worth noting that as the gate oxide thickness reduces to T_{ox} = 0.5 nm the drain current of the InAs NWFETs becomes smaller than the Si NWFETs for both cross sections. Such unexpected inferiority in the InAs NWFETs is considered due to a quantum capacitance of nanowire channels, as discussed below.

Fig. 4 shows the computed quantum capacitances as a function of gate voltage corresponding to the I_D - V_G characteristics in Fig. 3, where the results for $W \approx$ 2 nm and 3 nm are separately plotted. The vertical axis denotes the quantum capacitance normalized by the perimeter of nanowires. The horizontal dashed lines represent oxide capacitances determined by $C_{ox} = \varepsilon_{ox} / T_{ox}$. The quantum capacitance was calculated by $C_Q = \partial (qN) / \partial (-U_{scf} / q)$, where qN and U_{scf} are the charge density per unit length along the channel and the potential energy at the top of the barrier, respectively [6,10,12]. First, for T_{ox} = 3 nm the C_Q's are larger than or comparable to the C_{ox} as shown in Fig. 4 (a), and thus

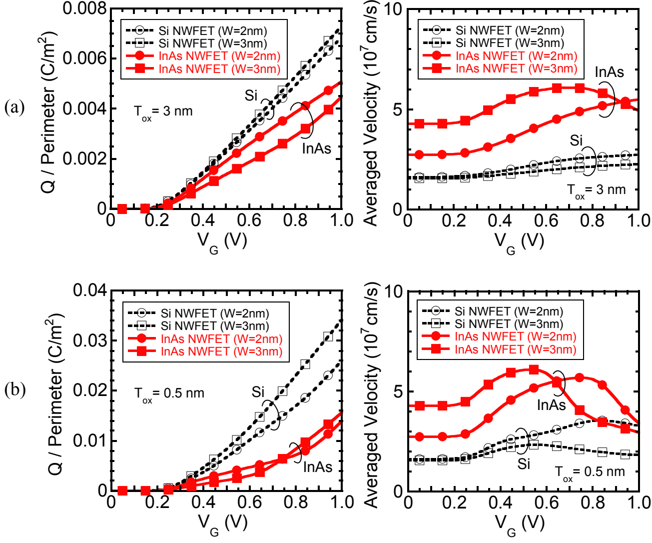

Fig. 5. Computed channel charge densities normalized by perimeter of nanowires (left column) and averaged electron velocities (right column) as a function of gate voltage, where (a) T_{ox} = 3 nm and (b) 0.5 nm.

both the Si and InAs NWFETs can be assumed to operate in the classical capacitance limit (CCL). As a result, the I_D - V_G characteristics are basically governed by the transport effective mass of the lowest subband, and the InAs NWFETs with smaller transport mass indicate the higher drain current as shown in Fig. 3 (a). In contrast, as seen in Fig. 4 (b) the InAs NWFETs with T_{ox} = 0.5 nm are found to be nearly operating in the quantum capacitance limit (QCL), since their C_Q's are significantly smaller than the C_{ox} in the wide range of gate bias. Consequently, the total gate capacitance becomes approximately equal to C_Q, and the channel charge density substantially decreases. Here, the rapid increase in the C_Q's of the InAs NWFETs at high gate voltages is attributed to the beginning of the electron occupation of the higher subband with heavier transport mass. In the QCL, the potential within the channel is moved efficiently by increasing the gate voltage unlike the CCL [17], and hence the higher subband can be easily involved with the electron transport. This is a unique feature of one-dimensional nanowire structures having small density-of-states.

To confirm the fact that the channel charge density substantially decreases in the QCL, we actually computed the channel charge density Q as a function of gate voltage as shown in the left column of Fig. 5, where the vertical axis denotes the charge density normalized by the perimeter of nanowires. Note that we compare charge density per unit length, so the channel length is irrelevant to the present discussion. First, we recognize that the InAs NWFETs have smaller charge density than the Si NWFETs for both T_{ox}'s, but a further marked reduction is observed in the case of T_{ox} = 0.5 nm. This represents that the InAs NWFETs with T_{ox} = 0.5 nm actually operate in the QCL, and hence the induced charge density is drastically decreased [18]. On the other hand, as shown in the right column of Fig. 5, the averaged electron velocity is larger in the InAs NWFETs for both T_{ox}'s, although

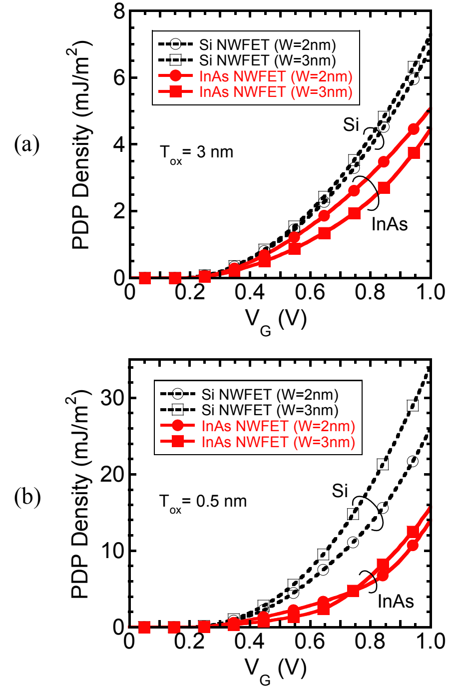

Fig. 6. Computed PDP densities as a function of gate voltage for (a) T_{ox} = 3 nm and (b) 0.5 nm, where V_D = 0.4 V. The vertical axis denotes PDP density divided by in-plane device area, and channel length is set as 10 nm.

it decreases when electrons begin to occupy the higher heavy subband [18]. This indicates that the lower drain current in the InAs NWFETs with T_{ox} = 0.5 nm observed in Fig. 3 (b) is primarily due to the drastic reduction in the channel charge density because of the QCL operation. Incidentally, the increase in the averaged velocity of the $W \approx$ 2nm Si NWFET with increasing the gate voltage is due to the absence of electron occupation in higher subband with heavier transport mass. Then, it contributes to increase the drain current of the $W \approx$ 2nm Si NWFET as shown in Fig. 3.

As presented above, InAs NWFETs unexpectedly exhibit a smaller current drive than Si NWFETs in the QCL. On the other hand, performance improvement in terms of power-delay-product (PDP) may be expected due to the QCL operation [13,17,19]. Then, we next investigate the PDP characteristics. Since the PDP represents the energy required for switching a device, we calculate it by $\mathrm{PDP} = I_{ON} V_{DD} \times (Q_{ON} - Q_{OFF}) / I_{ON} = (Q_{ON} - Q_{OFF}) V_{DD}$, which corresponds to charging of the MOS capacitor under the bias voltage V_{DD} [20]. Here, Q_{ON} and Q_{OFF} indicate the total charge densities in the channel at on-state and off-state, respectively. In this study, the off-state is always set at V_{DD} = 0 V, that is, $Q_{OFF} = Q$ (V_{DD} = 0 V). In addition, since the drain voltage hardly affects the on-state and off-state in the ballistic limit and we assumed perfect electrostatic gate control over the channel, V_{DD} was substituted with the gate voltage V_G in the present estimation. Fig. 6 shows the computed PDP densities as a function of gate voltage for (a) T_{ox} = 3 nm and (b) 0.5 nm, where V_D = 0.4 V. The vertical axis denotes the PDP density divided by the in-plane device area, and the channel length is

Table 1. PDP densities for (a) T_{ox} = 3 nm and (b) 0.5 nm, computed at I_{ON} = 1.5 mA/μm. The NWFETs with $W \approx 3$ nm are considered, while the results for $W \approx 2$ nm are also indicated in parentheses. The rightmost column indicates ON-current densities under the same PDP density as that of Si NWFET. In (c), PDP densities computed at I_{ON} = 2.5 mA/μm are shown, where T_{ox} is given as 0.5 nm.

(a)

T_{ox} = 3 nm	I_{ON} = 1.5 (mA/μm)		PDP = 6.34 (mJ/m^2) (PDP = 4.97 (mJ/m^2))	
Si NWFET	PDP (mJ/m^2)	6.34 (4.97)	I_{ON} (mA/μm)	1.50 (1.50)
InAs NWFET		1.77 (2.20)		2.45 (2.75)
Ratio	InAs/Si	0.28 (0.44)	InAs/Si	1.63 (1.83)

(b)

T_{ox} = 0.5 nm	I_{ON} = 1.5 (mA/μm)		PDP = 3.04 (mJ/m^2) (PDP = 2.65 (mJ/m^2))	
Si NWFET	PDP (mJ/m^2)	3.04 (2.65)	I_{ON} (mA/μm)	1.50 (1.50)
InAs NWFET		1.30 (1.47)		2.21 (2.44)
Ratio	InAs/Si	0.43 (0.55)	InAs/Si	1.47 (1.63)

(c)

T_{ox} = 0.5 nm	I_{ON} = 2.5 (mA/μm)		PDP = 5.95 (mJ/m^2) (PDP = 4.89 (mJ/m^2))	
Si NWFET	PDP (mJ/m^2)	5.95 (4.89)	I_{ON} (mA/μm)	2.50 (2.50)
InAs NWFET		4.22 (2.77)		2.88 (3.68)
Ratio	InAs/Si	0.71 (0.57)	InAs/Si	1.15 (1.47)

set as 10 nm. It is found that the InAs NWFETs have smaller PDP density as compared to the Si NWFETs for both T_{ox}'s. Particularly, in the case of T_{ox} = 0.5 nm, it exhibits a markedly smaller PDP density as shown in Fig 6 (b), which is definitely caused by the smaller channel charge density, that is, the smaller current drive, due to the QCL operation. Therefore, to make a reasonable comparison in power and performance, the PDP densities should be compared under the same I_{ON} condition by adjusting the bias voltage V_G.

Then, Table 1 (a) and (b) compare the PDP densities between Si and InAs NWFETs computed at I_{ON} = 1.5 mA/μm for T_{ox} = 3 nm and 0.5 nm, respectively. Here, the devices with $W \approx 3$ nm are considered, while the results for $W \approx 2$ nm are also indicated in parentheses. It is found that the reduction ratio in the PDP density increases from 0.28 to 0.43 by reducing T_{ox} from 3 nm to 0.5 nm. This means that the advantage in the lower power operation with InAs NWFETs reduces when the device operates in the QCL, although the power is still saved up to more than 50 % by using InAs nanowire channel with $W \approx 3$ nm even in the QCL. In Table 1, we also compare ON-current densities under the same PDP density as that of Si NWFET, of which data are listed in the rightmost column. The results indicate that the QCL operation (T_{ox} = 0.5 nm) also restrains a current enhancement by using InAs nanowire channel.

It is also important to assess the figure of merit in InAs NWFETs having I_{ON} exceeding 2 mA/μm. To this end, we estimated PDP densities at I_{ON} = 2.5 mA/μm as shown in Table 1 (c), where T_{ox} is given as 0.5 nm to reduce the bias voltage below 1.0 V. Here, it is worth pointing out that the advantage of InAs NWFETs drastically reduces, i.e., the power reduction ratio drastically increases to 0.71 and the current drive enhancement is limited to only 1.15. This is due to the participation of the higher subband with the heavier transport effective mass as mentioned before.

Furthermore, for the NWFETs with $W \approx 2$ nm, the power reduction ratio does not change drastically due to T_{ox} and I_{ON}, as seen in the parenthetic numbers of Table I. This is because the effective mass of the InAs nanowire increases in $W \approx 2$ nm and also the higher subband with heavier transport mass is elevated, as previously stated in Fig. 1 (b). Consequently, the influences of the quantum capacitance and the higher subband are mitigated in the case of $W \approx 2$ nm. The above results indicate that the roles of the quantum capacitance and higher subband with heavier transport mass are crucial to determine the superiority of InAs NWFETs over Si NWFETs, as a projection under the ideal ballistic transport.

IV. Conclusion

In conclusion, we have found that the device performance of InAs NWFETs strongly depends on the gate oxide thickness T_{ox}. That is, for T_{ox} = 3 nm the InAs NWFET indicates the higher drain current than the Si NWFET, but on the contrary it degrades to indicate the lower current drivability for T_{ox} = 0.5 nm. We have discussed the mechanism and found that the drain current degradation in the InAs NWFET is primarily due to the QCL operation caused by extremely scaling T_{ox}.

However, the QCL requires much smaller charge density for switching a device, and thus even in the QCL, lower power switching operation in InAs NWFETs than in Si NWFETs was verified by comparing the PDP densities under the same on-current condition. On the other hand, we have also found that the advantage in the lower power operation with InAs NWFETs significantly reduces when the devices operate in the QCL or higher subbands with heavier transport effective mass participate in the transport. Therefore, the influences of the quantum capacitance and higher subbands with heavier transport mass should be precisely taken into account in practical design of III-V semiconductor NWFETs.

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Naoya Takiguchi was born in Osaka, Japan, on June 20, 1987. He received the B. S. degree in electrical and electronics engineering from Kobe University, Kobe, Japan, in 2010, and is currently working toward the M. S. degree at Kobe University. His research interests involve atomistic simulation of nanowire transistors.

Mr. Takiguchi is a member of the Japan Society of Applied Physics.

Shunsuke Koba (M'10) was born in Hyogo, Japan, on December 21, 1987. He received the B. S. and M. S. degrees all in electrical and electronic engineering from Kobe University, Kobe, Japan, in 2010 and 2011, respectively, and is currently working toward the Ph. D. degree at Kobe University. His research interests involve quantum transport simulation and atomistic modeling of nanotransistors.

Mr. Koba is a member of the Japan Society of Applied Physics.

Hideaki Tsuchiya (M'93–SM'01) received the B. S., M. S., and Ph. D. degrees all in electronic engineering from Kobe University, Kobe, Japan, in 1987, 1989, and 1993, respectively.

In 1993, he was with the Department of Electrical and Electronic Engineering, Kobe University, as a Research Associate. He has been engaged in research of quantum transport simulation of mesoscopic devices. From 1999 to 2000, he was a Visiting Scientist with the University of Illinois at Urbana-Champaign, IL, USA. Since 2003, he has been an Associate Professor with the Graduate School of Engineering, Kobe University. His current research includes the quantum transport modeling of nanoscale MOSFETs and the first principles simulation of atomic-scale devices.

Dr. Tsuchiya is a member of the Institute of Electronics, Information and Communication Engineers of Japan, and the Japan Society of Applied Physics. He received a Young Scientist Award in 1998 from the Japan Society of Applied Physics and an Outstanding Achievement Award for a pioneering research on nanoscale device simulator in 2006 from the Institute of Electronics, Information and Communication Engineers of Japan.

Matsuto Ogawa (M'85–SM'09) received the B.E. in electrical engineering from the University of Tokyo, Tokyo, Japan, in 1980, and the M.S. and Ph.D degrees in electronic engineering from the University of Tokyo, Tokyo, Japan, 1n 1982, and 1985, respectively.

In that year he became a research associate in the Department of Electronic Engineering, Kobe University, Kobe, Japan, where he is presently a Full Professor. He has been engaged in research of lightwave electronics and nano-scaled devices. His current research includes quantum transport modeling in nanostructures. From 1992 to the end of 1993, he was on leave at IBM T.J. Watson Research Center, NY, as a Visiting Scientist.

Dr. Ogawa is a member of the Japan Society of Applied Physics and the Institute of Electronics, Information and Communication Engineers (IEICE) of Japan. He received Electronics Society Award in 2006 from the IEICE and Project Research Award from the Semiconductor Technology Academic Research Center (STARC) in 2008.