Compensation of CMOS Op-amps using Split-Length Transistors

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***Abstract*—Theoretical and experimental results are presented for op-amp compensation using split-length transistors. By using split-length devices the right-half plane zero which plagues op-amp performance can be eliminated. Experimental results indicate substantial enhancements in speed while reducing power consumption and layout area. Further, these techniques can be used to compensate op-amps when using small supply voltage (V_{DD}).**

I. Introduction

Two-stage op-amps have been the dominant amplifier topologies used in analog system design due to their simple frequency compensation and relaxed stability criterions. The two-stage op-amps have traditionally been compensated using the Miller (or Direct) compensation technique [1][2]. This method achieves dominant pole compensation by pole splitting due to Miller capacitance multiplication effect. However, the compensation capacitance (C_c) connected between the outputs of the first and second gain stages, leads to a right-half plane (RHP) zero. The RHP zero, located at $z_1=g_{m2}/C_C$ in the s-plane, decreases the phase margin of the op-amp and requires a larger capacitance to compensate the op-amp. This in turn results in a lower unity gain frequency of the op-amp given by $f_{un}=g_{m1}/2\pi C_c$ [1].

The RHP zero appears in the Miller compensated op-amps due to the feed-forward component of the compensation current flowing through C_C from the output of the first gain stage to the output of the second gain stage. Thus, the RHP zero can be eliminated by blocking the feed-forward compensation current, while allowing the feedback component of the compensation current to attain pole splitting. This can be achieved by several methods including a zero nulling resistor (R_Z) or a voltage buffer in series with the compensation capacitor in the feedback path [1][4].

A common-gate stage can also be employed to block the feed-forward component of the compensation current while achieving op-amp compensation [3]. If a cascoded differential amplifier (diff-amp) is employed in the first gain stage for higher gain, then the common-gate stage "embedded" in the cascode stack can be used for compensation [4]. This paper presents a brief review of the indirect feedback compensation and details the use of split-length devices for indirect compensation.

The op-amps presented in this paper have been fabricated with AMI's C5n (0.5µm) process and are designed to drive a 30pF off-chip load offered by the test setup.

II. Indirect Feedback Compensation

The class of compensation in which the compensation current is fed back indirectly from the output to the internal high impedance node is defined as *Indirect Feedback Frequency Compensation* or simply, indirect compensation [1], [5]. Here, the compensation capacitor is connected to an internal low impedance node in the first gain stage, which allows indirect feedback of the compensation current from the output node to the internal high-impedance node i.e. the output of the first stage. Figure 1 shows an indirect compensated op-amp using a common-gate stage [3]. Here, the compensation capacitor is connected between the output node-2 and an internal low impedance node-A. The feedback compensation current, i_c, is indirectly fed back to internal high impedance node-1 through the common gate device M_{CG}.

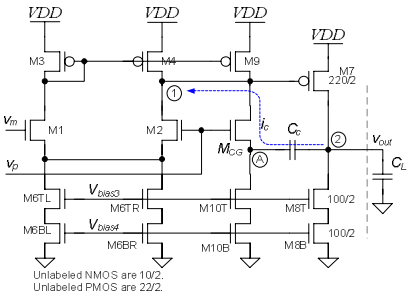


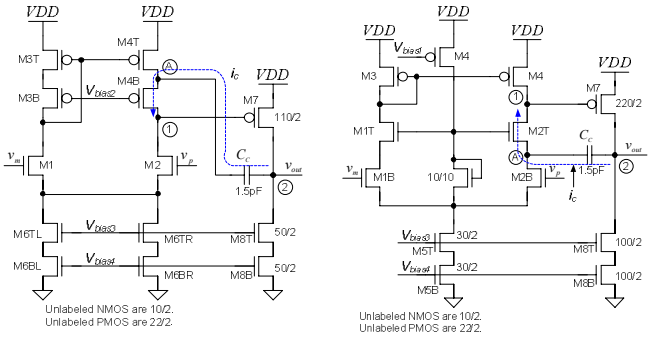
Figure 1. An indirect compensated two-stage op-amp with a common gate stage [1][3].

The dominant pole location for the indirect compensated op-amp is same as for the Miller compensation case. However, instead of a RHP zero we now have a LHP zero

located at $z_1=g_{mc}/(C_C+C_A)$, where g_{mc} is the transconductance of the common-gate device and C_A is the capacitance attached to the low-impedance node A. The non-dominant pole location is given as $p_2=-g_{m2}C_C/(C_1C_L)$. Also there exists a third parasitic pole arising due to the low impedance node-A [4].

We can observe that when using indirect compensation, the second pole, p_2, is moved further away from the dominant pole by a factor of approximately C_C/C_1. Hence, pole splitting can be achieved with a lower value of the compensation capacitor C_C and/or with a lower value of g_{m2}. This results in a significantly larger unity-gain frequency attainable by the op-amp. Also the LHP zero adds to the phase in the vicinity of the unity gain frequency, f_{un}, and significantly improves the phase margin [1][2].

Figure 2 shows the two-stage op-amp topologies where indirect compensation is achieved by using the "embedded' common-gate device in the cascode structure [4].



(a) Cascoded current mirror load

(b) Cascoded Diff-pair

Figure 2. Indirect compensated two-stage op-amps using cascode common gate device. The compensation capacitor, C_c, in each of the op-amps is connected to the the low impedance node A [1][4].

III. Indirect Compensation using Split-Length Transistors

High-speed, indirect-compensated, two-stage op-amps can be designed by employing the internal low impedance nodes in a cascode topology to feedback the compensation current [1]. However, as the supply voltage (V_{DD}) level has been scaling down continually and full scale cascoding may no longer be feasible in the nano-CMOS fabrication processes [6]. A suitable technique for low V_{DD} design which employs a split-length transistor for indirect compensation, proposed in [1]&[5], is analyzed in this section.

Figure 3 illustrates splitting of an n-channel MOSFET (NMOS) or a p-channel MOSFET (PMOS) to create a low impedance node-A. For an NMOS, it can be shown that the lower device, M1B, will either be in cut-off or triode region but never in saturation. Since a triode device offers a low channel resistance and also that node-A is connected to the source of the top device M1T, the node-A is a low impedance node. Similarly for the PMOS case, the top device M1T is either in cut-off or triode region causing the node-A to be a low impedance node [1].

The low impedance node-A can be used to feedback the compensation current to the output of the first stage i.e. node-1 in the op-amp in figures 1&2. Furthermore, indirect compensation can be achieved by splitting the lengths of either the current mirror load device or the diff-pair device.

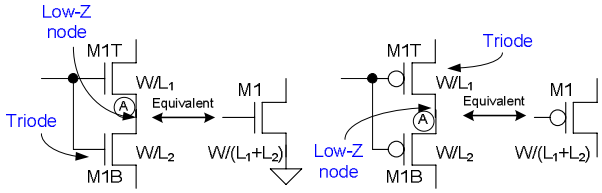


Figure 3. Illustration of the split-length NMOS and PMOS devices and the low-impedance nodes amenable for indirect compensation [1].

A. Split length current mirror load

Figure 4 exhibits a two-stage op-amp with a split-length current mirror load (SLCL) topology. The compensation capacitor is connected to the internal low impedance node-A to achieve indirect compensation.

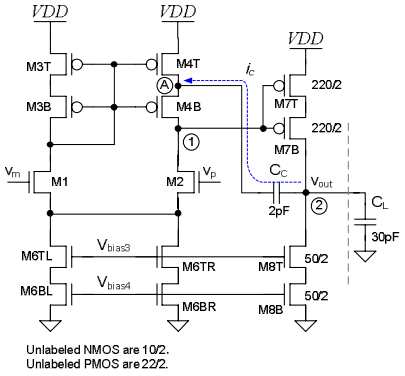


Figure 4. A two-stage op-amp with indirect feedback compensation using split-length load devices [1][5].

In order to simplify the small signal analysis of this op-amp topology, few assumptions have been made. Figure 5 illustrates the deduction of a small signal analytical model for the op-amp.

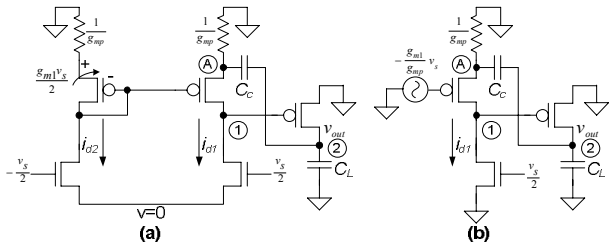


Figure 5. Small signal equivalent circuit for the op-amp with split-length current mirror load. The diffamp in (a) is simplified to derive the equivalent circuit (b).

The transconductance of each of the split PMOS devices is denoted as g_{mp}. The resistances and capacitances attached to nodes 1 and A, have been lumped together and connected between the respective nodes and ground. The resistance, R_A,

can be approximated to be equal to the channel resistance of the trioded PMOS, which is close to $1/g_{mp}$. Also, here if the current mirror load is designed with the same g_m as the diff-pair, we have $g_{mp} = \sqrt{2}g_{m1}$.

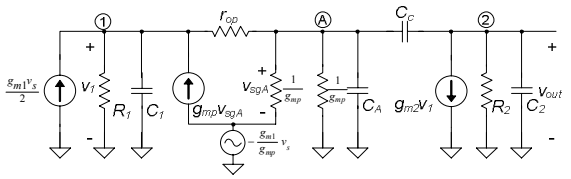


Figure 6. Small signal model for analysis of the two-stage op-amp employing split length load devices.

On applying nodal analysis on the small signal model shown in figure 6, we obtain a dc gain of $-g_{m1}R_1g_{m2}R_2$ and a unity gain frequency equal to

$$f_{un} = \frac{g_{m1}}{2\pi(2C_C)} \tag{1}$$

The LHP zero is located at

$$z_1 \approx -\frac{4g_{mp}}{3(C_C + C_A)} = -\frac{4\sqrt{2}g_{m1}}{3(C_C + C_A)} \approx \frac{8\sqrt{2}}{3}\omega_{un} \tag{2}$$

The dominant pole is given as

$$p_1 \approx -\frac{1}{2g_{m2}R_2R_1C_C} \tag{3}$$

Now, if $g_{mp} >> \frac{g_{m2}C_C(C_L||C_C + C_A)}{C_1(C_2 + C_C)}$, the non-dominant poles are given by

$$p_2 \approx -\frac{g_{m2}C_C}{2C_1C_L} \tag{4}$$

$$p_3 \approx -\left[2g_{mp}/C_2||C_C + 1/\left(R_1||r_{op}\right)C_1\right] \tag{5}$$

And for the case when $g_{mp} \le \frac{g_{m2}C_C(C_L||C_C + C_A)}{C_1(C_2 + C_C)}$ the conjugate complex non-dominant poles location is given as

$$|\mathrm{Re}(p_{2,3})| = \frac{g_{m2}}{C_L}\sqrt{\frac{g_{mp}C_L}{g_{m2}C_1}} \tag{6}$$

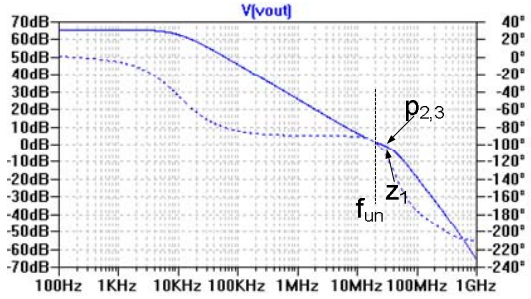


Figure 7. Simulated frequency response of the indirect compensated opamp with split-length current mirror load (SLCL). Here f_{un}=20MHz and PM=80°.

The SPICE simulated frequency response for this op-amp is displayed in figure 7. This op-amp exhibits a unity gain frequency of 20MHz, a phase margin of 75° and a transient settling of 60ns.

B. Split length differential pair

Figure 8 shows the proposed two-stage op-amp topology where a split-length diff-pair (SLDP) is used for indirect compensation. This topology exhibits better power supply rejection ratio (PSRR) since the node used for compensation (node A) is isolated from the supply rails.

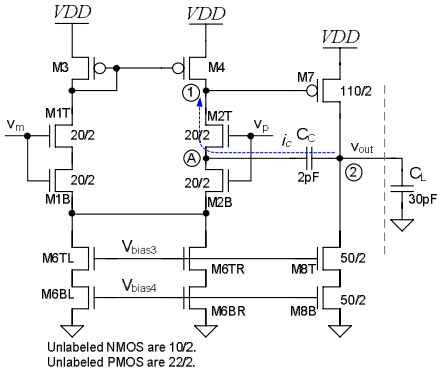


Figure 8. An indirect compensated two-stage op-amp employing split-length diff-pair.

Again, this topology is analyzed using the simplified equivalent circuit shown in figure 9. Here $g_{mn} = \sqrt{2}g_{m1}$ is the transconductance of the split-length NMOS in the diff-pair.

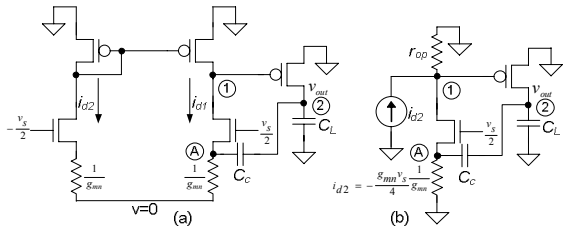


Figure 9. Small signal equivalent circuit for the op-amp with split-length diff-pair. The diffamp in (a) is simplified to derive the equivalent circuit (b).

Nodal analysis of this topology again yields the same non-dominant poles and zero locations as in the split-length current mirror load case. However, the unity gain frequency is now estimated by

$$f_{un} = \frac{2g_{m1}}{2\pi C_C} \tag{7}$$

Thus the LHP zero can now be expressed as

$$z_1 \approx -\frac{4g_{mn}}{3(C_C + C_A)} = -\frac{4\sqrt{2}g_{m1}}{3(C_C + C_A)} \approx \frac{2\sqrt{2}}{3}\omega_{un} \tag{8}$$

which implies that the LHP zero arrives slightly earlier than the unity gain frequency. This has the effect of flattening the gain magnitude response which may degrade the phase margin of the op-amp. The SPICE simulated frequency response for

this op-amp is shown in figure 10. This op-amp exhibits a unity gain frequency of 35MHz, a phase margin of 62° and a transient settling of 75ns.

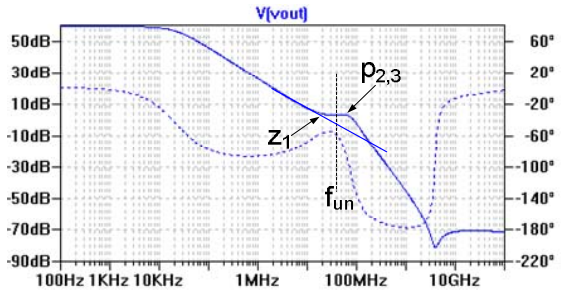


Figure 10. Simulated frequency response of the indirect compensated opamp with split-length diff-pair (SLDP). Here f_{un}=35MHz and PM=60°.

In the case of SLCL indirect compensation, we have the flexibility of varying g_{mp} independent of g_{m1} in order to control the location of the LHP zero and hence the phase margin of the op-amp. However, in the case of SLDP we do not have such convenience and it might be hard to obtain desirable phase margins with the SLDP topology. But the SLDP indirect compensation topology is of great utility when designing multi-stage indirect compensated op-amps [6].

IV. Chip Test Results and Performance Comparison

The test chip, designed using AMI's C5N (0.5µm) process, includes Miller compensated op-amps with and without the zero nulling resistor and the SLCL & SLDP indirect compensated op-amp topologies (see figure 11).

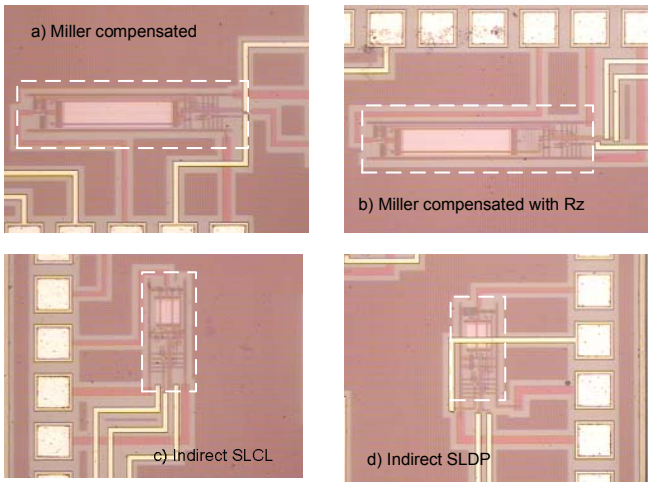
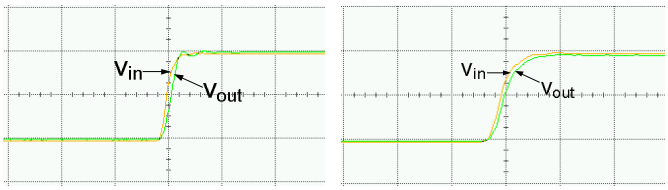


Figure 11. Micrographs of the two-stage op-amps fabricated on the test chip.

The step input test results for the indirect compensated op-amps in unity gain configuration is shown in figure 12. A performance comparison of the op-amp topologies fabricated on the test chip is presented in table 1.



(a) ISLCL, ts=60ns (b) Indirect SLDP, ts=75ns

Figure 12. Scope capture of the large input step response for the indirect compensated op-amps in follower configuration.

TABLE I. Performance Comparison of the Opamps for C_L=30pF.

Op-amp Topology	A_{DC} (dB)	f_{un} (MHz)	C_C (pF)	PM	t_s (ns)	Power (mW)	Layout area (mm^2)
Miller	57	2.5	10	74°	270	1.2	0.031
Miller with R_Z	57	2.7	10	85°	250	1.2	0.034
SLCL (this work)	66	20	2	80°	60	0.7	0.015
SLDP (this work)	60	35	2	60°	75	0.7	0.015

V. Conclusion

Indirect feedback compensation technique for two-stage op-amps using split-length transistors has been presented. The chip test results demonstrate that the indirect feedback compensation employing split-length devices leads significantly faster, more compact and lower power op-amps when compared to the traditional Miller compensation. The split-length indirect compensated topologies are suitable for op-amp design in low-voltage CMOS processes.

Acknowledgment

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