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Esmaeil Najafi Aghdam, Philippe Benabes, Javad Abbasszadeh

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Published on: 02 Oct 2009 - European Conference on Circuit Theory and Design

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Esmaeil Najafi Aghdam* ,   **Philippe Benabes **,**   **Javad Abbasszadeh***

* Sahand University of Tech., Faculty of Electrical Eng.
Sahand City, P. Code: 53317 11 111, Tabriz, Iran,
najafiaghdam@sut.ac.ir

** Dept. of Signal Processing and Electronic Systems,
SUPELEC, P. de Moulon, Gif sur Yvette, 91192, Franc.
Philippe.Benabes@supelec.fr

Abstract— In order to reduce mismatch error of a DAC used in a multibit delta-sigma some dynamic element matching (DEM) algorithms have been proposed before, from which Data-Weighted-Averaging (DWA) method is more hardware efficient and widely used. Unfortunately, DWA technique loses its functionalities for periodic signals which cannot be practically avoided. Many improvements have been suggested to minimize in band tone generated by DWA algorithm, but they cause limited performance compared with an ideal first order DEM. This paper presents a new modified DWA structure, which results in a completely first order mismatch noise shaping while solving in band tone problem. Simulations are presented for a 3rd-order lowpass delta sigma. However, its modified version can also be used in bandpass applications.

Keywords: *Data weighted averaging, DWA, DEM, ADC, DAC*

I. INTRODUCTION

Single bit delta-sigma modulators lead to very good linearity characteristics due to the 1-bit DAC inherent linearity. Today, however, telecommunications applications require large bandwidth thus leading to high oversampling ratios for single-bit topologies. Reducing this ratio can be compensated by using a multibit quantizer so that theoretically, the signal-to-noise-ratio (SNR) increases by 6dB per bit. Furthermore, multibit quantization enhances system stability by making possible the use of higher open-loop filter gain. It is also important to note that using multibit structure is one of the best ways to decrease jitter sensitivity and amplifiers constraints especially in the continuous time delta sigma modulators [1, 2].

Unfortunately, a DAC with very good linearity characteristics is required in multibit DSM. This leads to accurate component matching that is not generally compatible with CMOS standard technology.

Some algorithms were proposed to correct non-linearity errors in the internal DAC such as digital correction and dynamic element matching [3-7]. Randomization barrel shuffler can spread mismatch errors over the whole frequency range [1]. For high resolution application the circuit errors must be shaped and moved out of the band of interest. The mostly used first order DACs error shaping algorithm is Data Weighted Averaging in the feedback path of a Delta-Sigma modulator as shown in Fig.1. Such a selection scheme results in a first order mismatch shaping as will be denoted in the next section.

However, the DWA error reduction technique suffers more from periodic tones appeared in its band of interest which is usually accrued for some input levels.
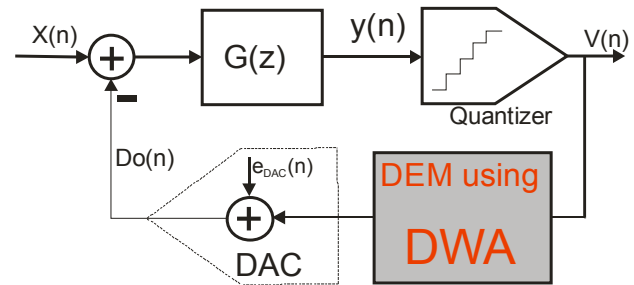

Figure 1. Multibit Delta-Sigma modulator using a DAW algorithm

Many modifications have been developed to solve tonal behavior of the DWA [8-11]. Most of them scarify DWA full performance to avoid affecting desired band from those tones [8, 11]. In other words, recently proposed modifications cause the DWA results error shaping behavior lower than its ideally first order function.

In this work, a new modification will be proposed which cause no functionality restriction, so the DWA algorithm can still acts as an ideal first order noise shaping system. The proposed algorithm uses a simple first order digital divider box and then a partitioned DWA structure.

In section II, the concepts of a conventional DWA is reviewed, in section III the tonal behavior of DWA scheme is presented, then, the modification proposed before will be addressed. The proposed new method is described in section IV, followed by simulation results. Some conclusions are finally mentioned in section V.

II. CONVENTIONAL DWA ALGORITHM

As mentioned above, the DWA is a technique to remove DAC cells mismatch errors out of the band of interest [3,4]. In essence, DWA tries to choose different DAC cells for consecutive codes. In this way, less common units participate in consecutive codes and DAC error signal shows fast changes in time domain which is an indication of high-frequency content in frequency domain [11].

Although, a conventional DWA block, shown in Fig.1, doesn't have any filter structure [10], use a suitable element selection strategy which can cause mismatched nonlinear errors to be filtered like an ideal first order high pass filter. The element selection strategy is depicted in table one for some consecutive input levels, where DAC uses a 3-bit thermometric structure.

As indicated on the table, DAC cells (example: D_1, D_2... D_8) must be selected circularly based its consecutive input value, v(n). From one period to another, the status of selected cells is simply memorized by a pointer called ***Ptr(n)*** described at end

column on the table. Mathematically, it was proven that the nonlinear part of DAC mismatch error on its output can be estimated as follow [3,11]:

$$DAC_{error} = (1 - z^{-1}) IM(Ptr(z))$$

$Where$:

$$IM(ptr) = \sum_{n=0}^{n=Ptr-1} (V(n) - V_{mean}) / V_{mean} \qquad (1)$$

$$V_{mean} = \frac{1}{N} \sum_{n=0}^{N-1} v(n)$$

Nonlinearity errors for a DAC derived by DWA element selection scheme can then be analytically calculated using (1). Such an error shaping is similar to main delta-sigma modulators, where an M-cell DAC presents a non linear error term on its output which can be formulated as follow [10,11]:

$$DAC_{error} = \frac{\pi^2}{3\ OSR^3} \cdot \frac{\sigma_{\alpha}^2 (1 - \frac{1}{M})^2 M}{12} \qquad (2)$$

Where σ_{α}^2 is variance of DAC cells mismatch error, for example $(0.01)^2$, means one percent mismatch.
Typical implementation circuit for the conventional DWA is shown in Fig.2 [11].

Table 1. Lowpass DWA selection scheme

DAC Cells (3-bit thermometric structure)

v(n)	D₁	D₂	D₃	D₄	D₅	D₆	D₇	D₈	Ptr(n)
2	■	■							3
5			■	■	■	■	■		8
4	■	■	■					■	4
7	■	■	■		■	■	■	■	3
5			■	■	■	■	■		8
2	■							■	2
3		■	■		■				5
4					■	■	■	■	1

(left axis label) DAC input value

III. TONAL BEHAVIOUR OF DWA

The conventional DWA is able to shape DAC mismatch errors as a first order high pass filter, but for some periodic inputs and some input DC-levels.
The tonal behavior of a conventional DWA scheme can also be described by system level simulation as Fig.3[10,11].
Where, the undesired tones comeback to the band of interest while the input level goes some smaller levels, which has not been already predicted by (1).
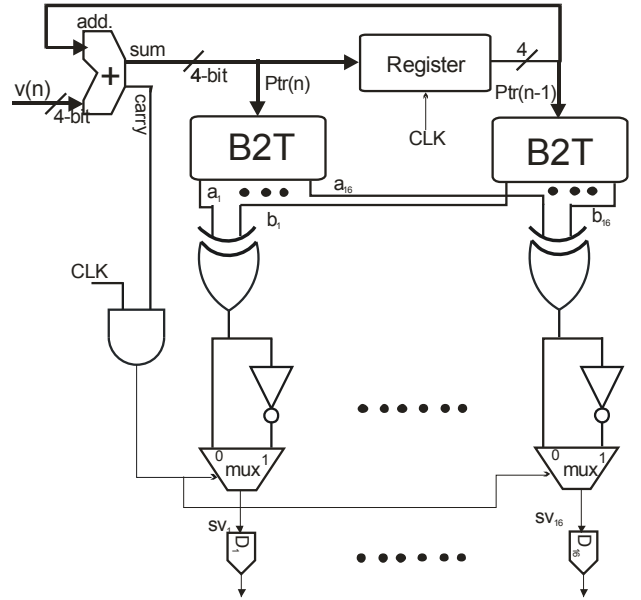

Figure 2. a suitable circuit block diagram to implement a 4-bit DWA

More simulation examples which are monitoring tonal behavior of a conventional DWA algorithm are presented in [10-11]. The tones frequency can be estimated as below [9-11]:

$$f_{tons} = k \frac{GCD}{M} f_s , \qquad k = 1,2,... \quad (3)$$

Term *GCD* means the greatest common devisor and M is the number of DAC cells.
Practically in order to avoid these tones, the over sampling ratio *(OSR)* of the delta-sigma modulator must satisfy certain condition as denoted below for the same *k*, which is not suitable in general case specially for wide-band applications.

$$OSR \geq (\frac{k+1}{2})M , \qquad k = 1,2,.... \qquad (4)$$

IV. PREVENTION OF TONAL BEHAVIOUR OF DWA

Based our researches, there are at least 9 different methods which have been already proposed to reduce in band tones resulting from DWA algorithm application. They are only summarized on table-II; one can refer to the related references. Between proposed tones prevention methods, the partitioned technique (PDWA) is more attractive because of its relatively better performance, simplicity and generality for lowpass and bandpass applications [8,9,12,12]. Fig.4 shows PDWA architecture, where DAC input code is divided into two parts using a simple divider and adding rest of division on only one definitive part of the results.
By this means, the difference of mean value between two sub DACs (upper M/2 cells and lower one) cannot be shaped by two separated DWA algorithms. So, theoretically, its performance will be decreased even for non periodic inputs. Furthermore, its tonal behavior may occur because of limited perturbation in its global algorithm but with smaller probability compared with conventional DWA implementation.
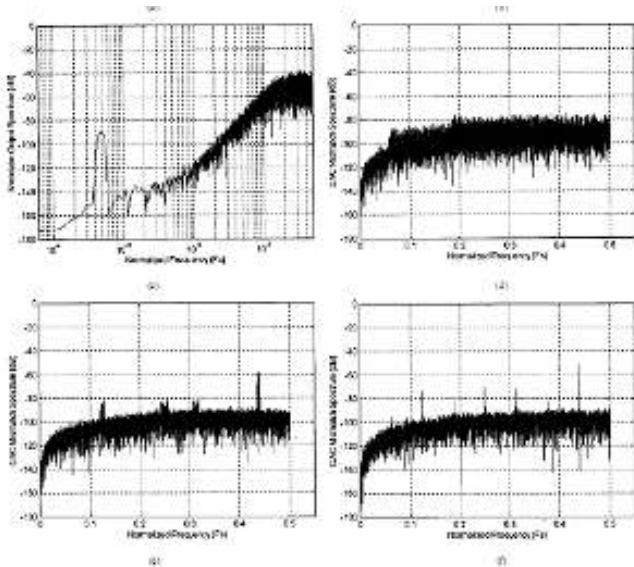
Figure 3. Output spectrum(log-scale versa normalized frequency) for different input levels where DAC mismatch errors made inband tones be appeared [10]

Table 1) Technique to prevent tonal behavior of DWA

	Tone-prevention technique for DWA	Characteristic and Inconvenience
1	dither[10]	The simplest, less performance
2	rotation, RDWA[9]	First idea, limited performance, need to be optimized
3	RnDWA [10]	Randomization based, limited performance, difficult to be implemented
4	DIA [9-10]	double index, Compatible with SC, no general
5	IDWA [10-11]	Incremented cells, limited performance, need to further DAC cells
6	bidirectionnelle BI-DWA [11]	Two pointer, limited performance, need to further DAC cells
7	PDWA[9,12]	Segmentation, limited performance, the best
8	DWApartielle [7,11]	Applied incompletely, Limited performance
9	pseudo –DWA [10]	Applied incompletely, Limited performance,

Equation below, analytically estimate the remained unshaped DAC error which correspond mainly the LSB of input code and difference between the mean value of upper half DAC and lower half one, in case of a simple partitioned DWA.

$$\Delta error_{PDWA}(n) = \frac{LSB_{v(n)}}{2}[\frac{2}{M}\sum_{1}^{M/2}\alpha_i - \frac{2}{M}\sum_{1+M/2}^{M}\alpha_i \ ] \quad (5)$$

This theoretical prediction of extra error terms in PDWA is verified by simulation as shown in Fig.5.

As seen on this spectrum, the DEM performance is decreased by increasing inband noise level, but its tones are moved far from the band of interest.
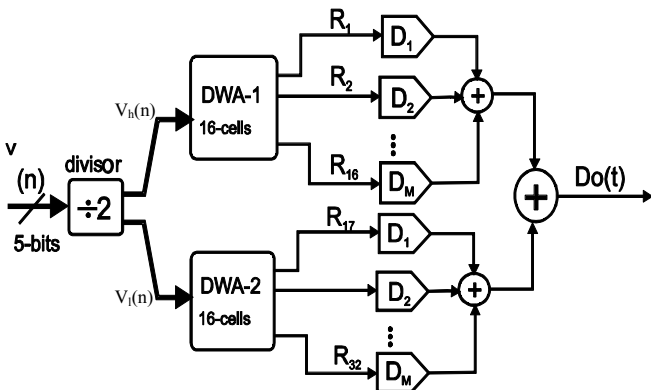

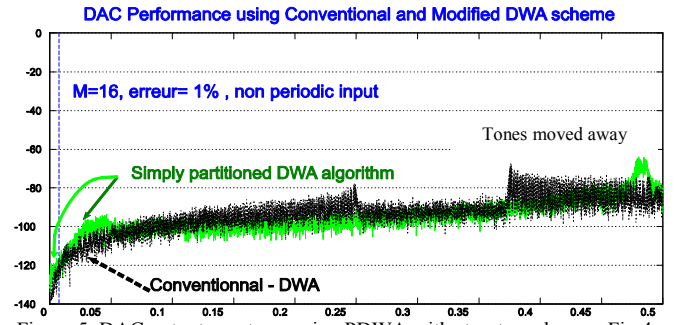Figure 4. Conventional PDWA block diagram(5-bit DAC)

Figure 5. DAC output spectrum using PDWA with structure shown Fig.4

V. PROPOSED METHOD TO PREVENT TONAL BEHAVIOUR OF DWA ALGORITHM

As mentioned above, in order to implement a multibit delta-sigma modulators using a DWA mismatch noise shaping technique, the partitioned DWA algorithm is the one of the best choice to prevent its tonal behavior[8-11]. However, its performance is limited mainly by divider function which has no more mismatch shaping action in its previously proposed structure [11-13]. In this work, a new filter based divider is proposed which causes divider to shape division rest. In fact, such an algorithm must select a suitable sequence as the difference between two outputs codes in a manner that there is no any power remained in the band of interest while respecting to the number conservation rule.

Fig.6 shows a desired first order filter based divider structure for lowpass applications. It has a switching block (SB) including a first order highpass digital filter in a delta-sigma like feedback architecture which can form its output R(n).
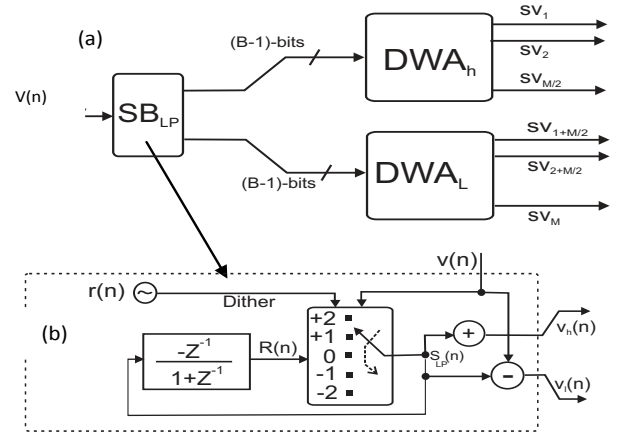

Figure 6. a)Modified PDWA block diagram, b) proposed lowpass

Where, *v(n)* is the input code, *vₕ(n)* and *vₗ(n)* are output of divider. *R(n)* is the filter output indicates that the rest of division must be added in what part of DWA. The case *R(n)>0* corresponds to the upper selection and vice versa. *r(n)* is a 1bit random number used when *R(n)* has no definitive indication, e.g. in its zero case. The switching sequence signal named *S(n),* is calculated at each period depending on filter output, DAC input code and randomly generated *1-bit r(n)*. Its transfer function is in general proposed as below, but may be simplified further with elimination of the cases S(n) =±2.

$$S(n) = \begin{cases} +1 & v(n) \ is\ odd & R(n) \succ 0 \\ r(n) & v(n) \ is\ odd & R(n) = 0 \\ -1 & v(n) \ is\ odd & R(n) \prec 0 \\ +2 & 2 \leq v(n) \leq (M-2)\ and\ even & R(n) \succ 0 \\ -2 & 2 \leq v(n) \leq (M-2)\ and\ even & R(n) \prec 0 \\ 0 & all\ other & cases \end{cases} \quad (6)$$

By this means, two half DAC inputs can be calculated as:

$$v_h(n) = \frac{v(n) + S(n)}{2} \quad v_l(n) = \frac{v(n) - S(n)}{2} \qquad (7)$$

Since, the switching sequence S(n) has a first order highpass transfer function depending on filter output R(n), the LSB (or two LSBs) is shaped by the same manner, which results in a first order mismatch shaping on (5). Total DAC error using the proposed partitioned DWA algorithm can now be written as (8) for lowpass applications, where α_h and α_l are the mean value of mismatch error for upper half DAC and lower one respectively. It can be derived following (1) [9,11]. Two former terms are directly given by (1) and the third term can be considered as an extra gain error which is linear with the DAC input having less importance [1]. However, the fourth term is a nonlinear error depending on the difference between average gains of two half DACs and shape of S(n) sequence which is produced by a desired highpass filter. Therefore, the only inconvenience rest in the proposed structure relayed on the forth term. This term can be compared with the whole of the right hand of (1), where it is clearly decreased by the shape of S(n) produced by the desired filter.

$$DAC\ error_{PDWA}(n) = \sum_{i=Ptr(n-1)}^{Ptr(n)-1} \alpha_i + \sum_{i=\frac{M}{2}+Ptr(n-1)}^{\frac{M}{2}+Ptr(n)-1} \alpha_i$$
$$- v(n)[\frac{\overline{\alpha_h} + \overline{\alpha_l}}{2}] - S(n)[\frac{\overline{\alpha_h} - \overline{\alpha_l}}{2}] \qquad (8)$$

As theoretically predicted by (8), the overall resolution of the proposed modification on PDWA is obtained nearly identical to the similar case of an ideal DWA block. The modified PDWA performance in terms of effective number of bit (ENOB) can be improved by 0.22-bit in best case or can be decreased as low as 0.5-bit in the worth case input sequences as described more in [11]. Based (1) and (8), we can derive the performance of the proposed algorithm as below: (9)

$$ENOB_{DWA} + Log_2[\frac{M-1}{M-2}] - 0.5 \le ENOB_{DWA}^{proposed} \le ENOB_{DWA} + Log_2[\frac{M-1}{M-2}]$$

Where $ENOB_{DWA}$ is related to the performance of a fully data weighted averaging algorithm without any tones. The difference between two sides of (9) comes from correlation between $v_h(n)$ and $v_l(n)$. The correlation term is about zero for lower input, i.e. there is no quotient form division operation and it is high for medium or upper input level. In case of low level input, the correlation is low so the proposed algorithm appears even a little more efficient the simple DWA. Practically, the performance of the proposed algorithm is obtained about 0.2-bit lower than that of an ideal DWA without tones as verified by different simulations, there is no saturation on integrator output **R(n)** [11].

VI. SIMULATION RESULTS

The proposed modification on PDWA algorithm is used in a third order lowpass multibit DSM with a 4-bit quantizer. A zoomed view of its output spectrum is shown in Fig.7. It can be seen that the proposed technique has a better function suppressing the in band tones and moving them far from band of interest by the desired filter. This figure is simulated supposing a given 1 percent DAC cells error. The amount of improvement depends on stochastic properties of input signal.

VII. CONCLUSION

Some aspects of the conventional DWA algorithm using as a dynamic element matching strategy were studied. Its major disadvantage is tonal behavior for periodic input levels. There were nine modification proposed before but no one operates completely as a first order error shaping predicted by an ideal DWA. We have proposed another modification which leads to definitively better results giving nearly a complete first order mismatch error shaping function with a little extra circuit. The analytical analysis has been derived and verified by system level simulations. Simulations are presented for a third order lowpass delta sigma. However, its modified version can also be used in bandpass applications.

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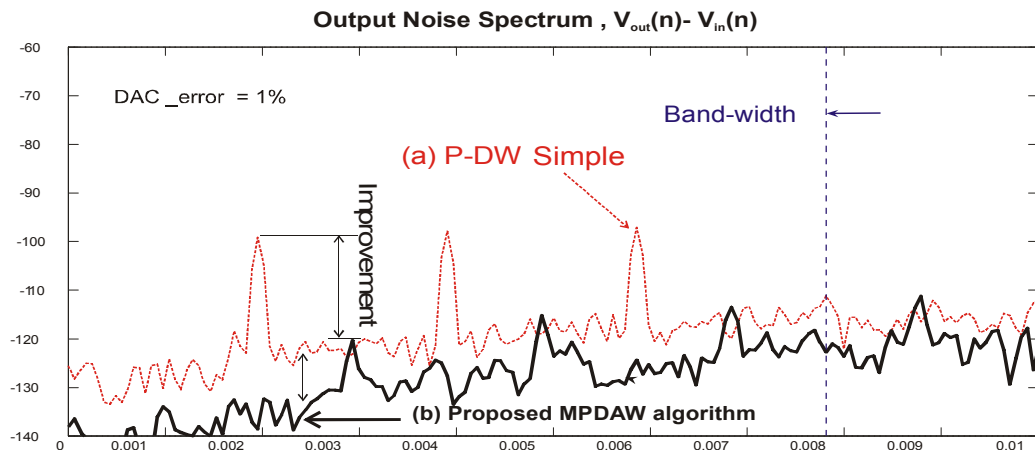
Figure 7. DAC output spectrum(zoomed), improving tones behavior and mismatch shaping function by a modified partitioned DWA proposed in this work