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Complex Power Distribution Network Investigation Using SPICE Based Extraction from First Principle Formulations

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I.   ABSTRACT

The modeling and the analysis of the power distribution networks (PDN) within multi-layer printed circuit board is crucial for the investigation of the performance of PCB systems. Carrying out such analyses in SPICE based tools has the advantage of being faster than the corresponding full-wave modeling and it allows obtaining both frequency and time domain results.

II.   INTRODUCTION

The modeling and analysis of the power distribution networks (PDN) within multi-layer printed circuit boards (PCB) are usually carried out in full-wave electromagnetic simulation tools or SPICE based tools. The charge delivery task performed by the PDN allows the correct functioning of all the active devices located on a PCB. Therefore, the correct modeling is crucial along with the necessity of carrying out the analyses in an efficient, i.e., not time-consuming way.

Full wave modeling approaches encompass all of the interactions necessary for modeling the PDN. However, the computational efficiency may be low for complex geometry. In fact, these PDN's are usually characterized by multi-scale features, i.e., features from a few mil associated with the via barrels and plane separation to the tens of cm scale associated with the board dimensions.

As proposed in [1], breaking down the PDN geometry into smaller parts to be investigated separately and then recombining these by means of the segmentation method [1,2,4] is a viable and efficient way of analyzing each of the constituent elements with the most appropriate method, provided the proper boundary conditions are enforced. In [1], the aforementioned approach is carried out in the frequency domain by combining the analyses performed on the two constituent elements of the complex PDN shown in Fig.1 and Fig.2. The first element is a pair of planes, whose center part, corresponding to a BGA footprint with vias and antipads, is removed. The second part is the very same removed geometry corresponding to a BGA packaged IC footprint. The first part is analyzed with the cavity model formulation, whereas the second is simulated using an FEM method. The equivalent impedance networks obtained with the different formulation and analyses are finally recombined through the segmentation method [2].

Although this approach is very helpful for the correct modeling and the analysis of the PDN of interest, the ultimate need of a design engineer is a SPICE deck, which can be cascaded with other circuit representations in order to analyze the behavior of the entire link path and PDN. This goal can be achieved by employing the aforementioned concept [1] to the two equivalent circuit representations associated with the constituent parts of the geometry described in Fig.1 and Fig.2. The first one is extracted by means of the cavity model approach, while the second is obtained by employing of IdEM [5] on the FEM simulation results of the cut out geometry.

The results of the SPICE simulations are compared along with the results of the Hybrid Method, i.e., Cavity Model plus FEM and the results of an FEM simulation of the entire PDN geometry.

II. GEOMETRIES INVESTIGATED

The geometry under investigation is obtained by extracting only the power delivery network associated with 1.5V and GND planes, as shown in Fig.1. The geometry consists of two solid planes, 10 cm by 8 cm, where many holes corresponding to a BGA package footprint are included. The hole patterns localized on the top and bottom planes correspond to the antipads of the BGA package pins connected to the 1.5 V plane, the GND plane or any other layer.
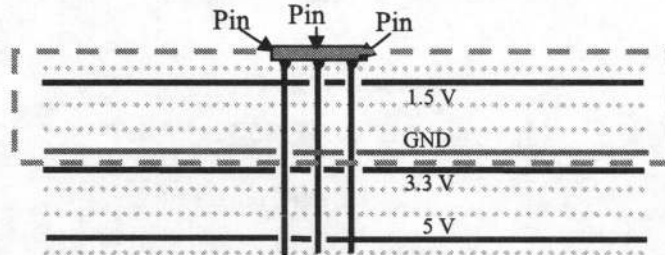

Fig.1. Board stack-up: the power distribution network considered is highlighted in the dashed box. The connections between the power layers and the IC are given just as an example.
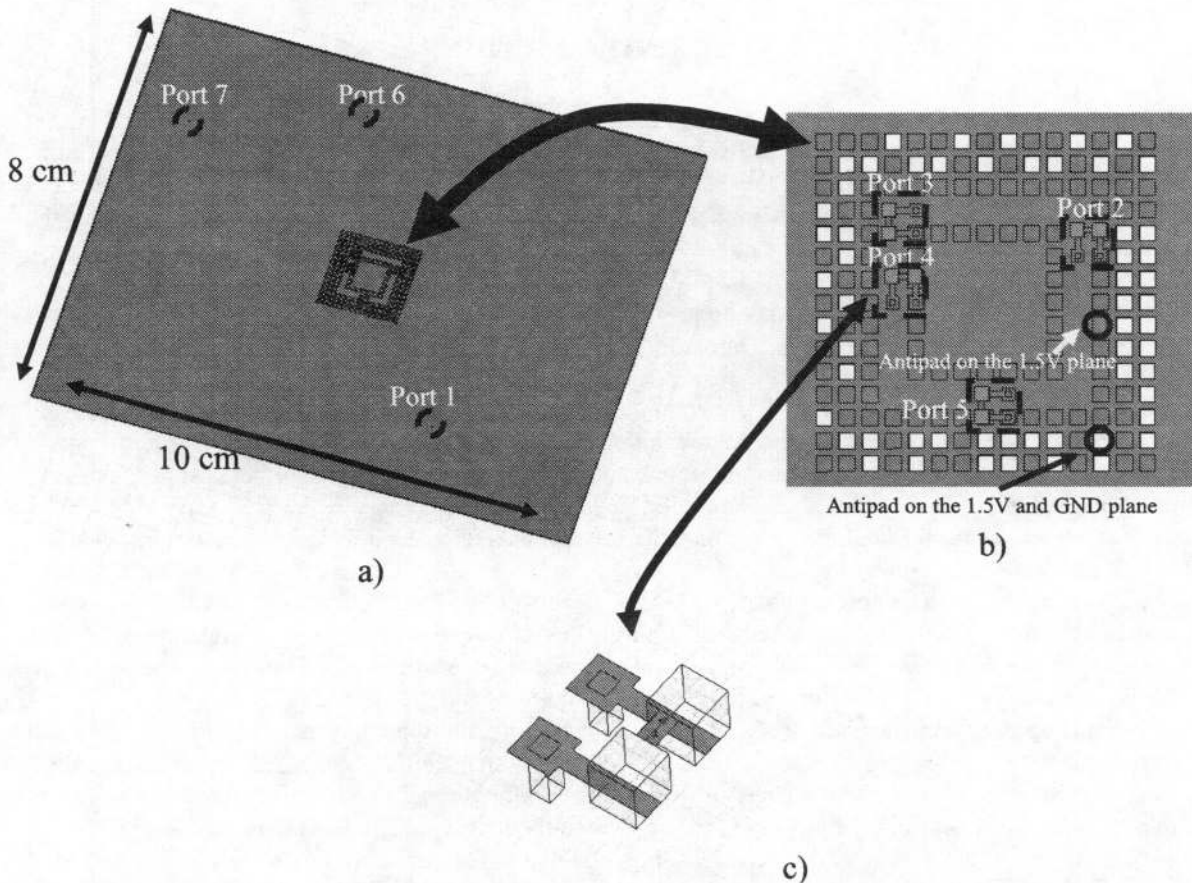

Fig.2. a) Top view of the of the power distribution network under investigation extracted from the stack-up of Fig.1. b) Close up of the hole pattern associated with the 1.5V plane of the PDN of interest. c) Close up of the interconnect associated with the ports located on the BGA footprint

Fig.2b shows the hole pattern on the top solid plane corresponding to the antipads associated with the pins of the BGA package connected to the bottom layer or any other of the layers. Seven excitation ports are employed in the geometry shown in Fig.2a. Four are located on the BGA footprint and three on the

reminder of the PDN. Each of the first four ports takes into account the entire interconnect from the bottom of the IC package down to the 1.5V or the GND plane and it consists of few elements, i.e., the balls - cubes in the current model - associated with the BGA package and the vias connecting the balls to the 1.5V or the GND planes. The spacing between the two planes is approximately 21 mils, the square balls have sides of 24 mils and the vias have sides of approximately 10 mils. Due to the complexity of the model, only the central 15 x 15 pins of an actual BGA package with all the pine assigned are represented in the 3D full wave model, as shown Fig.2b.

III. THE EQUIVALENT CIRCUIT MODELS AND THE RESULTS

The well-known cavity model formulation allows the extraction of equivalent circuit models associated with 2D geometries [2-4]. However, the complex nature of the PDN shown in Fig.2 requires the employment of several methods in order to extract an overall equivalent circuit model to be simulated in a SPICE-based tool. In particular, the PDN of interest is partitioned into five elements as shown in Fig.3. The equivalent circuit models of four of the five elements are extracted by means of the cavity model approach [2-3], while the equivalent circuit model associated with the center element is extracted by means of IdEM [5] (Identification of Electrical Macromodel, circuit extraction tool developed at the EMC Laboratory of the Politechnic University of Torino) employed on the FEM simulation results of the BGA footprint geometry. The five equivalent models are then recombined together into one SPICE deck. The recombination is made possible by employing several internal ports along the sides of each pair of touching patches according to the segmentation method [2-4]. These ports are located along the dashed lines shown in Fig.3 and they are spaced apart a tenth of the wavelength associated to the highest frequency of interest, i.e., 5 GHz. The comparison of the self and transfer impedances between several ports shown in Fig.2 are given in Fig.4. The comparison is carried out by between FEM simulation results of the geometry under investigation in Fig.2, the Hybrid Cavity Model Method result presented in [1], and a SPICE simulation associated with the same geometry.
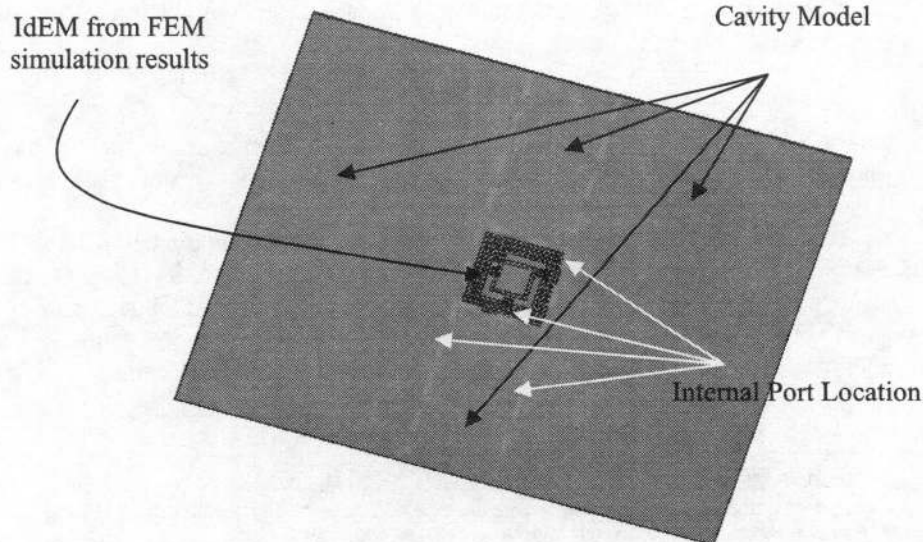

Fig.3. The PDN of interest is partitioned, an equivalent circuit model is extracted for each element and then all the elements are recombined
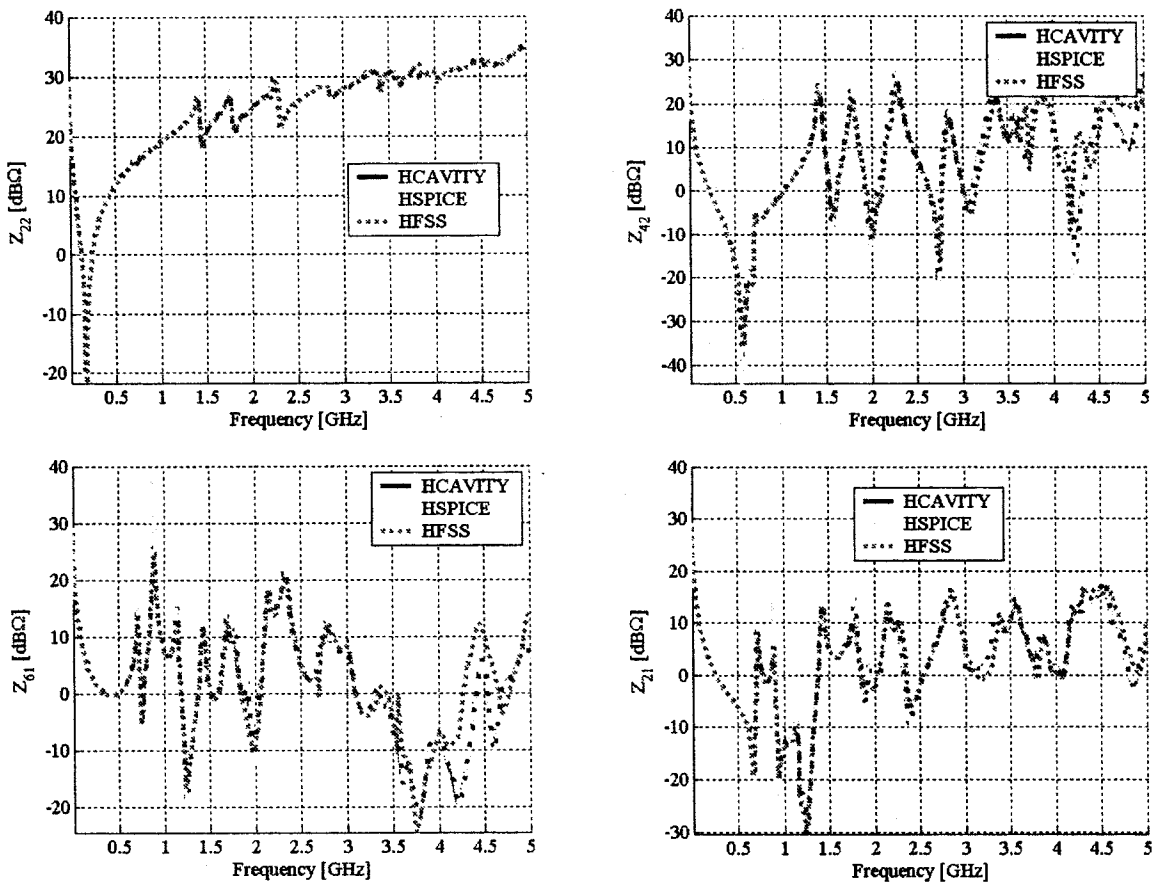
Fig.4. Self and transfer impedances comparison among different modeling approach of the same geometry of Fig.2. The Hybrid Cavity Model approach results and the SPICE simulation results overlap.

IV. CONCLUSIONS

The employment of different circuit extraction procedures and the segmentation method has been shown to give a good agreement up to several GHz, when the SPICE simulation results are compared with the results obtained by employing other methods.

In particular, a perfect match is obtained with the Hybrid Cavity Model approach, whereas no more than 10 dB difference is observed beyond 4GHz with respect to the FEM simulation results. On the other hand, a SPICE deck has the advantage of allowing time domain simulations of the PDN geometry of interest, it is faster than the corresponding full-simulation and it can be incorporated with other equivalent circuit model representations, allowing the possibility of investigating the entire full-link path within a SPICE based tool.

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