Panel: Complex System Verification: The Challenge Ahead

Chair: Ron Collett - Collett International, Inc., Santa Clara, CA
Organizers: Mike Gianfagna - Zycad Corp., Fremont, CA
                   Michel Courtoy - Quickturn Design Systems, Mountain View, CA

Time-to-market continues to be *The Challenge* faced by developers of complex electronic systems.   The bottleneck - which was traditionally in the design phase of the project - has now moved downstream to the system-level verification stage.   The growing adoption of top-down design methodologies based on HDL and synthesis has made the generation of large multi-million gate designs easier than before.   The efficient verification of those newly created gates in the final system is now the key to solving *The Challenge.*

Technologies such as rapid system prototyping, ASIC emulation and formal verification offer the potential to completely verify the full system.   Hardware and software co-design and HDL test benches offer the potential to feed real world inputs to the verification process.

This panel will assess the outlook for verification for complex systems.   We will focus on enabling technologies which show promise in this area, both now and for the future.   The panel will present a mixture of tutorial material, leading edge academic work, current technology and the user's perspective.   In addition to current and future technologies, each speaker will specifically address how design methodology is impacted by their choice of verification methodology.

The discussion of the panel will focus on:

- What's required from the EDA industry to make their customers successful in the future?

- System level verification can be quite expensive. Is the promised Return-On-Investment really   there?

- Which technologies are usable without turning design methodologies upside down?

- Just what is product and what is research in this area?

The target audience includes chip and system designers, design managers and executive management who are pondering the benefits and costs of implementing system-level verification.

The panelists represent a mix of academia, companies offering verification solutions and users of system-level verification products.   The panel will begin with a tutorial on Formal Verification.   All other panelists will be limited to a short position statement, allowing ample time for discussion.   Each panelist will provide their own perspective of system-level verification challenges.

Panel Members:

Martin Baynes - Zycad Corp., Fremont, CA
Johan Van Ginderdeuren - Philips ITCL, Leuven, Belgium
Ken McMillan - AT&T Bell Labs., Murray Hill, NJ
Stephen Ricca - Rockwell/CMC, Santa Barbara, CA
Alberto Sangiovanni-Vincentelli - Univ. of California, Berkeley, CA
Steve Sapiro - Intel Corp., Hillsboro, OR
Naeem Zafar - Quickturn Design Systems, Mountain View, CA