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Complexity and Power Reduction in Digital Delta-Sigma Modulators

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Cover figure is an illustration of the digital cascaded error-feedback modulator.

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To my parents and teachers

Abstract

A number of state-of-the-art low power consuming digital delta-sigma modulator ($\Delta\Sigma$) architectures for digital-to-analog converters (DAC) are presented in this thesis. In an oversampling $\Delta\Sigma$ DAC, the primary job of the modulator is to reduce the word length of the digital control signal to the DAC and spectrally shape the resulting quantization noise. Among the $\Delta\Sigma$ topologies, error-feedback modulators (EFM) are well suited for so called digital to digital modulation

In order to meet the demands, various modifications to the conventional EFM architectures have been proposed. It is observed that if the internal and external digital signals of the EFM are not properly scaled then not only the design itself but also the signal processing blocks placed after it, may be over designed. In order to avoid the possible wastage of resources, a number of scaling criteria are derived. In this regard, the total number of signal levels of the EFM output is expressed in terms of the input scale, the order of modulation and the type of the loop filter.

Further on, it is described that the architectural properties of a unit element-based DAC allow us to move some of the digital processing of the EFM to the analog domain with no additional hardware cost. In order to exploit the architectural properties, digital circuitry of an arbitrary-ordered EFM is split into two parts: one producing the modulated output and another producing the filtered quantization noise. The part producing the modulated output is removed after representing the EFM output with a set of encoded signals. For both the conventional and the proposed EFM architectures, the DAC structure remains unchanged. Thus, savings are obtained since the bits to be converted are not accumulated in the digital domain but instead fed directly to the DAC.

A strategy to reduce the hardware of conventional EFMs has been devised recently that uses multiple cascaded EFM units. We applied the similar approach but used several cascaded modified EFM units. The compatibility issues among the units (since the output of each proposed EFM is represented by the set of encoded signals) are resolved by a number of architectural modifications. The digital processing is distributed among each unit by splitting the primary input bus. It is shown that instead of cascading the EFM units, it is enough to cascade their loop filters only. This leads not only to area reduction but also to the reduction of power consumption and critical path.

All of the designs are subjected to rigorous analysis and are described mathe-

matically. The estimates of area and power consumption are obtained after synthesizing the designs in a 65 nm standard cell library provided by the foundry.

Populärvetenskaplig sammanfattning

I denna avhandling presenteras ett antal strukturer av digital delta-sigma-modulation som ligger i forskningens framkant inom energisnål digital-till-analog konvertering (DAC, eng. Digital to Analog Converter) av signaler. I en delta-sigma-modulator med översampling är modulatorns främsta uppgift att reducera den digitala ordbredden till DAC:en samt filtrera och omforma frekvensspektrumet av kvantiseringsbruset. Bland de olika delta-sigma strukturerna är felåterkopplingmodulatorer (EFM, eng. Error-Feedback Modulator) väl lämpade för såkallad digital-till-digital modulation.

För att möta kraven har här ett antal olika modifieringar av den konventionella EFM-strukturen föreslagits. Om interna och externa digitala signaler inte skalas korrekt, riskerar både modulatorn och efterföljande konstruktioner att bli överdimensionerade vilket resulterar i resursslöseri. För att undvika detta, har ett antal skalningskriterier tagits fram. Det totala antalet utgångsnivåer i EFM-strukturen bestäms av: antalet ingångsnivåer, graden av modulation och typvalet av filter för återkoppling.

Vidare beskrivs hur strukturella egenskaper hos en DAC med enhetselement tillåter oss att överföra en del av den digital bearbetning i EFM till den analoga domänen utan extra kostnad. För att utnyttja de strukturella egenskaperna hos en EFM av godtycklig ordning, är den indelad i två delar. Första delen producerar den modulerade datan och den andra delen producerar det filtrerade kvantiseringsbruset. Den första delen kan tas bort efter att EFM utsignalen har representerats med ett set av kodade signaler. Digital-till-analogiomvandlaren förblir oförändrad i den föreslagna EFM jämfört med konventionell EFM. Besparingar görs genom att bitarna som ska konverteras inte ackumuleras i den digitala domänen, utan skickas direkt till DAC:en.

En strategi för att reducera hårdvaran av en konventionell EFM har nyligen formats där multipla EFM-enheter kaskadkopplad. Vi applicerar ett liknande tillvägagångssätt, men använder istället flera modifierade kaskadkopplade EFM-enheter. Det problem med kompatibilitet som uppstår, pågrund av att utgångarna av den modifierade EFM-strukturen är kodade, löses enkelt genom ett antal aritmetiska operationer. Den digitala bearbetningen är distribuerad bland de olika EFM-enheterna och delas upp genom att den primära bussen av insignalen delas upp. Vi visar att istället för att kaskadkoppla hela EFM-enheter, är det tillräckligt att enbart kaskadkoppla deras filter för återkoppling. Detta leder inte bara till en reduktion av kiselarean utan även en reduktion av såväl effektförbrukningen som den kritiska vägen i kretsen.

Alla konstruktioner har analyserats rigoröst och beskrivits matematiskt. Upp-

skattningarna av kiselarea och effektförbrukning är gjorda efter syntes i ett 65-nm standardbibliotek tillhandahållet av tillverkaren.

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Peace and blessings of Allah be upon the Holy Prophet MUHAMMAD (peace be upon him), the last of the prophets of Allah, who exhort his followers to seek for knowledge from cradle to grave and whose in-comparable life is the glorious model (being the best follower of the Quran) for the humanity.

My motivation of research is also a direct manifestation from the Holy Quran, the user manual for the entire humanity where the Almighty Allah has invited the whole mankind at several places to think, ponder, investigate, research and reflect not only on their own creation but also the entire creation. For example,

And He has subjected to you, as from Him, all that is in the heavens and on earth: behold, in that are signs indeed for those who reflect. [Quran, chap 45: verse 13]

He Who created the seven heavens in layers. You will not find any discrepancy in the creation of the All-Merciful. Look again-do you see any gaps? Then look again and again. Your sight will return to you dazzled and exhausted! [Quran, chap 67: verse 3-4]

Behold! In the creation of the heavens and the earth; in the alternation of the night and the day; in the sailing of the ships through the ocean for the benefit of mankind; in the rain which Allah Sends down from the skies, and the life which He gives therewith to an earth that is dead; in the beasts of all kinds that He scatters through the earth; in the change of the winds, and the clouds which they trail like their slaves between the sky and the earth (Here) indeed are Signs for a people that are wise. [Quran, chap 2: verse 164]

I would like to express my gratitude towards:

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Nadeem Afzal
December 11, 2014,
Linköping Sweden

Preface

The research on complexity and power reduction in digital delta-sigma modulators has resulted in the following published material and manuscripts:

Paper A

A hardware-efficient arrangement of delta-sigma digital-to-analog converter ($\Delta\Sigma$-DAC), is propose. In the proposed design, the digital input is split into two parts: one is applied to a first order $\Delta\Sigma$ while the other is applied directly to the unit-element-based DAC. In this way, DAC gets a partially shaped digital signal. In the proposed arrangement, the performance is maintained while the hardware of the $\Delta\Sigma$ is reduced. Conclusions are based on theory and simulation results.

- **Nadeem Afzal** and J Jacob Wikner, "Power efficient arrangement of oversampling sigma-delta DAC," *NORCHIP*, Copenhagen, Nov. 2012.

Paper B

In Paper B, we propose how the hardware complexity of digital multi-bit error-feedback $\Delta\Sigma$ modulator (EFM) of arbitrary order can be reduced. This is achieved by splitting the combinatorial circuitry of the modulators into two parts: one producing the modulator output and another producing the filtered error signal. The part producing the modulated output is removed by utilizing a unit-element-based DAC.

To illustrate the reduced complexity and power consumption, we compare the synthesized results with those of conventional structures. Fourth-order modulators implemented with the proposed technique use up to 26% less area compared to conventional implementations. Due to the area reduction, the designs consume up to 33% less dynamic power. Furthermore, empirical results show that it can operate at a frequency 100 MHz higher than that of the conventional.

- **Nadeem Afzal**, J Jacob Wikner and Oscar Gustafsson, "Reducing complexity and power of digital multi-bit error-feedback delta-sigma modulators," *Circuits and Systems II: Express Briefs, IEEE Transactions on*, June 2014.

Paper C

In order to determine the maximum allowed input scale for stable operation of higher-order $\Delta\Sigma$ modulators, designers largely depend on the analytical and numerical analysis-es. In Paper C, the maximum allowed input scale to an EFM of arbitrary order is mathematically derived. The digital modulator with an arbitrary output word length is stable if its output does not overflow. Thus, to avoid overflow of the modulator output, the relations between the peak values of the involved digital signals, are devised. A number of example configurations are presented to illustrate the usefulness of the derivations.

- **Nadeem Afzal**, Oscar Gustafsson and J Jacob Wikner, "On scaling and output cardinality of digital multi-bit error-feedback modulators," manuscript to be submitted.

Paper D

The hardware of an arbitrary-order EFM has recently been reduced by using multiple cascaded EFMs. In Paper D, a modified cascading strategy is devised. Parts of the processing of consecutively placed EFM stages are merged such that a significant amount of circuitry is removed in each stage. In the proposed design, the modulated output is represented by a set of encoded signals to be used by the signal processing block placed after the EFM.

To illustrate the savings, a number of configurations of fourth-order EFM designs, composed of two- and three-cascaded stages, have been synthesized in a 65 nm CMOS process technology using conventional and the proposed implementation techniques. Savings of 52.7% and 47%, in terms of area and power consumption, respectively, at an oversampling ratio of 4 could be obtain. The trade-off between sampling frequency and hardware cost is also presented. The proposed designs operate at sampling frequency from 50 MHz to 600 MHz higher than those of the conventional.

- **Nadeem Afzal** and J Jacob Wikner, "Digital multi-bit cascaded error-feedback $\Delta\Sigma$ modulators with reduced hardware and power consumption," manuscript to be submitted.

The contributions are also made in the following publications but the contents are not included in the thesis

1. **Nadeem Afzal** and J Jacob Wikner, "Study of modified noise-shaper architectures for oversample sigma-delta DACs," in *NORCHIP*, Finland, Tampere, October, 2010.

2. **Nadeem Afzal**, M. Reza Sadeghifar, J Jacob Wikner, "A study on power consumption of modified noise-shaper architectures for sigma-delta DACs," in *Proc. European Conf. Circuit Theory Design (ECCTD)*, Sweden, Linköping, Aug., 2011.

3. M. Reza Sadeghifar, **Nadeem Afzal**, and J Jacob Wikner, "A digital-RF converter architecture for IQ modulator with discrete-time low resolution quadrature LO," in *Proc. IEEE Int. Conf. Electronics, Circuits and Syst. (ICECS)*, Abu Dhabi, UAE, Dec., 2013.

4. **Nadeem Afzal** and J Jacob Wikner, "A low-complexity LMMSE based channel estimation algorithm for multiple standards in mobile terminals," in *Proc. Swedish System On Chip Conference (SSOCC)*, Sweden, Linköping, Aug., 2010. (non-peer-reviewed)

5. **Nadeem Afzal** and J Jacob Wikner, "An analysis on the power consumption and performance trande-off in digital signal-feedback $\Delta\Sigma$ modulator," in *Proc. Swedish System On Chip Conference (SSOCC)*, Sweden, Gothenburg, Aug., 2012. (non-peer-reviewed)

6. **Nadeem Afzal** and J Jacob Wikner, "A Strategy of reducing the power consumption in digital signal-feedback delta-sigma modulator of order four," in *Proc. Swedish System On Chip Conference (SSOCC)*, Sweden, Lund, Aug., 2013. (non-peer-reviewed)

7. **Nadeem Afzal** and J Jacob Wikner, "Reducing the hardware and power consumption of a fourth-order digital delta-sigma modulator," in *Proc. Swedish System On Chip Conference (SSOCC)*, Sweden, Linköping, Aug., 2014. (non-peer-reviewed)

Abbreviations

$\Delta\Sigma$	Delta-sigma Modulator
DAC	Digita-to-analog Converter
OS$\Delta\Sigma$DAC	Oversampling Delta Sigma Digital-to-analog Converter
OSR	Oversampling Ratio
ADC	Analog-to-digital Converter
DEM	Dynamic Element Matching
WLAN	Wireless Local Area Network
IF	Intermediate Frequency
EFM	Error-feedback Delta-sigma Modulator
STF	Signal transfer function
NTF	Noise transfer function
FIR	Finite impulse response
conv-EFM	Conventional Architecture of Single-stage Error-feedback Modulator
SNR	Signal-to-noise Ratio
DEC	Binary-to-unitary Decoder
prop-EFM	Proposed Architecture of Single-stage Error-feedback Modulator
VHDL	Very High Speed Integrated Circuit Hardware Description Language

Contents

Chapter 1

Introduction

1.1 Introduction

In the early twentieth century, the electrical transmission was used to carry out by sending the quantized samples of the message waveform. Later on, in the 1940s the transmission head room was increased by sending the errors between the successive quantized samples. These errors were predicted through a feedback system known as delta-modulator (Δ-modulator), whose block diagram is shown in Fig. 1.1 The Δ-modulator was built independently for the first time

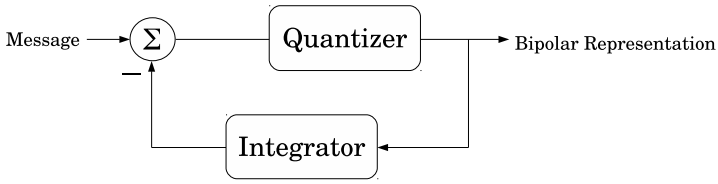


Figure 1.1: Block diagram of Δ-modulator.

by ITT Laboratories [1, 2], Philips Research Laboratories [3, 4] and Bell Telephone Labs [5]. The delta modulator has a number of limitations, for example, incapability to modulate a DC, poor performance for high-frequency signals and inevitable a need for an integrator in the demodulator, etc. In order to cope with these discrepancies, the delta-sigma modulator ($\Delta\Sigma$) was suggested by Inose *et al.* in 1962 [6, 7] after the introduction of oversampling and noise-shaping concepts employing error-feedback by Cutler in 1954 [8] (Fig. 1.2). The

modulator was labeled as $\Delta\Sigma$ (the Δ for sampling and the Σ for integration.) Later on, after the invention of the decimation filter by Goodman in 1969 [9], Candy introduced in 1974 a full multi-bit $\Sigma\Delta$ [10] modulator. He also renamed it as $\Sigma\Delta$-modulator with the possible argument that the integration operation is performed after the sampling thus just like the root-mean-square, the Δ should be appended to the Σ. Both notations are today equally popular and the choice of proper notation between these two is may not be an earth shaking dispute. In this report, we pay respect to the inventor and the notation $\Delta\Sigma$ is used throughout the text.

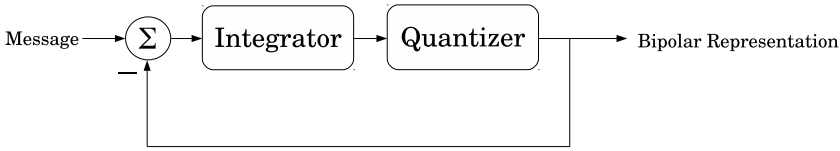


Figure 1.2: Block diagram of $\Delta\Sigma$-modulator.

Typically, non-linearities in digital-to-analog converters (DACs) are exponentially proportional to the length of the digital control words applied to their inputs. In order to reduce the word length of the DAC digital input, Bhagwati [11] used digital $\Delta\Sigma$ in 1982 (Fig. 1.3). The idea was introduced as a modification to the first-order interpolating DAC architectures [12–14]. Since then, it has been widely adopted in the oversampling $\Delta\Sigma$ DAC (OS$\Delta\Sigma$DAC), for example, [15–34]. In digital $\Delta\Sigma$ modulators the input is re-quantized to a shorter word length and the resulting quantization error due to that operation is also spectrally shaped. Thus, the performance of the $\Delta\Sigma$ is determined by the quantization bits, the filtering (for the spectral shaping) of the quantization error, oversampling ratio (OSR) etc.

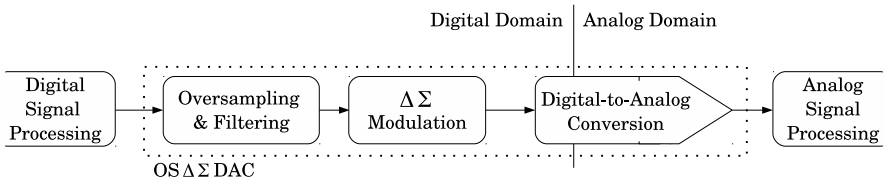


Figure 1.3: Simplified block diagram of oversampling $\Delta\Sigma$ digital-to-analog conversion.

The utilization of digital $\Delta\Sigma$ is not limited to digital-to-analog conversion only. It is also used in analog-to-digital conversion [35–38], in phase-locked

loops [39–49], and as a source to generate dithering signals [50–56], to segment the DAC further [57, 58] and in multiple-input, multiple-output transceivers [59], etc. All of the above signal processing blocks are used for narrow-, wide- and ultra-wide-band applications like digital audio [60–62], handsets [63–65], biomedical [66, 67], TV [68–70], digital radio tuners [71, 72] and wireless infrastructures [73–75].

1.2 Motivation

In this section, the targeted applications of our work are presented. For the applications, the need of the low power consuming $\Delta\Sigma$ of enhanced sampling frequency, is motivated.

For low-power high-bandwidth applications, the multi-bit $\Delta\Sigma$-based ADC with limited oversampling ratio is favored [36]. By using the multi-bit quantizer, not only the complexity of the analog reconstruction filter is relaxed but the resolution is also increased. Depending upon the topology of such an ADC, the digital output is fed back at one or multiple places into the analog circuitry via a multi-bit DAC. The non-linearities in the DAC are one of the critical bottlenecks for the overall performance of the ADC. In order to cope with these non-linearities, various dynamic element matching (DEM) techniques have been used, for example, [76–89]. A disadvantage of the DEM is that size and power consumption grow exponentially with the increased word length and higher resolution of the digital feedback signal. A second disadvantage is that it converts the mismatch into noise that also affects the performance of the ADC. Because of these facts, the solutions without DEM, i.e., consuming less power, for example [35–37], are gaining more interest. In the "DEM-free" architectures, the digital $\Delta\Sigma$ is used to reduce the resolution of the outermost feedback signal since the non-linearities in the outermost feedback appear at the ADC output with the same transfer function as the input. Thus, for such applications, the lower power consuming digital $\Delta\Sigma$ architectures which could operate at higher sampling rate would be very desirable.

Recently, the 60-GHz transmitters have become attractive for short-range wireless communication between systems using bandwidths in the order of hundreds of megahertz. The main reason is that these exploit the unlicensed radio bands, 57-64 GHz [90]. With some modifications, the 5 GHz (the radio-frequency of WLAN) is used as intermediate-frequency (IF) in these transmitters [91]. It is hard for conventional digital-to-analog converters to produce

≈10-bit resolution at this high IF. However, the time-interleaved $\Delta\Sigma$-based DACs [92, 93] have the potential to carry out the task. In these architectures, multiple $\Delta\Sigma$ units, clocked at a lower frequency, are time-interleaved. For instance, in order to achieve the clock speed of $n \times f$, the n number of $\Delta\Sigma$ units are interleaved while each operating at the clock frequency of f. There is a trade-off between the clock frequency and the power consumption of the unit. A $\Delta\Sigma$ unit that consumes less power and operates at a higher sampling rate would of course be desirable.

1.3 Contribution

In this thesis, a number of digital $\Delta\Sigma$ architectures are proposed. The estimates of the area, the power consumption and the highest operable frequency, are obtained, for the comparison purpose, after synthesizing the designs in 65-nm standard cell library provided by the foundry. The proposed designs are not only lower power consuming but also operable at the higher frequencies compared to the conventional ones.

- The quantization bits of the $\Delta\Sigma$ not only determine the complexity of the DAC but also effect the complexity of $\Delta\Sigma$ itself. Thus, the $\Delta\Sigma$ output could induce a digital and/or analog hardware over design in OS$\Delta\Sigma$DAC. In order to avoid it while maintain the performance, the output of a multi-bit error-feedback $\Delta\Sigma$ modulator (EFM) of arbitrary order is described with a term: cardinality (defined as the total number of unique levels of a digital signal.) Expressions of the input scale for the desired output cardinality and the signal range, are also derived. The proposed criteria also ensure the stable operation of the EFM by avoiding the overflow at the output.

  This work is intended to publish with (preliminary) title: **On scaling and output cardinality of multi-bit digital error-feedback modulators**.

- In the second phase of our work, a lower power consuming architecture of the EFM of arbitrary order is proposed. Usually, the EFM output is encoded to the control sequences compatible to the unit element based DAC. After adopting modified encoding strategies a significant amount of hardware in the proposed design is removed. The proposed architecture

is also operated, successfully, at more strict delay constraints than the conventional architecture without any timing violations.

This work has resulted in a publication with the title **Reducing complexity and power of digital multi-bit error-feedback $\Delta\Sigma$-modulators**.

- A strategy to reduce the hardware of conventional $\Delta\Sigma$ has been devised recently that uses multiple cascaded modulation units [40, 94]. A similar approach is devised in our work where we cascade several modified EFM units. The compatibility issues among the units (since the output of each is represented by the set of encoded signals) are resolved by a number of architectural modifications. The digital processing is distributed among the units by splitting the primary input. It is shown that instead of cascading the whole EFM units, it is enough to cascade their loop filters only. This leads to reduction in area, power consumption and critical path.

  These findings are intend to publish with preliminary title **Digital multi-bit cascaded error feedback $\Delta\Sigma$ modulators with reduced hardware and power consumption.**

For the sake of comparison, all of the above mentioned strategies are applied to a fourth-order 5-bit EFM. Saving in terms of the area, the power consumption and the critical path are presented.

1.4 Thesis Organization

Rest of the thesis is organized as follows:

- In **chapter 2**, the basic $\Delta\Sigma$ topologies: signal feedback and error-feedback are analyzed, briefly, for the purpose of digital-to-digital conversion. The analysis includes the linear models of the quantizer and the transfer function of the modulators with respect to the FIR function of the loop filter. After considering the EFM as one of the most suitable topology, its implementation detail is presented. An implementation of the EFM of arbitrary order is presented as the conventional EFM architecture. An expression for the total in-band noise at the output of the EFM is also presented.

- In **chapter 3**, a scaling method of the EFM for the desired output cardinality, is presented. The cardinality is defined as the total number of

unique signal levels at the output of the EFM. In order to monitor the overflow at the output, the mathematical expressions describing the effect on the signal ranges, are derived. A modified schematic of the EFM is presented in order to show the separated signal- and the error-path. In the modified diagram, the input bus is split into MSB-containing and LSB-containing paths. For the desired output range, the handles in the form of input scale, bus-split configurations, and, the order and type of the loop filters, are also provided. An expression for the maximum signal-to-noise ratio is also presented when the input is uniformly distributed random signal and independent to the quantization error.

- In **chapter 4**, the modification methods to the conventional EFM architecture of arbitrary order, are presented. In one of the methods, the bus-splitter and the binary-to-unitary decoder are used to remove the significant amount of circuitry of the modulator. The architectural properties involved in this method are discussed in detail. In the other method, the processing of the quantization error is distributed into a number of loop filters. In fact, the method presents the hardware reduced implementation of the cascaded error-feedback modulator: where several EFMs are cascaded in order to reduce the hardware. It is shown that it is enough to only nest the loop filters instead of cascading the whole EFM stages.

- In **chapter 5**, the savings are presented after applying the modifications (according to the methods which will have been described in chapter 5) to a 5-bit conventional EFM of order four. In this regard, the EFM is configured for the maximum possible SNR. Then, the OSR range where its performance is better than the 5-bit fifth-order modulator, is identified. Later, the architectural modifications are applied to the configured 5-bit fourth-order EFM.

  The area, the power consumption and the sampling frequency of the EFM after realizing it by using the conventional and the proposed approaches, are presented. Saving in the silicon area and dynamic power consumption, and the improvements in the operating frequencies are identified and analyzed.

- In **Chapter 6** the conclusions of this work are presented and the future trends are identified.

Chapter 2

Conventional $\Delta\Sigma$ Modulators

2.1 Introduction

With increasing signal frequencies and bandwidths most analog signal processing is being replaced by digital signal processing in order to increase reliability of transceivers [95]. Due to the shrinking analog portion, digital-to-analog converters are being shifted closer towards antennas. The move has tightened the DAC requirement for linearity, speed, complexity, etc.

Unit element-based DACs are most commonly used DACs for high-speed operation (for example, current-steering DAC [96].) The unit elements of the DAC are controlled by the digital control signal from the DSP (digital signal processing block). In digital-rich and analog-light process, the complexity of such an high-speed DAC can be reduced by prepending a digital $\Delta\Sigma$ [23], as shown in Fig. 2.1. In $\Delta\Sigma$DAC, the $\Delta\Sigma$ does not only re-quantize the digital signal from the DSP, with the quantization step of $\Delta = g$, to a lower granularity but also mitigates the in-band deviation (due to the re-quantization) by predicting and correcting the future quantization-error values. The processing of the $\Delta\Sigma$ is easiest to understand when it is described in z-domain using its linear model as [97]

$$Out\,(z) = In\,(z) \times \mathrm{STF}\,(z) + Noise\,(z) \times \mathrm{NTF}\,(z)\,, \tag{2.1}$$

where In, Out, and $Noise$ represent the input signal applied to the $\Delta\Sigma$, the obtained modulated output signal and the quantization error added by the coarse

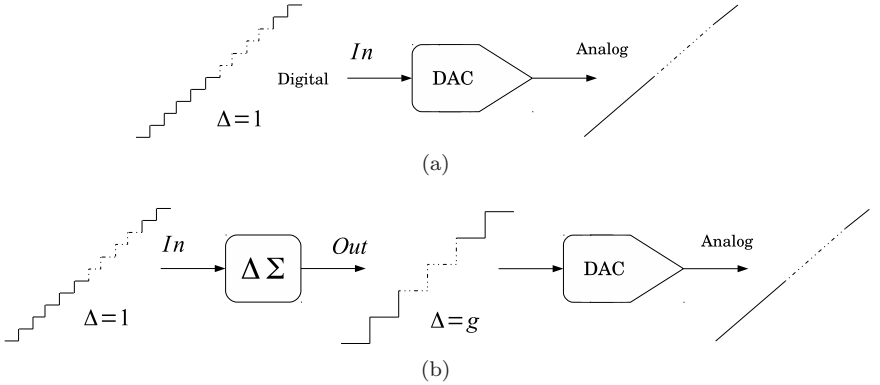


Figure 2.1: Block diagrams of DAC (a) and ΔΣDAC (b).

quantizer, respectively. In a typical low pass ΔΣ, the STF (signal-transfer-function) represents a low- or all-pass whereas the NTF (noise-transfer-function) represents an high-pass function.

The high-pass characteristics of the NTF can only be exploited if the input to the ΔΣ is over-sampled, i.e., sampled at a rate higher than the Nyquist-rate. The cost and the performance of the ΔΣ depends on the quantization bits, the order and topology of the filter, the sampling rate and word length of the input, etc.

2.2 Quantization Process

Assume, both the input and the output of the quantizer are digital integer-valued signals. Then, the quantization operation on an arbitrary sample i of its input can be performed by scaling and rounding or truncating [94], as given by

$$Y[i] = \frac{T[i]}{g} + \epsilon[i], \tag{2.2}$$

where the T and the Y are the input and the output of the quantizer, respectively. The $0 \leq \epsilon[i] < 1$ represents the rounding/truncation error and scalar g represents the quantization step size. The process can be described in the z-domain after representing $g\epsilon(z)$ with $\varepsilon(z)$ as

$$gY(z) = T(z) + \varepsilon(z). \tag{2.3}$$

Thus, the quantizer can coarsely be modeled by the sum of its input and an error signal ε (quantization error).

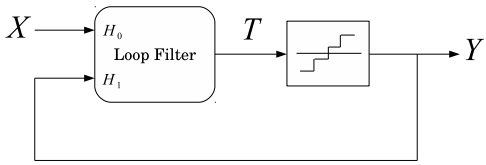


Figure 2.2: A block diagram of signal feedback ΔΣ (SFM).

2.3 Basic Topologies of the ΔΣ Modulators

Modifications to the basic ΔΣ architecture have been proposed many times, but fundamentally, the signal processing is the same as described in (2.1). There are two basic ΔΣ architectures known as signal-feedback modulator (SFM) and error-feedback modulator (EFM).

2.3.1 Signal-feedback Modulator

A block diagram of the signal-feedback modulator is shown in Fig. 2.2 [27]. The structure is composed of two blocks: a quantizer that produces the quantized output and a loop filter that mitigates the in-band performance deterioration caused by the quantization error. The X and the Y are transformed through the H_0 and the H_1 functions, respectively. The z-transforms of the output of the loop filter can can be described as

$$T(z) = X(z)\,H_0(z) + Y(z)\,H_1(z)\,. \tag{2.4}$$

After substituting (2.4) in (2.3), we get

$$gY(z) = X(z)\,\frac{H_0(z)}{1 - H_1(z)} + \varepsilon(z)\,\frac{1}{1 - H_1(z)}. \tag{2.5}$$

After comparing (2.1) and (2.5) we get

$$\begin{aligned} H_0(z) &= \frac{\mathrm{STF}(z)}{\mathrm{NTF}(z)}, \\ H_1(z) &= 1 - \frac{1}{\mathrm{NTF}(z)}. \end{aligned} \tag{2.6}$$

The relations show that the loop filter is designed according to the desired STF and NTF.

There exist a number of topologies of the loop filter of the SFM, for example, [23, Sec. 5.6] [27, Sec. 4.4] [98]. Except the first order ΔΣ modulator, the loop

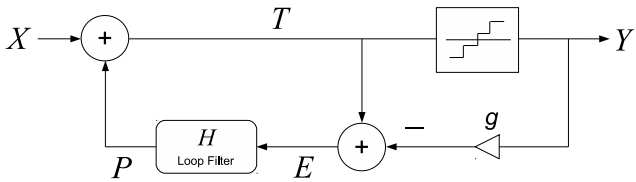


Figure 2.3: A block diagram of error feedback ΔΣ (EFM).

filter of SFM is always composed of single or multiple infinite-impulse-response (IIR) filters. The presence of poles in the loop filter makes the stability of the higher order SFM design a major design challenge. There exist a number of criteria to ensure the stability but extensive simulations are still required. Thus, the SFM is rendered to a high design complexity once the order of modulation increases.

2.3.2 Error-feedback Modulator

The noise shaping was first introduced using the error-feedback modulator structure, as shown in Fig. 2.3. As the name indicates, after being obtained by subtracting the output of the quantizer from its input, the (quantization) error is fed back to the loop filter of transfer function $H(z)$. The quantization error can mathematically be expressed as

$$E(z) = T(z) - gY(z). \tag{2.7}$$

After comparing (2.3) and (2.7) we get

$$E(z) = -\varepsilon(z). \tag{2.8}$$

The sum of the output of the loop filter, $P(z) = E(z)H(z)$, and the X, is applied again to the quantizer. In this way, the loop continues. The T can be described in z-transform as

$$\begin{aligned} T(z) &= X(z) + E(z)H(z) \\ &= X(z) - \varepsilon(z)H(z). \end{aligned} \tag{2.9}$$

After substituting T from (2.9) in (2.3), the following is obtained

$$gY(z) = X(z) + \varepsilon(z)(1 - H(z)). \tag{2.10}$$

After comparing (2.1) and (2.10), the relation between the loop filter function and the NTF is obtained as

$$H(z) = 1 - \mathrm{NTF}(z), \tag{2.11}$$

while the $\mathrm{STF}(z) = 1$. According to (2.11), as long as NTF is finite-impulse-response (FIR) function the loop filter is also an FIR function.

Unlike the SFM, the EFM design is simple and does not fall into stability issues due to the FIR loop filter. It is simple to protect the EFM from quantizer overflow especially when the quantization bits are higher than the order [99]. Conclusively, the multi-bit higher order EFM topology is comparatively simple and better suitable as a digital $\Delta\Sigma$ modulator.

2.4 Implementation Details of the Error-feedback Modulator

The EFM can be divided into three sub-blocks: quantization process, filtering process and addition between the input and the filtered error. In order to present the implementation details of the processes, the word lengths of signals X, P, T, E and Y are represented as x, p, t, e and y, respectively.

According to section 2.2 and (2.8), the g is described as

$$g = \frac{|E|}{|\epsilon|} \tag{2.12}$$

where the $|E|$ and $|\epsilon|$ represent the magnitudes of E and ϵ, respectively. Assume the E has l number of integer and f number of fractional bits such that $e = l + f$ and its magnitude is described as $|E| = E^+ - E^- = 2^l - 2^{-f}$, where E^+ and E^- are its peak positive and peak negative values, respectively. Assume, the quantization is a truncation operation, then, the $|\epsilon|$ being the truncation error has the maximum value of $1 - 2^{-e}$. Hence, the value of g is given by

$$g = \frac{\left(2^l - 2^{-f}\right)}{\left(1 - 2^{-e}\right)} = 2^l. \tag{2.13}$$

Thus, by substituting the value of g from (2.13) and that of ε from (2.8) in (2.2), we get

$$T(z) = 2^l Y(z) + E(z). \tag{2.14}$$

The relation, (2.14), describes the operation of a bus-splitter. An example, explaining the split (truncation) operation, is described in Table 2.1. Two MSBs

Table 2.1: An example where the T is quantized to Y and the E represents the quantization error. The value of g in this example is 2.

T	Y	E
two's complement	two's complement	unsigned
3.5 $(011.1)_2$	1 $(01)_2$	1.5 $(1.1)_2$
3 $(011.0)_2$	1 $(01)_2$	1 $(1.0)_2$
2.5 $(010.1)_2$	1 $(01)_2$	0.5 $(0.1)_2$
2 $(010.0)_2$	1 $(01)_2$	0 $(0.0)_2$
1.5 $(001.1)_2$	0 $(00)_2$	1.5 $(1.1)_2$
1 $(001.0)_2$	0 $(00)_2$	1 $(1.0)_2$
0.5 $(000.1)_2$	0 $(00)_2$	0.5 $(0.1)_2$
0 $(000.0)_2$	0 $(00)_2$	0 $(0.0)_2$
-0.5 $(111.1)_2$	-1 $(11)_2$	1.5 $(1.1)_2$
-1 $(111.0)_2$	-1 $(11)_2$	1 $(1.0)_2$
-1.5 $(110.1)_2$	-1 $(11)_2$	0.5 $(0.1)_2$
-2 $(110.0)_2$	-1 $(11)_2$	0 $(0.0)_2$
-2.5 $(101.1)_2$	-2 $(10)_2$	1.5 $(1.1)_2$
-3 $(101.0)_2$	-2 $(10)_2$	1 $(1.0)_2$
-3.5 $(100.1)_2$	-2 $(10)_2$	0.5 $(0.1)_2$
-4 $(100.0)_2$	-2 $(10)_2$	0 $(0.0)_2$

from the 4-bit signal T are truncated and the truncation error in the form of 2 LSBs is collected to E where the T and Y are represented with 2's complement and the E being deprived of the sign bit, is unsigned. The value of g here is 2^1. Note that the T and E have same fractional bits, i.e, f. Hence, the transformation of the quantize and subtract operation to the bus-split operation for the $g = 2^l$ is graphically shown in Fig. 2.4.

A block diagram of addition between the X and P, is shown in Fig. 2.5. The word length of the sum (T) is related as $t = \max\{x, p\} + 1$. The same schematic diagram is used to represent every addition and subtraction in the designs presented in this thesis. For subtraction, a hard value '1' is applied at

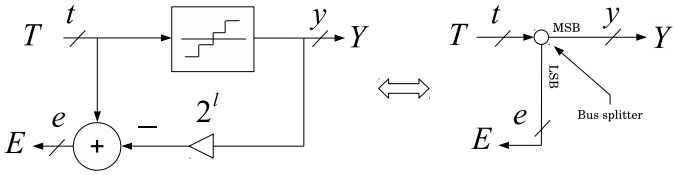


Figure 2.4: The quantization and subtraction in an EFM is replaced by a bus-split operation.

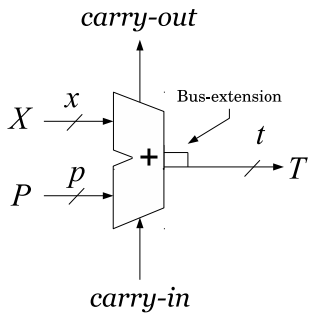


Figure 2.5: Block diagram of an adder. The same schematic is used throughout the thesis.

the carry-in location and the bits of subtrahend are inverted. For example, the subtraction of B from A is performed as, $A - B \rightarrow A + \overline{B} + 1$ where $\overline{B}$ represents the one's complement of B.

The EFM being a feedback system must contain at least one delay element in the loop filter (H). With only one delay element in the loop filter, i.e., $H(z) = z^{-1}$, the coefficients of NTF and those of H are related according to (2.7) as

$$\begin{aligned} \mathrm{NTF}(z) &= 1 - H(z) \\ &= 1 - z^{-1}. \end{aligned} \tag{2.15}$$

In other words, the condition for stability of arbitrary order EFM is that the zeroth coefficient of the polynomial of NTF must be unity. For the r-tap finite-impulse-response function of $\mathrm{NTF}(z) = h_0 - \sum_{u=1}^{r} h_u z^{-u}$ (where the $h_0 = 1$,)

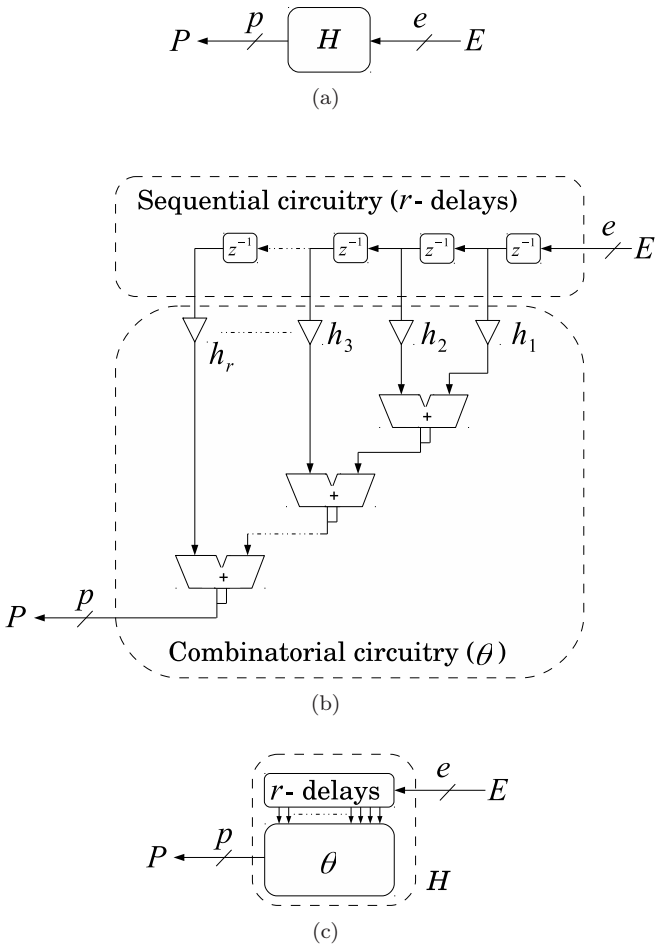


Figure 2.6: The loop filter is composed of two blocks r-delay (sequential circuitry) and θ (combinatorial circuitry). The block diagram of (a) is modified to (c) by explicitly representing θ and r-delays.

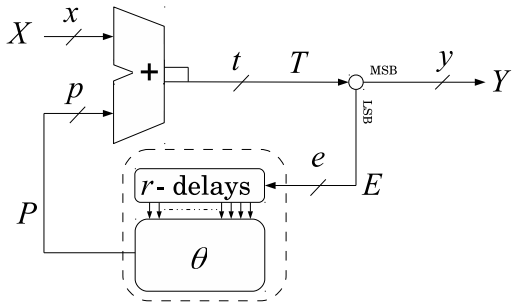


Figure 2.7: A schematic diagram of rth-order EFM, termed as conv-EFMr.

the loop filter is described as

$$\begin{aligned} H(z) &= 1 - \mathrm{NTF}(z) \\ &= 1 - h_0 + \sum_{u=1}^{r} h_u z^{-u} \\ &= \sum_{u=1}^{r} h_u z^{-u}, \end{aligned} \tag{2.16}$$

where h's are the filter coefficients. A general schematic of the r-tap loop filter is shown in Fig. 2.6. The block diagram of the H (shown in Fig. 2.6a) is decomposed into sequential circuitry, r-delay, and combinatorial circuitry, θ. The explicit blocks, r-delay and θ are shown in Fig. 2.6c for the future purpose.

After replacing the sub-blocks, the EFM is shown in Fig. 2.7. This schematic with multiplier-less implementation of θ is referred as the conventional implementation of the EFM (conv-EFM) in this thesis.

Although the conv-EFM design is simple but a significant amount of circuitry can further be reduced in order to save the hardware and the power consumption and to reach GHz operating speeds using standard components.

2.5 Total In-band Noise of the Error-feedback Modulator

The output of the EFM is described as the sum of its input and the spectrally shaped quantization error, as in (2.10). The $E = -\varepsilon = -g\epsilon$ where the ϵ being the truncation error, is assumed to be white [23]. Then, the total in-band noise

($\mathcal{N}$) introduced by the EFM can be described as

$$\begin{aligned}\mathcal{N} &= \frac{1}{\pi}\int_0^{\pi/\mathrm{OSR}} \left|\mathrm{NTF}\left(\omega T\right)\right|^2 \sigma_E^2 \mathrm{d}\omega T \\ &= \sigma_E^2 \frac{1}{\pi}\int_0^{\pi/\mathrm{OSR}} \left|1 - H\left(\omega T\right)\right|^2 \mathrm{d}\omega T,\end{aligned} \tag{2.17}$$

where, $\sigma_E^2 = \sigma_\varepsilon^2 = g^2\sigma_\epsilon^2 = 2^{2l}\frac{1}{12}$ represents the variance of the quantization error and the OSR represents the oversampling ratio of the input. To solve the integral of (2.17), term $\left|1 - H\left(\omega T\right)\right|^2$ is simplified as

$$\begin{aligned}\left|1 - H\left(\omega T\right)\right|^2 &= \left|\sum_{u=0}^{r} d_u e^{-j\omega u}\right|^2 \\ &= \sum_{u_1=0}^{r} d_{u_1} e^{-j\omega u_1} \sum_{u_2=0}^{r} d_{u_2}^* e^{j\omega u_2} \\ &= \sum_{n=0}^{r}\left(\sum_{u_1=0}^{r-n} d_{u_1} d_{u_1+i}^* e^{j\omega i} + \sum_{u_2=n}^{r} d_{u_2} d_{u_2-n}^* e^{-j\omega n}\right) \\ &= \sum_{n=0}^{r}\sum_{u=0}^{r-n} d_u d_{u+n} U_n \cos(n\omega),\end{aligned} \tag{2.18}$$

where

$$U_n = \begin{cases} 1 & n = 0 \\ 2 & n \neq 0 \end{cases}$$

where for all u, $d_u = -h_u$ and $d_0 = 1$. After substituting (**??**) in (2.17), we get the close form expression of the total in-band noise as

$$\mathcal{N} = \frac{2^{2l}}{12}\lambda \tag{2.19}$$

where

$$\lambda = \sum_{n=0}^{r}\sum_{u=0}^{r-n} h_u h_{u+n} U_n \frac{1}{n\pi}\sin\left(\frac{n\pi}{\mathrm{OSR}}\right). \tag{2.20}$$

The expressions (2.19) and (2.20) are used to measure the effects on performance of the EFM caused by the later presented architectural modifications.

2.6 Conclusions

The fundamentals of ΔΣ-DAC have been discussed. The linear model of the quantization process has been presented. Two basic topologies of the ΔΣ mod-

ulator: signal-feedback modulator and error-feedback modulator have been presented for the application of digital-to-digital conversion. The digital implementation of the error-feedback $\Delta\Sigma$ modulator using a conventional approach has been provided. A close form expression for the total in-band noise has also been presented.

Chapter 3

Scaling and Output Cardinality of Error-feedback Modulators

3.1 Introduction

The signal-levels and word length of the output of an EFM (error-feedback modulator) are some of the critical parameters that describe the stable, high performing and low power consuming construction of $\Delta\Sigma$DAC. Some of the previous methods to determine these parameters are described in [99] and [100]. In [99], the total number of unique signal levels (termed as cardinality) produced at the output of the error-feedback modulator (shown in Fig. 2.3) has been determined by using the $\mathcal{L}_1$ norm of the loop filter. A sufficient stability criterion of the EFM has been provided in [100] where an EFM with a truncator of $q+1$ bits and an FIR loop filter $H(z)$ (that contributes to a q-bit increase in the data-flow) is stable. The EFM is considered as "un-stable" if it produces a poor signal-to-noise ratio (SNR) compared to that predicted by the linear models, according to [100, Sec. I] and [23, Sec. 4.1].

In addition to these, the output signal (minimum) peak to (maximum) peak range has also to be determined in order to devise methods that prevent the output overflow. Furthermore, the actual output range of the EFM may not be equal to the theoretical range. For instance, the theoretical range of a $(q+1)$-bit signal represented in two's complement, is given by $\{-2^q, 2^q - 1\}$. Thus, by increasing the actual output signal range towards the theoretical range, maximum performance can be obtained.

In this chapter, the output range is expressed mathematically in terms of the ranges of the signals of the EFM. Through these expressions, a method for the desired output range is also devised. The achievable SNR is also provided in terms of the signal ranges and the type of the loop filter. This chapter summarizes the detailed derivations that has been presented in [Paper B].

3.2 Cardinality of Digital Signals

In this section, cardinality of a digital signal is defined. The relations between the signal ranges of the inputs and the outputs of the signal processing elements are also given.

The total number of unique levels contained in a digital signal is defined as its cardinality. If X is a digital, integer-valued, x bit signal represented in two's complement (where the weight of LSB is one,) then its cardinality is represented as

$$\mathcal{C}_X = X^+ - X^- + 1, \tag{3.1}$$

where X^+ and X^- are the positive and negative peak values of X, respectively. Thus, the cardinality of a digital signal is determined by the peak values of the signal. The relationship between the peak values of the signals of the combinatorial processing elements (adders and bus-splitters) are given as follows. The relations for an adder adding n number of inputs, shown in Fig. 3.1a, are described as

$$\begin{aligned} O^+ &= \sum_{i=1}^{n} I_i^+, \\ O^- &= \sum_{i=1}^{n} I_i^-, \end{aligned} \tag{3.2}$$

where O is the output and I_i is the ith input of the adder. Similarly, the peak values of the MSB containing signal among the n split signals after a bus-splitter, as shown in Fig. 3.1b, is given as

$$\begin{aligned} O_n^+ &= \left\lfloor \frac{I^+}{\prod_{i=1}^{n-1} \mathcal{C}_{O_i}} \right\rfloor, \\ O_n^- &= \left\lfloor \frac{I^-}{\prod_{i=1}^{n-1} \mathcal{C}_{O_i}} \right\rfloor, \end{aligned} \tag{3.3}$$

where $\prod_{i=1}^{n-1} \mathcal{C}_{O_i}$ is equal to LSB-weight of the O_n.

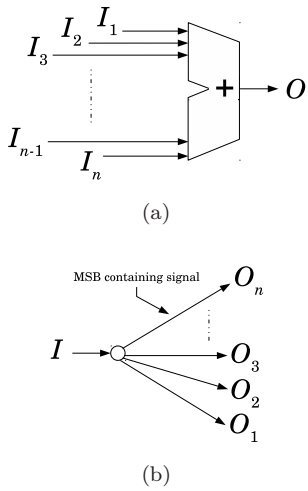


Figure 3.1: An adder and a bus-splitter. (a) Adder adding n signals. (b) A signal split into n signals.

The expressions for the cardinality and the range of the EFM output are obtained by using the relations given in (3.2) and (3.3), to the processing elements in the following sections.

3.3 A Modified Schematic of the Error-feedback Modulator

For convenience, the EFM shown in Fig. 2.7 is redrawn in a modified way without effecting the overall transfer characteristics or the total hardware. The strategy of modification is as follows: if an adder is followed by a bus-splitter then the adder can be split by moving the bus-splitter from its output to its inputs, as shown in Fig. 3.2a and 3.2b. In the figure, the adder adding X and P is split into *add*-1 and *add*-2 by moving the splitter backward. In the split form, the *add*-1 produces the Y and the *add*-2 produces the E. Both the adders belong to the same carry chain. The bit significance of the signals remains conserved, i.e., the LSB-weights of the M, Q, c and Y are equal whereas the MSB-weights of the L, S and E are equal. Furthermore, in the case of unequal q and m, the sign-bit of the signal with shorter word length is extended up to $q = m$. The word lengths of the inputs and outputs of the splitters are related

as

$$\begin{aligned} x &= l + m, \\ p &= e + q. \end{aligned} \tag{3.4}$$

The X being integer-valued (as assumed in the beginning of the previous section) has $f = 0$ whereas the P depends on the nature of the loop filter. In the case of integer-valued loop filter coefficients, we will have the $e = l$. Otherwise, if the loop filter coefficients are fractional-valued as well, then, the output of the loop filter has to be quantized to hold the fractional accuracy. Assume, the output of the loop filter is quantized to f number of fractional bits then, the relation between the word lengths of *add*-1 will be $e = l + f$. The MSB weight of L, E and S remains equal to 2^l. Thus, according to (2.14), we have

$$\begin{aligned} X &= 2^l M + L, \\ P &= 2^l Q + S, \end{aligned} \tag{3.5}$$

where all of the signals are represented in z-domain. The inputs and outputs of the adders are related as

$$\begin{aligned} Y &= M + Q + c, \\ 2^l c + E &= S + L. \end{aligned} \tag{3.6}$$

Now, by solving (3.5) and (3.6), we get

$$\begin{aligned} 2^l Y + E &= 2^l M + L + 2^l Q + S \\ &= X + P, \end{aligned} \tag{3.7}$$

which is in conformity with relation $X + P = T = 2^l Y + E$ of Fig. 3.2a. By following the above procedure of adder splitting, the alternative structure of the EFM (of Fig. 2.7) is shown in Fig. 3.3. Both the drawings (Fig. 2.7 and 3.3) produce the output (Y) of the same transfer function, given as,

$$2^l Y(z) = X(z) + (H(z) - 1) E(z). \tag{3.8}$$

By using the modified drawing the EFM output range can be determined from the split configurations of X and P.

3.4 Expressions of the Output Signal Range

In this section, signal range of the Y (EFM output) is expressed, mathematically, in terms of loop filter coefficients and the input range. An example is also presented to show the importance of the derivations.

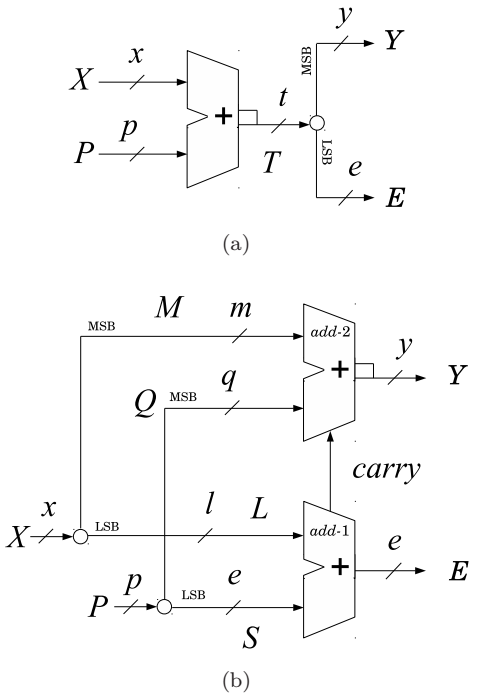


Figure 3.2: The adder following a bus-splitter can be split by moving the splitter from its output to its inputs.

According to Fig. 3.3, the output range ($\{Y^-, Y^+\}$) is obtained by applying (3.2) to *add*-2, as given by

$$\begin{aligned} Y^+ &= M^+ + Q^+ + c^+, \\ Y^- &= M^- + Q^-, \end{aligned} \tag{3.9}$$

where c^+ is unity since it is the carry from *add*-1. For a given input range, $\{X^-, X^+\}$ and a loop filter of type (2.16), peak values of M and Q, according to (3.3) and [Paper B], are expressed as

$$M^+ = \left\lfloor \frac{X^+}{2^l} \right\rfloor + 1, \quad M^- = \left\lfloor \frac{X^-}{2^l} \right\rfloor, \tag{3.10}$$

$$Q^+ = \left\lfloor \frac{\lfloor (2^l - 2^{-f}) \sum h^+ \rfloor}{2^l} \right\rfloor, \quad Q^- = \left\lfloor \frac{\lfloor (2^l - 2^{-f}) \sum h^- \rfloor}{2^l} \right\rfloor, \tag{3.11}$$

where, $\sum h^+$ and $\sum h^-$ are the sum of positive and the sum of negative filter coefficients, respectively. By substituting (3.10) and (3.11) in (3.9), the relation

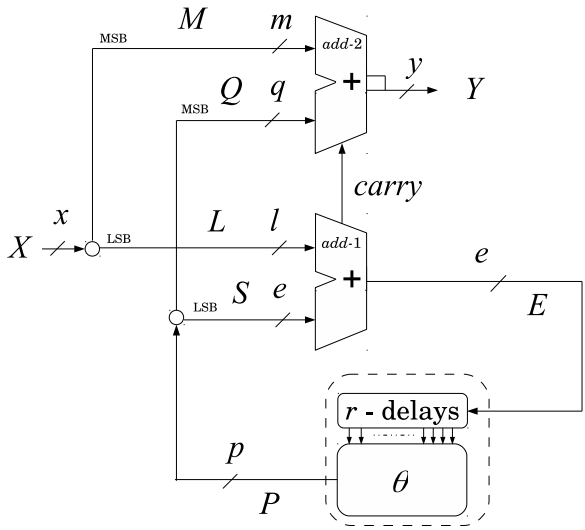


Figure 3.3: The adder of the EFM (as shown in Fig. 2.7) is split into two adders (*add*-1 and *add*-2) by moving the bus-splitter from its output to the inputs.

for the output range is described as

$$\begin{aligned} Y^{+} &= \left\lfloor \frac{X^{+}}{2^{l}} \right\rfloor + \left\lfloor \frac{\left\lfloor \left(2^{l} - 2^{-f}\right) \sum h^{+} \right\rfloor}{2^{l}} \right\rfloor + 1, \\ Y^{-} &= \left\lfloor \frac{X^{-}}{2^{l}} \right\rfloor + \left\lfloor \frac{\left\lfloor \left(2^{l} - 2^{-f}\right) \sum h^{-} \right\rfloor}{2^{l}} \right\rfloor . \end{aligned} \tag{3.12}$$

Conclusively, both the M and the Q contribute to the output range of the EFM through *add*-2. According to (3.10) and (3.11), M depends on the split configuration whereas the Q depends on the type of the loop filter.

As an application, a minimum output word length can be as small as unity and can only be produced through a first-order EFM due to a fact that it does not produce Q (since $\sum h^{+} = 1$ and $\sum h^{-} = 0$). Thus, the minimum output range is given by

$$\{Y^{-}, Y^{+}\} = \{Q^{-}, Q^{+} + 1\}, \tag{3.13}$$

when $M^{+} = M^{-} = 0$ for the EFM of arbitrary order.

As an example, consider an EFM employs a loop filter of order r with the z-transform given by

$$H(z) = \left(1 - z^{-1}\right)^{r}, \tag{3.14}$$

where the filter coefficients are equal to the $(r+1)$th row of Pascal-triangle so that $\sum h^+ = 2^{r-1}$ and $\sum h^- = -2^{r-1}+1$. Due to the integer-valued filter coefficients, the $f = 0$. By substituting these values in (3.11), the range of Q is obtained to be

$$\{Q^-, Q^+\} = \{-2^{r-1}+1, 2^{r-1}-1\}. \tag{3.15}$$

The minimum output range of this EFM is, according to (3.13), given as

$$\{Y^-, Y^+\} = \{-2^{r-1}+1, 2^{r-1}\}, \tag{3.16}$$

and the minimum output cardinality (minimum output signal levels) as

$$\mathcal{C}_Y = Y^+ - Y^- + 1 = 2^r. \tag{3.17}$$

According to (3.16), the output signal can not be represented with r number of bits although the number of output signal levels are 2^r. The block (for example, a unit element-based DAC) following the EFM can still be constructed for the r bit signal but after incorporating a single-level of DC shift while decoding.

Conclusively, the expression for the output signal range gives critical information for the overflow at the output.

3.5 Input Scaling for the Desired Output Signal Range

The overflow at the output of the EFM with an FIR loop filter can be avoided by configuring the parameters like the range of X, the value of l, the order of the loop filter and the type of the filter coefficients, according to (3.12). There could be many configurations of the parameters in order to produce a desired output swing, however, in the this section, we present the way to configure the value of l and to restrict the range of X, with the filter of type given in (2.16).

Consider that the desired output range is $\{Y^{-'}, Y^{+'}\}$ and the output is represented in two's complement with the word length $y \in \mathbb{Z}$. In order to obtain the desired output range, l number of LSBs should be split from the input (X). The value of l can be obtained by substituting the output range of Q (that is obtained from (3.11) when both l and the f are greater than two,) in the following manner:

$$\begin{aligned} l &= x - m \\ &= x - \left\lceil \log_2 \left(Y^{+'} - Q^+ - \left(Y^{-'} - Q^- \right) \right) \right\rceil. \end{aligned} \tag{3.18}$$

Then, the positive and negative ranges of the X should be scaled down using $A_X = \min\{A_1, A_2\}$ as $X^{+'} = \lfloor A_X X^+ \rfloor$ and $X^{-'} = \lfloor A_X X^- \rfloor$. The a_1- and a_2-bit scaling factors $0.5 < A_1 \leq 1$ and $0.5 < A_2 \leq 1$, can be expressed, according to [Paper B], as

$$\begin{aligned} A_1 &= \left\lfloor \frac{\left(Y^{+'} - Q^+\right) 2^{l+a_1} - 1}{X^+} \right\rfloor 2^{-a_1}, \\ A_2 &= \left\lfloor \frac{\left(Y^{-'} - Q^-\right) 2^{l+a_2}}{X^-} \right\rfloor 2^{-a_2}. \end{aligned} \tag{3.19}$$

For the configuration where $l = x$, we must have $A_X = 1$.

Hence, for the desired $Y^{+'}$ and $Y^{-'}$ the input range is either restricted to $\{X^{+'}, X^{-'}\}$ using the scalars or the preceding signal processing block such as interpolation filter in the over sampling $\Delta\Sigma$DAC, is designed in such a way that the EFM receives an already restricted signal.

As an example, consider an EFM is required to produce the output range of $\{-2^{r+1}, 2^{r+1} - 1\}$ with loop filter, given in (3.14). The range of Q is given, according to (3.15) as $\{-2^{r-1}+1, 2^{r-1}-1\}$ and the value of l is given, according to (3.18), as $x - r - 2$. The empirical results in [Paper-B] show that the scalar should be at least of $r + 1$ bits, i.e., $a = a_1 = a_2 = y - 1 = r + 1$. Hence, by using the values of the range of Q, that of l and the a's in (3.19), the value of A_X is obtained to be $A_X = \min\{A_1, A_2\} = A_1 = \left\lfloor \frac{3 \cdot 2^{r+x-2}-1}{2^{x-1}-1} \right\rfloor 2^{-r-1}$.

3.5.1 Signal-to-noise Ratio of the Error-feedback Modulator

In order to show the effect of the input scaling, the SNR of the EFM of arbitrary order is expressed in terms of the input scale, the word length of M and the loop filter coefficients, mathematically. In this derivation, we assume that the input is an integer-valued uniformly distributed random signal.

Assume, X is uniformly distributed between $\{X^-, X^+\}$. Then, its variance can be described as

$$\sigma_X^2 = \frac{\left(X^+ - X^-\right)^2}{12} = \frac{\left(A_X 2^x\right)^2}{12}, \tag{3.20}$$

Now, using the expressions (2.19), (3.4) and (11), the SNR can be expressed as

$$\mathrm{SNR} = \frac{\sigma_X^2}{\frac{2^{2l}}{12}\lambda} = \left(A_X 2^m\right)^2 \lambda^{-1}. \tag{3.21}$$

A 6.02 dB increase in SNR can be made for every bit in m while keeping the λ constant, for particular loop filter and OSR value. For the configurations where the output cardinality is minimum, i.e., $l = x$ according to (3.18), the SNR equals λ^{-1}.

3.5.2 Configuration Choice and the OSR Limit

In this section, two configurations are compared in terms of performance and the complexity. It is shown that the EFM with minimum output cardinality should only be used if the OSR is sufficiently high.

Assume, the output cardinality of $\mathcal{C}_Y = 2^y$ is required to be produced from the EFM by using the loop filter given in (3.14). For this loop filter we have $f = 0$ since filter coefficients are integer-valued and the value of λ can be described, using (2.19)

$$\lambda_{\mathrm{DC}} = \frac{\pi^{2r}}{(2r+1)\,\mathrm{OSR}^{2r+1}} \tag{3.22}$$

Thus, for the desired output cardinality, the EFM could be implemented using two configurations given as:

- $C_I : A_X = 1,\ m = 0,\ r = y,$
  i.e., all of the input bits are applied to a yth-order loop filter,
- $C_{II} : A_X = A_1,\ m = y,\ r = y - \delta,$
  i.e., the $(x - y)$ LSBs of the input are applied to the $(y - \delta)$th-order loop filter while the rest of the y MSBs are bypassed,

where δ is a positive integer can have the values among $\{1, 2, \ldots, y-1\}$. Comparing the two configuration, C_{II} consumes less power since the order as well as the word length to the loop filter is less compared to that of C_I. Among many parameters OSR is one which can be adjusted, in order to maintain the SNR. The SNR values for the two configurations are obtained using (3.21) and (3.22), as

$$\begin{aligned} \mathrm{SNR}_{C_I} &= \lambda_{DC_{C_I}}^{-1} = \frac{(2y+1)\,\mathrm{OSR}^{2y+1}}{\pi^{2y}}, \\ \mathrm{SNR}_{C_{II}} &= (A_X 2^y)^2\, \lambda_{DC_{C_{II}}}^{-1} = \frac{(2y-2\delta+1)\,\mathrm{OSR}^{2y-2\delta+1}}{\pi^{2y-2\delta}}. \end{aligned} \tag{3.23}$$

Due to the fact that C_{II} is a lower power consuming configuration, we want

$$\mathrm{SNR}_{C_{II}} \geq \mathrm{SNR}_{C_I}. \tag{3.24}$$

After substituting (13) in (3.24) we get

$$\mathrm{OSR} \leq \pi \left(A_X 2^y \sqrt{\frac{2y - 2\delta + 1}{2y + 1}} \right)^{1/\delta}. \tag{3.25}$$

Hence, in order to produce y-bit full-scale output a $(y-1)$th-order EFM with the configuration C_{II} should be used, if the OSR follows the inequality, (14).

3.6 Conclusions

The relation between the ranges of the inputs and outputs of the processing elements have been provided. A modified schematic of the error-feedback modulator has been provided that helps in identifying the handles to control the output signal. The peak-to-peak range of the error-feedback modulator output has been determined and expressed mathematically in terms of the input signal range, the loop filter order, the loop filter coefficients and the number of least significant bits of the input applied to the loop filter. A method of scaling the input for the desired output range has also been presented. A systematic approach has been adopted to increase the output signal range to the theoretical limit without causing overflow. The effects of the input scaling and that of the configurations of other involved parameters on the performance has been determined using mathematical expression for the signal-to-noise ratio.

Chapter 4

Complexity and Power Reduction by Architectural Modifications

4.1 Introduction

In order to generate control signals to unit-element-based DACs, the binary weighted output of $\Delta\Sigma$ modulators are often decoded to unitary weighted codes. A block diagram of the processing is shown in Fig. 4.1, where binary weighted output, Y, of the EFM (error-feedback modulator) is decoded into unitary weighted signal, Y_u, using the DEC$\cdot Y_u$ (binary-to-unitary decoder). The output of a unit-element-based DAC is obtained by adding the analog outputs of each unit element that is switched on or off by the control unitary bit. Thus, the total number of ones or zeros in a control code determines the DAC output. In this chapter, two methods of hardware reduction in the conventional implementation of the modulator of order r (termed as conv-EFMr, as shown in Fig. 3.3), without effecting the total number of ones to the DAC, are presented.

In one of the proposed methods, a significant amount of hardware complexity of conv-EFMr is removed by merging the decoder block into the EFM. Due to this unification, the output of the modified EFM architecture, termed here as prop-EFMr (proposed single-stage error-feedback modulator), is represented by a set of multiple unitary coded signals. The details are presented in section 4.2.

In the second proposed method, a modified architecture of the cascade of multiple EFM stages is presented. The strategy of cascading a number of modulators has previously been proposed by other authors. However, our proposed

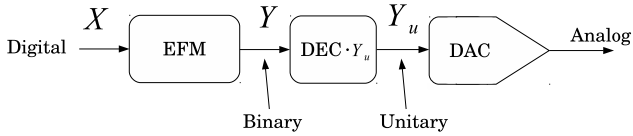


Figure 4.1: An arrangement of ΔΣDAC, i.e., an EFM, a binary to unitary decoder (DEC·Y_u) and a unit elements-based DAC.

method lowers the hardware complexity. The modulator implemented using the proposed approach is termed as proposed cascaded error-feedback modulator (prop-EFM$r_1 r_2 \ldots r_n$) where n number of stages are being cascaded such that $r_1 < r_2 < \cdots < r_n$, i.e., the order of any of the preceding stages is less than those of the following stages.

4.2 Proposed Single-stage Error-feedback Modulator

In this section, the first of the proposed modification methods is described in two steps. In the first step, the combinatorial circuitry of the conv-EFMr is split into two parts: one producing the modulated output signal and the other producing the error-feedback signal. In the second step, the part responsible for producing the modulated output is removed by using the alternative decoding strategy.

4.2.1 Design Step I

As it has been described in section 3.3 (Fig. 3.2), an adder is split if a bus-splitter is propagated from its output to its inputs. By following the same principle, in the first design phase the bus-splitter at signal P, is propagated back inside the combinatorial circuitry (θ) of the conv-EFMr (shown in Fig. 3.3.) It is assumed that the loop filter has multiplier-less implementation, i.e, θ consists of shift and add operations only. The propagation of the bus-splitter splits the θ into two sub-blocks θ_S and θ_Q, as shown in Fig. 4.2. The adder (add-2) and θ_Q belong to the combinatorial circuitry that produces the output (Y) whereas the combinatorial circuitry that is composed of the add-1 and the θ_S produces the error-feedback signal (E). The split does not alter the transfer characteristics.

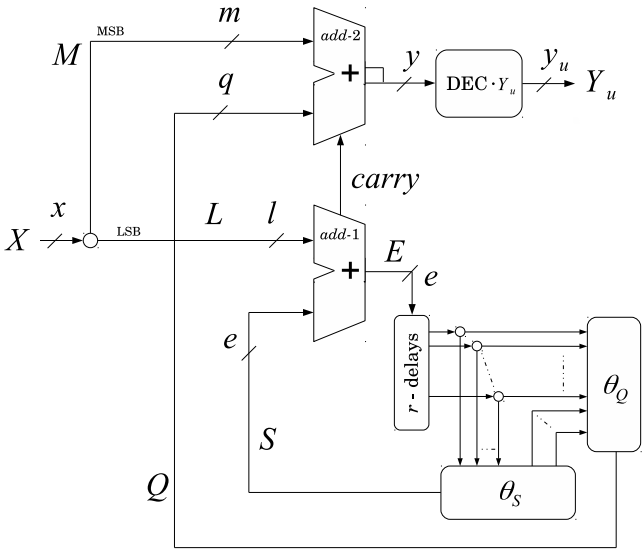


Figure 4.2: The circuitry of conv-EFMr (shown in Fig. 3.3) is split into the θ_S and θ_Q.

4.2.2 Design Step II

In the second design phase, an architectural property: an adder is removed if the binary-to-unitary decoder at its output is propagated back to its inputs, is utilized. The decoding operation is explained with the help of the following mathematical model. The ith time-domain sample of Y_u is described as

$$Y_u[i] = \sum_{\forall y_u} y_u[i] = Y[i] + \left|Y^-\right|. \tag{4.1}$$

where y_u is the uth bit of unitary code. In order to explain the architecture property further, consider an example of the two setups shown in Fig. 4.3. Assume that the ith sample of the inputs to the adder has the following values: $M[i] = -4 = (100)_2$, $Q[i] = 3 = (011)_2$ and $carry[i] = 0$ (all of the signals are represented in two's complement). Then, in the setup of Fig. 4.3a, output of the adder, $Y[i] = -1 = (1111)_2$ is decoded to unitary coded signal $Y_u[i] = Y[i] + 2^3 = 7 = (000000001111111)_1$ using DEC·Y_u where -2^3 is theoretical negative peak of a 4-bit signal. In the alternative setup, Fig. 4.3b, the $M[i]$ and $Q[i]$ are first decoded to $M_u[i] = -4(i) + 2^2 = (0000000)_1$ and $Q_u[i] = 3+2^2 = (1111111)_1$ by the DEC·M_u and the DEC·Q_u, respectively, and then joined along with $carry$ to produce $Y_u^{'}[i] = (000000011111110)_1 = 7$. The

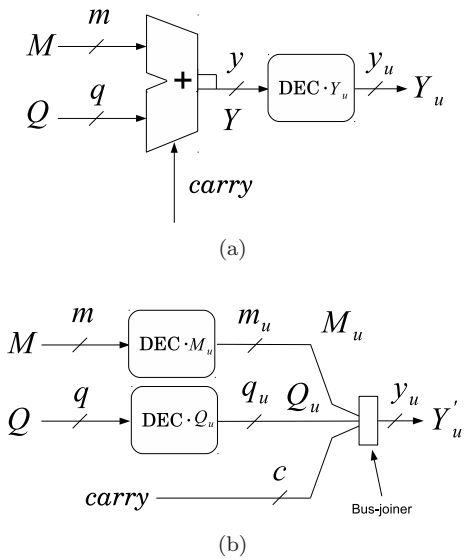


Figure 4.3: An adder is removed by replacing single larger decoder, DEC·Y_u, with two smaller sub-decoders, DEC·M_u and DEC·Q_u.

codes patterns could be different but numerically both the setups are equivalent since the total number of ones in both Y_u and $Y_u^{'}$ are equal.

Thus, by applying this principle to conv-EFMr of Fig. 4.2, *add*-2 is removed using DEC·Y_u. After removing *add*-2, the DEC·Y_u is replaced with DEC·M_u and DEC·Q_u. Then, by using the DEC·Q_u, the outer most adder in θ_Q is removed and the process continues until the decoder blocks reach to the sequential circuitry. The resulting design, prop-EFMr, is shown in Fig. 4.4a. Block D in the figure is a low-power implementation of the H where K is represented with the set $\{k^1,\ k^2, \ldots, k^v\}$. The ith sample of K is described as

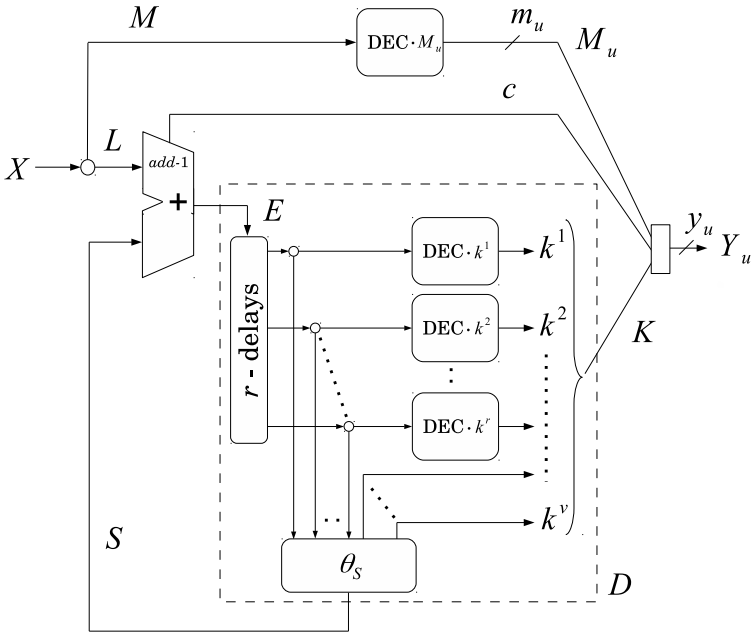
$$K\left[i\right] = k^1\left[i\right] + k^2\left[i\right] + \cdots + k^v\left[i\right] = Q\left[i\right] + \left|Q^-\right|, \tag{4.2}$$

where v is the word length of K given by

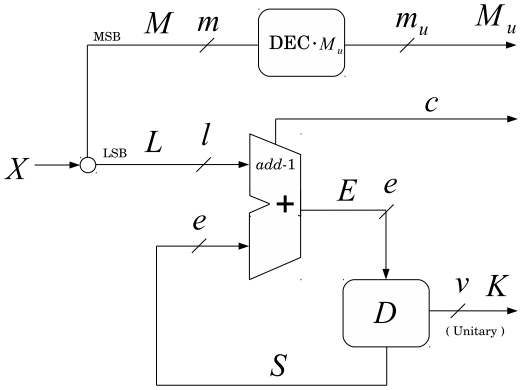
$$v = Q^+ - Q^-. \tag{4.3}$$

The unitary coded output of the prop-EFMr can now be represented by a set of signals as

$$Y_u = \{M_u, c, K\}. \tag{4.4}$$



(a)



(b)

Figure 4.4: (a) The proposed error-feedback modulator of arbitrary order r (prop-EFMr.) (b) The block diagram of prop-EFMr where the output is represented by a set of three signals M_u, c and K.

The block diagram of the prop-EFMr is shown in Fig. 4.4b where the output branches which need to be added in the analog domain, have the following z-transforms

$$\begin{aligned} 2^l M_u(z) &= X(z) - L(z) + \left|M^-\right|, \\ 2^l c(z) &= L(z) + S(z) - E(z), \\ 2^l K(z) &= E(z) H(z) - S(z) + \left|Q^-\right|, \end{aligned} \tag{4.5}$$

where $|M^-|$ and $|Q^-|$ are the DC terms added while decoding the signals M and K. The relations show that all of the output signals are at the same significance, hence, no additional relative scaling is required. The addition between these signals is transferred to the analog domain. Thus, once the signals are added in the analog domain, the final z-transform expression turns to be the same as that of the conventional EFM, i.e.,

$$2^l M_u(z) + 2^l c(z) + 2^l K(z) = X(z) + E(z)(H(z) - 1) + \left|M^-\right| + \left|Q^-\right|. \tag{4.6}$$

The proposed design will be more effective if the analog addition is simple, for example a wire connection in the case of a current-mirror DAC.

The proposed method saves hardware due to the fact that the resulting modulator accumulates less number of error bits but produces the same total number of ones as compared to the original architecture, conv-EFMr. The prop-EFMr can be seen as the modulator with several quantizers that truncates multiple branches towards the output.

The sizes of *add*-1 and D in Fig. 4.4a will scale with the input word length. However, the removed circuitry (*add*-2 and θ_Q in Figs. 4.2) is independent of the input word length. Hence, one can expect that the relative area savings as well as speed-up increase with shorter input word length.

In addition to the savings in hardware, the shorter carry chains of the proposed design reduces the critical path and it can operate at a higher clock frequency.

4.3 Proposed Cascaded Error-feedback Modulator

In this section, another hardware reduction method, i.e., by cascading multiple loop filters, is presented [Paper D]. The idea is to split the error signal and process it through multiple loop filters of different orders.

At first the proposed design, termed as prop-EFMr_1r_2, consisting of cascade of two loop filters, $H_{r_1}(z) = 1 - \left(1 - z^{-1}\right)^{r_1}$ and $H_{r_2}(z) = 1 - \left(1 - z^{-1}\right)^{r_2}$ where $r_1 < r_2$, is presented. Then, the proposed design consisting of an arbitrary, n, number of loop filters is presented. This design is termed as prop-EFM$r_1r_2\ldots r_n$.

The implementation of prop-EFMr_1r_2, is shown in Fig. 4.5a. The input is split, in a similar fashion as it was done in Fig. 4.4, into an l-bit signal, L, and an m-bit signal, M. Signals M_u and c are the part of the set which represents the output, thus, the signals have the relation similar to that described in (4.5), as

$$\begin{aligned} 2^l M_u(z) &= X(z) - L(z) + \left|M^-\right|, \\ 2^l c(z) &= L(z) + S(z) - E(z). \end{aligned} \tag{4.7}$$

Due to the fact that the filter coefficients of the loop filters are integer-valued, the word lengths of L, E and S equal l. Signal E is split into an l_{r_1}-bit signal, E_{r_1}, and the l_{r_2}-bit signal, E_{r_2}. The split signals are, then applied to two different loop filters. The signals are related, according to (2.14), as

$$E(z) = E_{r_1}(z) + 2^{l_{r_1}} E_{r_2}(z). \tag{4.8}$$

Blocks D_{r_1} and D_{r_2} are the reduced-hardware implementations of the H_{r_1} and H_{r_2}, respectively. The design of D_{r_1} is similar to that shown in Fig. 4.4. Thus, its inputs and outputs are related, according to (4.5) as

$$2^{l_{r_1}} K_{r_1}(z) = E_{r_1}(z) H_{r_1}(z) - S_{r_1}(z) + \left|Q_{r_1}^-\right|. \tag{4.9}$$

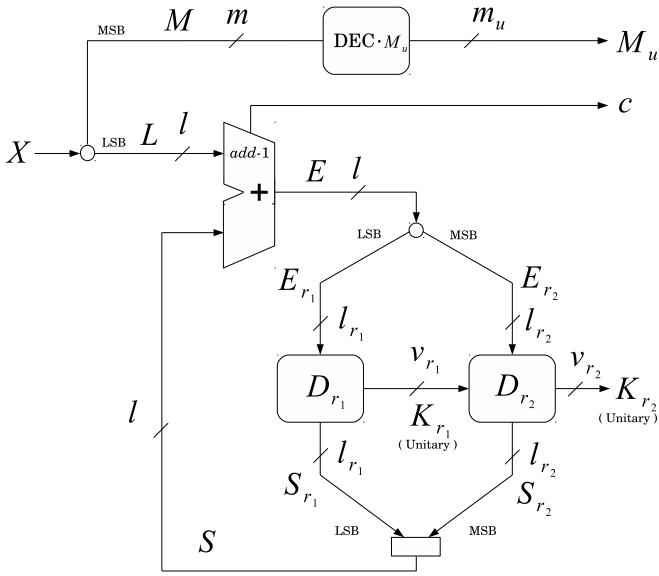
Block D_{r_2} has a slightly modified architecture, as shown in Fig. 4.5b, hence, the unitary coded signal from D_{r_1}, i.e., $K_{r_1} = \{k_{r_1}^1, k_{r_1}^2, \ldots, k_{r_1}^{v_{r_1}}\}$ is applied to the carry-in locations of the adders in D_{r_2} (the design is explained in chapter 5 with the help of an example.) The output of D_{r_2} is given by

$$2^l K_{r_2}(z) = 2^{l_{r_1}} E_{r_2}(z) H_{r_2}(z) - 2^{l_{r_1}} S_{r_2}(z) + 2^{l_{r_1}} \left|Q_{r_2}^-\right| + 2^{l_{r_1}} K_{r_1}(z), \tag{4.10}$$

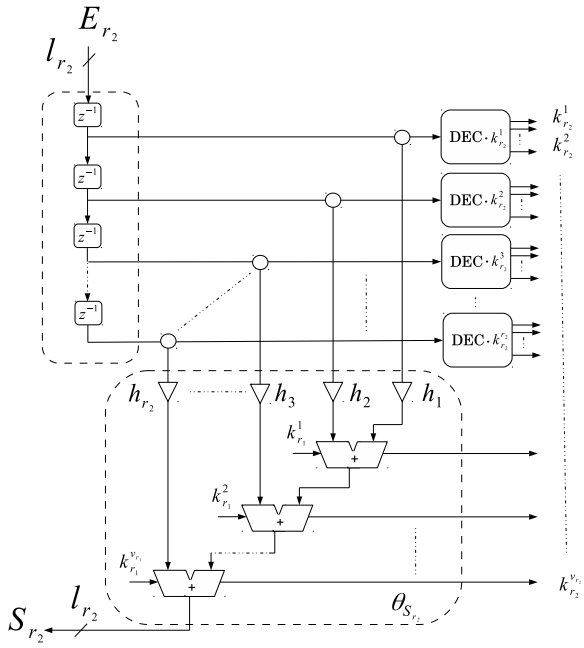
where $K_{r_2} = \{k_{r_2}^1, k_{r_2}^2, \ldots, k_{r_2}^{v_{r_2}}\}$. By substituting (4.9) in (4.10), we get

$$2^l K_{r_2}(z) = E_{r_1}(z) H_{r_1}(z) + 2^{l_{r_1}} E_{r_2}(z) H_{r_2}(z) - S(z) + \left|Q^-\right|, \tag{4.11}$$

where $S(z) = S_{r_1}(z) + 2^{l_{r_1}} S_{r_2}(z)$ and $|Q^-| = \left|Q_{r_1}^-\right| + 2^{l_{r_1}} \left|Q_{r_2}^-\right|$. The relations in (4.7) and (4.11) jointly give the transfer function of the output of the



(a)



(b)

Figure 4.5: (a) The block diagram of proposed cascaded EFM (prop-EFMr_1r_2, where two loop filters of orders r_1 and r_2, are cascaded.) (b) The schematic of D_{r_2}.

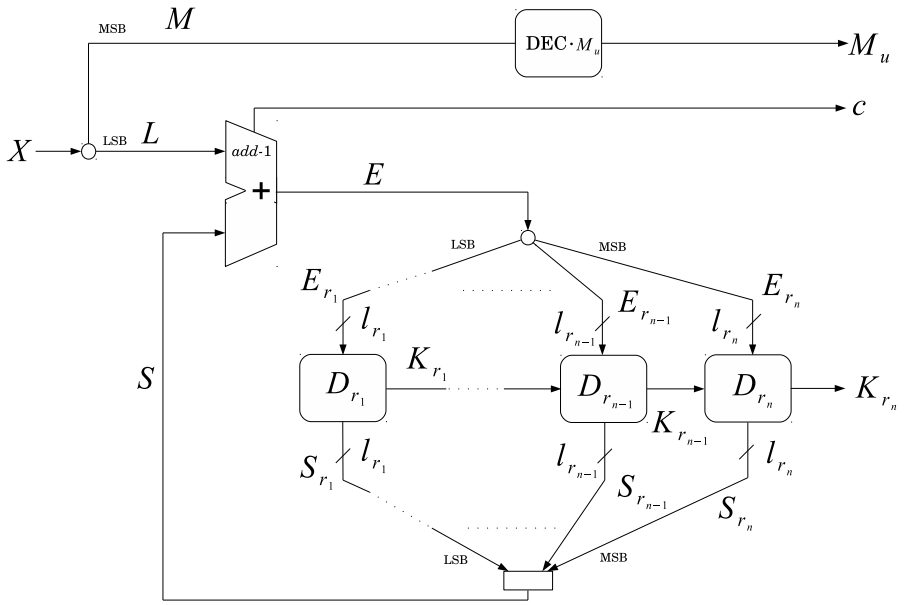


Figure 4.6: The block diagram of proposed cascaded EFM, prop-EFM$r_1 r_2 \ldots r_n$, where arbitrary, n, number of loop filters are cascaded.

prop-EFM$r_1 r_2$, as

$$2^l M_u(z) + 2^l c(z) + 2^l K_{r_2}(z) = X(z) + E_{r_1}(z)(H_{r_1}(z) - 1) + 2^{l_{r_1}} E_{r_2}(z)(H_{r_2}(z) - 1) + \left|M^-\right| + \left|Q^-\right|. \tag{4.12}$$

Similarly, the modulator design consisting of the cascade of n number of loop filters is shown in Fig. 4.6. Its transfer function can be expressed, according to (4.12), as

$$2^l M_u(z) + 2^l c(z) + 2^l K_{r_n}(z) = X(z) + \sum_{i=1}^{n} 2^{\left(\sum_{j=1}^{i} l_{r_j}\right)} E_{r_i}(z)(H_{r_i}(z) - 1) + \left|M^-\right| + \left|Q^-\right|, \tag{4.13}$$

where $l_{r_1} + l_{r_2} + \cdots + l_{r_n} = l$. Signal E is split into $E_{r_1}, E_{r_2}, \ldots, E_{r_n}$ and applied to $D_{r_1}, D_{r_2}, \ldots, D_{r_n}$, respectively. The transfer function is similar to that of described in [94] (where multiple error-feedback modulators are cascaded.) The output of prop-EFM$r_1 r_2 \ldots r_n$ finds the contributions of the shaped noise from

each of the loop filter. By applying the expression (2.19) to each stage in (4.13), the total in-band noise at the output of prop-EFM$r_1 r_2 \ldots r_n$ is obtained as

$$\mathcal{N}_{r_1 r_2 \ldots r_n} = \sum_{i=1}^{n-1} 2^{\left(2\sum_{j=1}^{i} l_{r_j}\right)} \lambda_{r_i} + 2^{\left(2\sum_{j=1}^{n} l_{r_j}\right)} \lambda_{r_n}. \tag{4.14}$$

For a comparison with the prop-EFMr, assume $r_n = r$, then, according to (2.20), we have $2^{\left(2\sum_{j=1}^{n} l_{r_j}\right)} \lambda_{r_n}/12 = 2^{2l}\lambda/12 = \mathcal{N}$. Thus, (4.14) is modified to

$$\mathcal{N}_{r_1 r_2 \ldots r} = \sum_{i=1}^{n-1} 2^{\left(2\sum_{j=1}^{i} l_{r_j}\right)} \lambda_{r_i} + \mathcal{N}. \tag{4.15}$$

Hence, the total in-band noise is increased by an additional factor,

$$\sum_{i=1}^{n-1} 2^{\left(2\sum_{j=1}^{i} l_{r_j}\right)} \lambda_{r_i}$$

compared to that of prop-EFMr. However, the $\mathcal{N}_{r_1 r_2 \ldots r}$ can be kept within the desired limit by carefully configuring the parameters like $l_1, \ldots, l_n$ and $r_1, \ldots, r_{n-1}$. The trade-off of the SNR against the parameters configurations have previously been reported in [94]. Thus, our contribution is the reduced hardware architecture, prop-EFM$r_1 r_2 \ldots r$, as shown in Fig. 4.6.

Conclusively, the prop-EFM$r_1 r_2 \ldots r$ has a reduced-hardware complexity compared to prop-EFMr due to the fact that only l_{r_n} number of error bits are processed through the rth order loop filter. Furthermore, its hardware is significantly less compared to the previously reported implementation (where the EFMs are cascaded, as in [94]) because only the loop filters are cascaded instead of whole EFM stages. The comparison is presented in [Paper D].

4.4 Conclusions

A method of reducing hardware of the multi-bit error-feedback $\Delta\Sigma$ modulator of arbitrary order has been presented. The method has utilized the bus-splitter and the binary-to-unitary decoder. A modified lower hardware implementation of the loop filter has also been presented by following the proposed strategy.

Another method of reducing the hardware further has also been reported. The error signal has been split and applied to multiple loop filters. The reduction in the input bits to the highest order loop filter decreases the overall hardware of the modulation system. The hardware reduction using multiple loop filters comes at a cost of additional in-band noise.

Chapter 5

Comparison of Hardware, Power and Speed

5.1 Introduction

In this chapter, the hardware reduction methods that have been presented in the previous chapter, are evaluated by examples. Two five-bit modulation systems, the EFM4 (single-stage error-feedback modulator of order four) and the EFM24 (a cascade of second- and fourth-order error-feedback modulators), were described in VHDL using the conventional and the proposed approaches. The designs were realized with the loop filters given in (3.14).

In order to obtain the hardware estimates, the designs were synthesized using Synopsys Design Compiler under different delay constraints, in steps of 0.05 GHz, in a 65-nm standard cell library from ST Microelectronics. The best cases were selected for presentation after performing more than 50 synthesize runs using random seeds for each delay constraint. Dynamic power consumption was obtained after back-annotating the switching activities for a total of 2^{16} uniformly distributed random input samples. The input bus for all of the designs was 17-bit.

5.2 Single-stage Error-feedback Modulators

According to sections 3.4 and 3.5 a 5-bit full-scale output can be obtained by either of the first-, second-, third- or fourth-order EFM when configured according to C_{II} or by fifth-order EFM when configured according to C_I (the

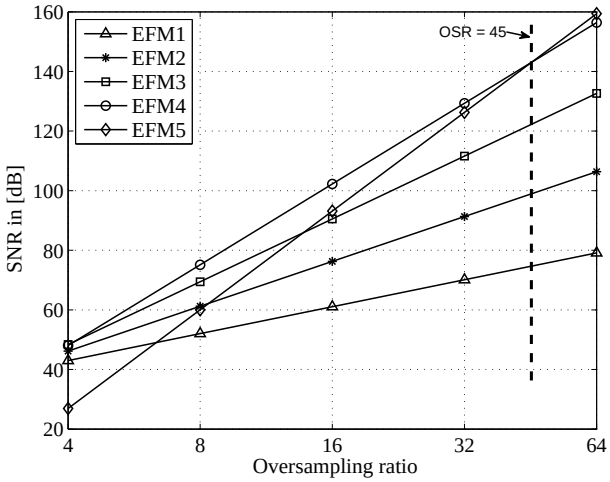


Figure 5.1: Signal-to-noise ratio of conv-EFMs of order from one to five over low OSR (oversampling ratio) values.

configurations are explained in 3.5.2). Due to the fact that the low-OSR applications are targeted, the SNR of the designs for OSR values up to 64 are shown in Fig. 5.1 using (3.21). It can be observed that the fourth-order modulator (EFM4) produces best SNR as long as the OSR is less than 45 (the value can also be calculated from (14) after substituting $\delta = 1$ and $y = 5$.) Thus, we chose to realize the 5-bit EFM4 for the OSR values less than 45. The transfer-function of the loop filter of the EFM4 can be obtained by (3.14) is

$$H_4(z) = 4z^{-1} - 6z^{-2} + 4z^{-3} + z^{-4}. \tag{5.1}$$

The Q for this loop filter can be represented with 4-bits since the range of Q is $\{-7, 7\}$ according to (3.11). In order to produce a 5-bit output of range $\{-15, 15\}$, four MSBs should be split from the input to M according to (3.18) and (3.19).

A multiplier-less implementation of conv-EFM4 is shown in Fig. 5.2a. The P is obtained after implementing the loop filter with four adders as

$$P(z) = E(z)\,H_4(z) = 4\left(E_{z^{-1}} + E_{z^{-3}}\right) + \overline{2\left(2E_{z^{-2}} + E_{z^{-2}}\right)} + 1 + \overline{E_{z^{-4}}} + 1, \tag{5.2}$$

where $E_{z^{-i}} = E(z)\,z^{-i}$ and every subtraction is implemented using an addition, e.g., $A - B$ is transformed into $A + \overline{B} + 1$ where $\overline{B}$ represents bit reversal.

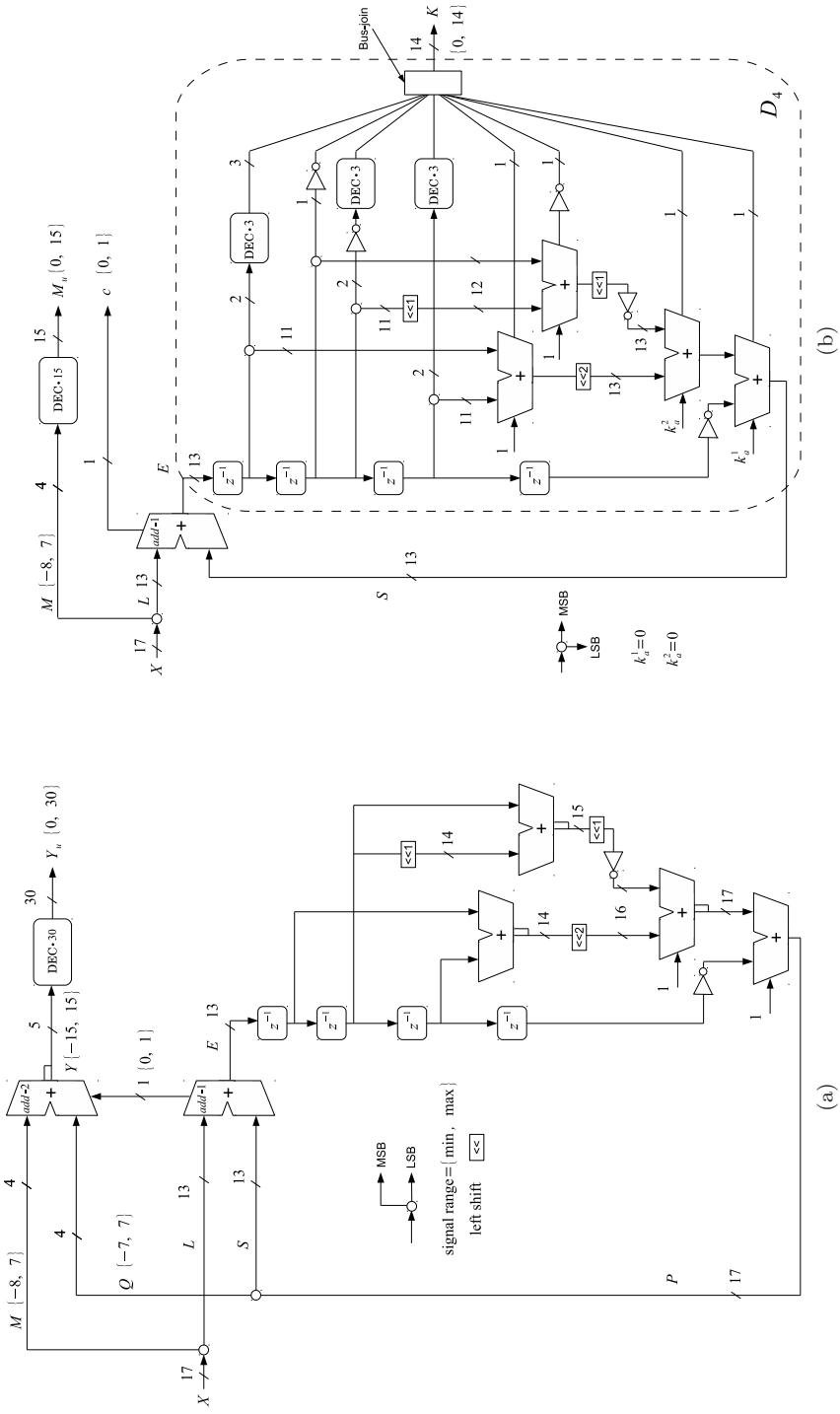


Figure 5.2: Implementation details of fourth-order single-stage EFM (a) The schematic of conv-EFM4 (conventional architecture, according to Fig. 3.3). (b) The schematic of prop-EFM4 (proposed architecture, according to Fig. 4.4).

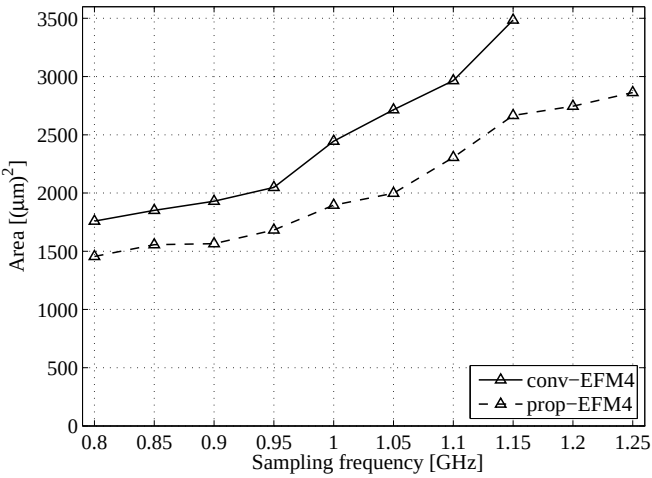


Figure 5.3: Area for the conventional and the proposed architectures of single-stage EFM of order four over sampling frequency.

In the modified design (prop-EFM4) shown in Fig. 5.2b, the *add*-2 is removed, the combinatorial circuitry is split and the Q-producing circuitry is removed using the DEC·30 by following the procedure given in Section 4.2 and [Paper C]. The DEC·30 is replaced with four sub-decoders. In the prop-EFM4, the output is represented by unitary decoded signals M_u, c and K. The M_u is the decoded signal of the 4 MSBs of the input. The c is the carry-out of the *add*-1 and the K is obtained by joining the branches from the decoders and the carry-outs from the adders within the modified implementation of the loop filter. The word length of the K is given, according to (4.3), as $v_4 = 14$. The modified circuitry of the loop filter is labeled as D_4 where the k_a^1 and k_a^2 are the unitary weighted signals.

The resulting area and the dynamic power consumption are shown Fig. 5.3 and 5.4, respectively. The results show that the proposed approach saves more than 26% of the area for the best case at a common operating frequency. The power consumption follows the same trend, with the prop-EFM4 always producing better results, this time with savings of more than 33%. The static power consumption, not shown, is in the range of just below 2% up to almost 3% of the dynamic power consumption for all the designs, and, hence, does not alter the conclusions. For the prop-EFM4, the maximal clock frequency is increased from 1.15 to 1.25 GHz.

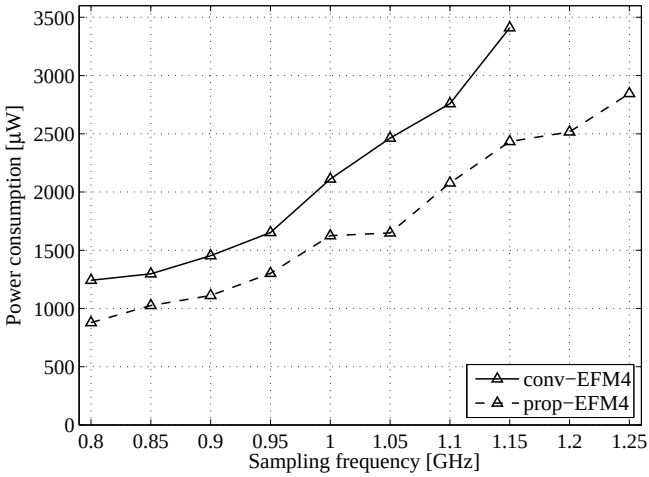


Figure 5.4: Dynamic power for the conventional and the proposed architectures of single-stage EFM of order four over sampling frequency.

5.3 Cascaded Error-feedback Modulators

In this section, an implementation of a 5-bit cascaded fourth-order error-feedback modulator is presented. According to the procedure described in section 4.3, the modulator can cascade any combination of the loop filters from D_1 to D_4, as shown in Fig. 4.6, as long as the order of every of the preceding is lower than all of the following loop filters. The implementation of one of these combinations: a cascade of the D_2 (second-order loop filter) and D_4 (fourth-order loop filter), termed as prop-EFM24, is presented here. For the other combinations the reader is referred to [Paper D].

The architecture of the prop-EFM24 is shown in Fig. 5.5. The E is split into E_2 and E_4 of word lengths l_2 and l_4, and applied to the D_2 and the D_4, respectively. The values of l_2 and l_4 has been calculated using (27) and shown against the OSRs in Table. 5.1. For these values, the prop-EFM24 produces a less than 1 dB deviated SNR from that of the prop-EFM4 shown in Fig. 5.1. The procedure to obtain D_2 from the conventional implementation of the H_2 is shown in Fig. 5.6. The only adder in Fig. 5.6a is split, then the Q_2 producing part is removed and the unitary weighted K_2 is taken to the output. The K_2 is applied to D_4, by using $k_a^1 = k_2^1$ and $k_a^2 = k_2^2$, where the architecture of D_4 is already shown in Fig. 5.2b. The output is represented with the M_u, c and the K_4, and its range is not different than that of the prop-EFM4, i.e., $\{0, 14\}$.

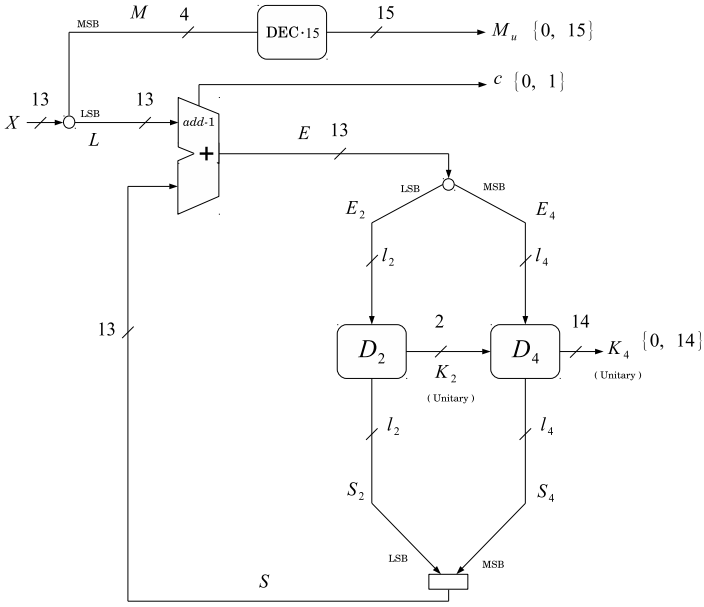


Figure 5.5: The schematic of prop-EFM24 (proposed architecture of the EFM where a second- and a fourth-order loop filters are cascaded).

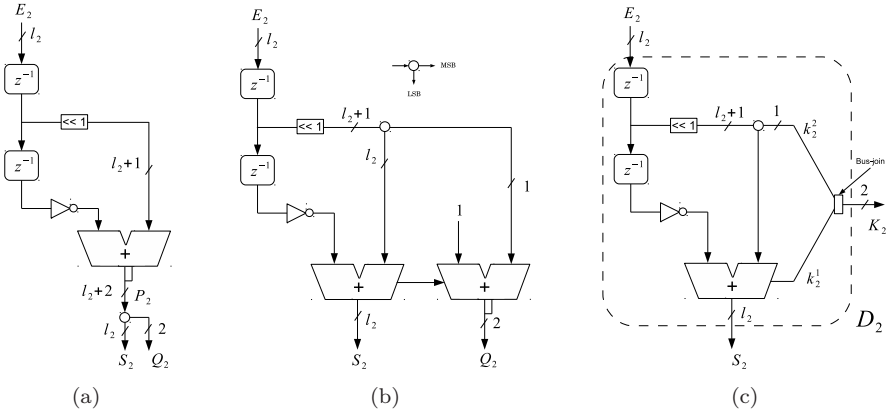


Figure 5.6: Block D_2 is obtained as the modified implementation of the H_2.

Table 5.1: The split configurations of the prop-EFM24 with less than 1 decibel additional in-band noise compared to that of EFM4 ($l = 13$) for various OSR values.

OSR	32	16	8	4
prop-EFM24 (l_2, l_4)	$(5, 8)$	$(7, 6)$	$(9, 4)$	$(11, 2)$

The trade-offs between, the area, the dynamic power, the sampling frequency and the OSR for the prop-EFM24 are shown in Figures 5.7 and 5.8. The hardware cost increases with the increase in sampling frequency or the OSR. The designs with lowest OSR values allow the highest sampling frequencies, for instance, with OSR values of 4 and 8 the the prop-EFM24 is operated at sampling frequency as high as 1.75 GHz.

It was shown in the previous section that the conv-EFM4 can be operated at a maximum sampling frequency of 1.15 GHz. At this sampling frequency, the prop-EFM4 implementation saves an area and power of 23.5% and 28.6%, respectively compared to the conv-EFM4. At the same sampling frequency, the prop-EFM24 saves even more as shown in Table 5.2. The highest area and power savings of 76.2% and 81%, respectively, are obtained at OSR of 4. The static power consumption of all of the designs is less than 2%, thus, do not change the conclusions.

5.4 Conclusions

In this chapter, we have presented the results of single-stage error-feedback $\Delta\Sigma$ modulators after implementing these using the conventional and proposed approaches. The proposed methods save up to 23% of area and 28% of dynamic power consumption.

We have also presented the results of the proposed error-feedback modulators consisting of two loop filters in cascade. A reduction in area and power consumption up to 76% and 81%, respectively, is observed as compared to the conventional realization of the single-stage error-feedback modulator at the cost of about 1.5 dB additional in-band noise.

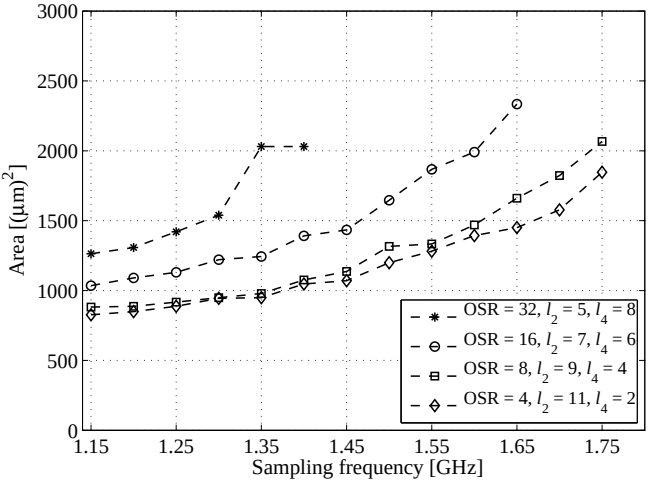


Figure 5.7: Area of the prop-EFM24 over sampling frequency for various OSR values.

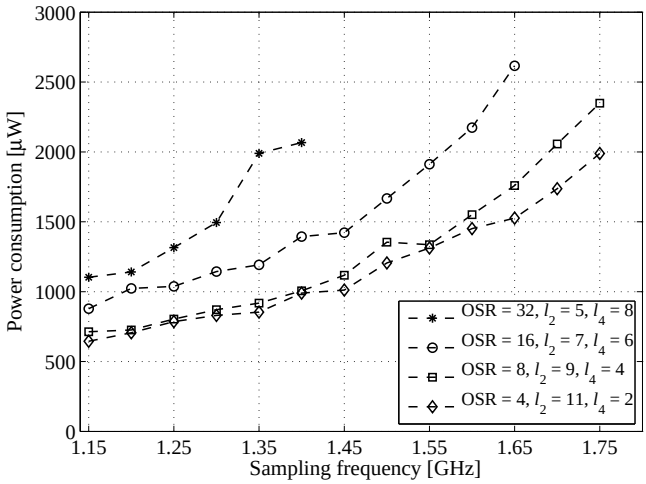


Figure 5.8: Dynamic power of the prop-EFM24 over sampling frequency for various OSR values.

Table 5.2: Savings of the area and the dynamic power consumption in the prop-EFM4 and prop-EFM24 compared to those of conv-EFM4 at the sampling frequency of 1.15 GHz.

Design	OSR	Results		Savings from (a)	
		Area $[(\mu m)^2]$	Power $[\mu W]$	Area [%]	Power [%]
(a) conv-EFM4	$\{4, \ldots, 32\}$	3485	3410	-	-
prop-EFM4	$\{4, \ldots, 32\}$	2666	2433	23.5	28.6
prop-EFM24	32	1263	1103	63.7	67.6
	16	1035	878	70.3	74.2
	8	882	713	74.6	79
	4	826	645	76.2	81

Furthermore, by trading the area and the power consumption against the sampling frequency of the designs, the proposed designs are found to be faster compared to the conventional design. The savings are presented in the form of silicon area, dynamic power consumption and sampling frequency.

Chapter 6

Conclusions and Future Trends

In this chapter, the work presented in this thesis is concluded and the future extensions are identified.

6.1 Conclusions

For the targeted applications, low power and high-speed digital $\Delta\Sigma$ modulators were required. In order to meet the demands, a number of hardware reduction methods have been presented. The techniques have been described in the form of mathematical expressions and architectural modification procedures. In short, the presented expressions have discussed the principle of scaling the input to multi-bit error-feedback $\Delta\Sigma$ modulators (EFM) of arbitrary order which does not only remove the over-design but also guarantees stable operation. The configurations of the modulator parameters that produce the maximum signal-to-noise ratio, have also been derived from the expressions.

By applying the devised modification method, the non-critical circuitry in the single and the cascaded EFM has been removed. The mathematical expressions of the signal ranges have been used such that the hardware can be designed to avoid the possibilities of overflows. The resulting designs not only consume less dynamic power but also operate at higher speeds compared to conventional designs.

The proposed methods have been evaluated by implementing a number of design examples. The area, dynamic power consumption and the highest operable sampling frequency of a conventional EFM have been considered as reference for

comparisons. The modified architectures when implemented using the proposed approaches provide significant savings compared to the reference values.

The highest operating speeds have been established by synthesizing the design configurations against several delay constraints. Across each of the delay constraints, a number of synthesize runs were performed to search the best cases. The area numbers were obtained for the placed and routed designs in CMOS 65-nm process using standard components provided by the foundry. In order to obtain the dynamic power consumption, the switching activity for 2^{16} simulation points, were back annotated.

6.2 Future Extensions

As a result of the hardware reduction methods adopted in this work, the modulators output are represented with multiple binary weighted signals. The requirements on the design of the signal processing blocks which would be placed after such a modulator, could be unconventional. In this regard, the suggestions are presented as follows:

In order to generate unitary-weighted control signals to access a unit element based DAC, the proposed designs require the modified binary-to-unitary decoding strategies. One possible way is to divide the conventional single large decoder into a number of small sub-decoders. This needs further investigation since the modifications may produce different patterns of the unitary codes.

Furthermore, usually, a matching network is required, in order to remove the non-linearity of a multi-bit DAC. In order to obtain linearity of the DAC, the proposed designs may put tighter requirements on the construction of the matching network mainly due to the multiple branches at the output. The trade-off relating to the over-all power consumption, complexities, speed etc., of the digital blocks: $\Delta\Sigma$, decoders and the matching network, could be another research direction.

The binary-weighted or segmented DACs can also be used with the proposed $\Delta\Sigma$ designs although the unit element based DACs have been our main focus in this thesis. Due to the fact that the output of the modulator does not require relative scaling within its branches, it provides a natural segmentation strategy for the DAC. The elements of each DAC segment could be matched by the sub dynamic element matching block. It is a vast research subject itself, however, some conservative investigations may lead to the solutions compatible to the proposed $\Delta\Sigma$ modulator designs.

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Publications

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